Khalid Munawar

POWER ELECTRONICS

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POWER ELECTRONICS
M.S. Jamil Asghar

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To my best teachers

- **Mrs. Sunaina Devi**
- **Dr. Shamsuddin Ahmed**
- **Prof. M. Salman Beg**

Contents

Preface *xi*

Chapter 1 Introduction to Power Electronics **1–19**

1.1 Introduction *1*
1.2 Scope and Applications *3*
1.3 Evolution of Power Electronics *10*
1.4 Classification of Power Electronic Converters *13*
1.5 Requirements of an Ideal Switching Device *16*
1.6 Ideal Switch *18*
1.7 Classification of Power Electronic Devices *18*
Summary *19*
Review Questions and Problems *19*

Chapter 2 Power Semiconductor Devices **20–80**

2.1 Introduction *20*
2.2 Classification of Devices *20*
2.3 Diodes (Uncontrolled Rectifiers) *21*
2.3.1 General-purpose Power Diodes *22*
2.3.2 Schottky Power Diodes *23*
2.3.3 Fast-recovery Power Diodes *23*
2.3.4 Power Zener Diodes *23*
2.3.5 Thyrectors or Metal-oxide Varistors (MOV) *24*
2.3.6 Tunnel Diodes *24*
2.3.7 Unijunction Transistor (UJT) *25*
2.3.8 Diacs *26*
2.3.9 Photodiodes *26*
2.3.10 Light-emitting Diodes (LED) *26*
2.4 Thyristors (Controlled Rectifiers) *27*
2.4.1 Silicon Controlled Rectifiers (SCR) *27*
2.4.2 Forward-blocking (FB) Region *28*
2.4.3 Forward Conducting (FC) Region *29*
2.4.4 Reverse-blocking (RB) Region *30*
2.4.5 Triggering of Thyristor *30*
2.4.6 Dynamic Switching Characteristics of SCR *31*
2.4.7 Effect of *dv/dt* and Snubber Circuits *35*
2.4.8 Effect of Rate of Rise in Current (*di/dt*) *38*
2.4.9 Thyristor Gate Characteristics *39*
2.4.10 Turn-off Characteristics *40*
2.4.11 Thyristor Ratings *41*
2.4.12 Thyristor Protection *43*

2.4.13 Series and Parallel Operation of Thyristors *44*
2.4.14 Commutation of SCR *50*
2.5 Other Thyristors *50*
2.5.1 Triac *51*
2.5.2 Light Activated SCR (LASCR) *52*
2.5.3 Reverse Conducting Thyristor (RCT) *52*
2.5.4 Asymmetrical SCR (ASCR) *52*
2.6 Gate Commutation Devices *53*
2.6.1 Gate Turn-off Thyristors (GTO) *53*
2.6.2 Power Bipolar-junction Transistors (Power BJT) *55*
2.6.3 Metal-oxide Semiconductor Field-effect Transistors (MOSFET) *56*
2.6.4 Insulated-gate Bipolar Transistors (IGBT/IGT) *63*
2.6.5 Static Induction Devices *66*
2.6.6 MOS-controlled Thyristors (MCT) *70*
2.7 A General Comparison of Devices *71*
2.7.1 General Performance of Devices *71*
2.7.2 Ideal Characteristics of Devices *73*
2.7.3 Relative Performance of MOSFET/BJT/SCR *74*
2.8 Manufacturer's Data Sheet *75*
2.9 General Considerations *76*
2.10 Power Modules *77*
2.11 Application of Devices *78*
Summary 79
Review Questions and Problems 79

Chapter 3 Triggering Circuits for Thyristors 81–111

3.1 Introduction *81*
3.2 Thyristor Gate Requirements *81*
3.3 Trigger Circuits for Thyristors *84*
3.4 Simple Gate Trigger Circuits for Thyristors *86*
3.4.1 Resistance Trigger Circuits *86*
3.4.2 *RC* Trigger Circuits *87*
3.4.3 Diac Trigger Circuits *91*
3.4.4 AC-thyratron Type Trigger Circuits *93*
3.4.5 UJT-based Trigger Circuits *94*
3.4.6 Advanced Triggering Circuits for Thyristors *99*
3.4.7 Driver and Buffer Circuits for Thyristors *99*
3.5 A Master Triggering Control (MTC) Circuit *103*
3.6 Some Practical Triggering Circuits *105*
3.6.1 Simple Triggering Circuits *105*
3.6.2 IC-based Advance Triggering Circuits *106*
3.6.3 Microprocessor-based Trigger Circuits *108*
Summary 110
Review Questions and Problems 111

Chapter 4 Driver Circuits for Gate-commutation Devices 112–126

4.1 Introduction *112*
4.2 Gate Drive Circuits for Power MOSFET *113*
4.2.1 Gate and Device Capacitances *113*
4.2.2 Different Driver Circuits *115*
4.2.3 Design Considerations of MOSFET-driver Circuits *118*

4.3 Driver Circuits for IGBT *120*
4.4 Base-drive Circuits for Power BJT *121*
4.5 Gate-drive Circuits for GTO *122*
4.6 Some Practical Driver Circuits *123*
Summary *126*
Review Questions *126*

Chapter 5 AC Voltage Regulators 127–186

5.1 Introduction *127*
5.2 On-off or Integral-cycle Control (ICC) *128*
5.3 Principle of Phase Controlled Switching *130*
5.4 Full Wave with *R* Load *133*
5.5 Harmonic Analysis of Converters *136*
5.6 Analysis of ac Voltage Regulators with *R* Load *143*
5.7 Full Wave with *RL* Load *147*
5.8 AC Regulators with Pure Inductors *153*
5.9 Three-phase ac Regulators *158*
5.9.1 Circuit Configurations *158*
5.9.2 Y-connected, *R* Loads *160*
5.9.3 Delta-connected Load (*T-R* Load Configuration) *165*
5.9.4 Delta-connected *R* Loads *168*
5.10 Electronic Tap Changers *170*
5.11 AC Chopper Regulators *173*
5.12 AC Chopper with Multiple PWM Control *176*
5.13 Cycloconverters *177*
5.13.1 Single-phase Cycloconverters *177*
5.13.2 Three-phase-to-single-phase Cycloconverters *179*
5.13.3 Three-phase Cycloconverters *180*
5.14 Discontinuous Phase-controlled Switching *181*
Summary *185*
Review Questions *186*

Chapter 6 Phase-controlled (ac-to-dc) Converters 187–248

6.1 Introduction *187*
6.2 Converter Rectifiers *188*
6.3 Uncontrolled Converters *188*
6.3.1 Half-wave, Uncontrolled Converters *189*
6.3.2 Half-wave, Uncontrolled Converters with a Freewheeling Diode *191*
6.3.3 Half-wave, Uncontrolled Converters with *RC* Loads *192*
6.3.4 Full-wave, Uncontrolled Converters *193*
6.4 Controlled Converters *195*
6.4.1 Half-wave, Fully-controlled Converters *195*
6.4.2 Half-wave, Half-controlled Converters *197*
6.4.3 Full-wave, Half-controlled Converters *197*
6.4.4 Full-wave, Full Converters *201*
6.4.5 Full-converters with *RLE* Load *205*
6.5 Analysis of Converters *209*
6.5.1 Analysis of Semi-converters *210*
6.5.2 Full Converters *211*

6.6 Three-phase Converters *213*
6.6.1 Rectifier Operation *214*
6.6.2 Three-phase, Uncontrolled Converters *216*
6.6.3 Three-phase, Controlled Converters *222*
6.7 Effect of Source Impedance (or Overlap) *231*
6.8 Multiple Converters *236*
6.8.1 Single-phase, Parallel Dual Converters *237*
6.8.2 Three-phase Dual Converters *238*
6.8.3 Series Multiple-stage Converters *239*
6.8.4 Three-phase Converters *241*
6.9 Twelve-pulse Converters *241*
6.9.1 Twelve-pulse Series Converters *242*
6.9.2 Twelve-pulse Parallel Converters *243*
6.10 Reactive Power of Converters *244*
Summary *246*
Review Questions and Problems *246*

Chapter 7 DC-to-DC Converters 249–298

7.1 Introduction *249*
7.2 Principle of dc Choppers *250*
7.3 Classifications of dc Choppers *254*
7.4 Forced-commutated Thyristor-based Choppers *256*
7.4.1 Voltage or Impulse Commutation *257*
7.4.2 Resonant Pulse-commutated Chopper *260*
7.5 Load Commutated Choppers *265*
7.6 Linear dc Power Supplies *269*
7.7 DC-to-DC Converters without Isolation *272*
7.7.1 Buck or Forward Type *272*
7.7.2 Boost Type Converters *277*
7.7.3 Buck-boost Type *281*
7.7.4 Cuk Converters *284*
7.8 DC-to-DC Converters with Isolation *287*
7.8.1 Flyback Converters *287*
7.8.2 Forward Converters *291*
7.8.3 Push–Pull Converters *294*
7.8.4 Full-bridge Converters *295*
Summary *296*
Review Questions and Problems *297*

Chapter 8 Inverters 299–351

8.1 Introduction *299*
8.2 Classification of Inverters *299*
8.2.1 Current-source Inverters (CSI) *300*
8.2.2 Voltage-source Inverters (VSI) *300*
8.3 Classification of Thyristor-based Inverters *300*
8.4 Single-phase, Half-bridge, Voltage-source Inverters *301*
8.4.1 Resistive Loads *301*
8.4.2 *RL* Loads *302*
8.4.3 *RC* Loads *304*
8.5 Single-phase, Full-bridge Inverters *306*

8.6 Performance Parameters of Inverters *307*
8.7 Performance of Square-wave Inverters *308*
8.8 Pulse-width Modulated Inverters *310*
8.8.1 Single Pulse-width Modulation *311*
8.8.2 Uniform Pulse-width Modulation *313*
8.8.3 Sinusoidal Pulse-width Modulation *314*
8.9 Principle of Operation of Three-phase Inverters *318*
8.9.1 180°-conductor Mode *318*
8.9.2 120°-conductor Mode *322*
8.9.3 Comparison of 180°- and 120°-conduction Schemes *326*
8.10 Current Source Inverters *326*
8.11 Forced Commutated Thyrister-based Inverters *330*
8.11.1 Modified McMurray Inverter *330*
8.11.2 McMurray–Bedford Inverter *333*
8.12 Voltage Control of Inverters *337*
8.12.1 Control of Input dc Voltage *337*
8.12.2 External Control of ac Output Voltage *338*
8.12.3 Internal Control of Inverters *339*
Summary 349
Review Questions and Problems 349

Chapter 9 Resonant Converters 352–388

9.1 Introduction *352*
9.2 Principle of Resonant Converter Circuits *355*
9.2.1 Series Resonant Circuits *355*
9.2.2 Parallel Resonant Circuits *360*
9.2.3 Parallel-loaded Resonant *LC* Converters *362*
9.3 Classification of Resonant Converters *362*
9.3.1 Self-commutating or Load Resonating Converters *362*
9.3.2 Resonant-switch Converters *371*
9.3.3 Resonant dc Link Converters *382*
9.3.4 Resonant ac Link Converters *386*
Summary 387
Review Questions and Problems 387

Chapter 10 UPS and SMPS 389–409

10.1 Introduction *389*
10.2 Disturbances in Commercial Power Supply *390*
10.2.1 Types of Disturbances *390*
10.2.2 Power Quality and Power Conditioners *392*
10.3 Uninterrupted Power Supplies (UPS) *396*
10.3.1 Off-line, Preferred UPS *397*
10.3.2 Off-line, Interactive UPS *398*
10.3.3 On-line, Preferred UPS *399*
10.4 Storage Batteries *399*
10.5 Switched-mode Power Supplies (SMPS) *402*
10.6 Power Factor Correctors *405*
10.7 High-power PWM Audio Amplifiers *408*
Summary 409
Review Questions and Problems 409

Chapter 11 Device Protection and Magnetic Circuits 410–440

11.1 Introduction *410*
11.2 Protection of Devices *411*
11.2.1 Over-current Protection *411*
11.2.2 Over-voltage Protection *413*
11.2.3 Crowbar Protection Circuits *413*
11.2.4 Noise Protection *414*
11.3 Thermal Protection and Heat Sinks *415*
11.4 Cooling of Devices *415*
11.4.1 Heat Flow by Conduction *416*
11.4.2 Thermal Compounds and Insulators *417*
11.4.3 Transient Thermal Impedance *421*
11.4.4 Heat Flow by Convection *424*
11.4.5 Heat Flow by Radiation *425*
11.5 Procedure of Heat Sink Design *426*
11.6 Magnetic Materials *427*
11.6.1 Ideal or Perfect Permeability *428*
11.6.2 Soft Magnetic Materials *428*
11.6.3 Magnetically Hard Materials *429*
11.6.4 Constant Permeability Materials *429*
11.6.5 Complex and/or Nonlinear Permeability Materials *429*
11.6.6 Accurate Characteristics Materials *429*
11.7 Magnetic Circuits *429*
11.7.1 Electrical Analog of Magnetic Circuits *431*
11.7.2 Magnetic Circuit Calculation *432*
11.7.3 Calculation of Inductance *433*
11.7.4 Inductors with an Air Gap *434*
11.7.5 Effect of Leakage *434*
11.7.6 Energy Storage *435*
Summary 439
Review Questions and Problems 439

Chapter 12 Simulation of Power Electronic Converters 441–454

12.1 Introduction *441*
12.2 Importance of Simulation *441*
12.2.1 Benefits of Computer-aided Simulation *442*
12.2.2 Demerits of Computer-aided Simulation *442*
12.3 What is Simulation? *443*
12.4 Simulation Tools *444*
12.5 Some Examples *448*
12.5.1 Analysis of a Full-bridge Rectifier *448*
12.5.2 Analysis of a Buck Converter *449*
12.5.3 Dynamic Stability Analysis of a Buck Converter *451*
12.5.4 Analysis of a Half-bridge SMPS Topology *452*
Summary 454
Review Questions and Problems 454

Appendix ***455–476***
Bibliography ***477–478***
Answers ***479–481***
Index ***483–492***

Preface

The invention of silicon-controlled rectifiers (SCR), in 1957, and subsequent development in devices of their family—thyristors—have created a new branch of Electrical Engineering, i.e. Power Electronics. Its application covers all branches of Electrical Engineering. The rating and applications of power electronics converters vary over wide range—from few milli-watt toy motors to several hundred mega-watt HVDC systems. Extremely high efficiency (of the order of 99%) and flexibility of control (automatic and fast) are main merits of power electronic controllers. It is estimated that, in future, either at generation and transmission stage or utilization stage, the generated power will flow through the power electronic converters.

Now, Power Electronics has become an essential curriculum of undergraduate courses both in Electrical and Electronics Engineering. Moreover, it is also an essential part of Mechatronics.

This book, intended to be used as a textbook for the courses on Power Electronics—spanning over two semesters of the undergraduate course. In addition to that a one-semester course, comprising of selected chapters can also be set at postgraduate level. The chapters containing analysis and simulation of converters are useful for students and R&D design engineers alike.

In case of one-semester course, Chapters 1–7 will be enough to provide a strong background of the subject. The book also covers the practical aspects of the subject while theory is being discussed. Illustrative examples, relevant problems and computer programs are also given with the text, wherever necessary. Switching mechanisms of different converters are illustrated and discussed in detail. Analysis of converters, which is an important aspect to evaluate their performance, is provided throughout the text.

Chapter 1 is meant to highlight the background and utiltiy of power electronics. Chapters 2–4 provide the details of the power semiconductor devices, their characteristics and ways to use these devices as a switch. It also covers practical aspects of realizing an actual power electronic circuit. Phase-controlled switching circuits are discussed in Chapters 5 and 6. It is the pioneer control approach that was utilized to control the output ac or dc voltage. Apart from extensive harmonic analysis of converters, relevant problems and computer programs are given. Pulse-width modulation (PWM) based dc-to-dc and dc-to-ac converters are discussed in Chapters 7 and 8. Chapter 9 deals with resonant dc-to-dc and dc-to-ac converters, where LC resonant circuits with PWM control are utilized to improve the performance of converters. Chapter 10 highlights the disturbances in power supply and their remedy. It includes uninterruptible power supplies (UPS) and switched-mode power supplies (SMPS). Chapter 11 provides the general information about the thermal protection and magnetic components. It covers the fundamental aspect of heat sinks—an integral part of the device assembly. This chapter also deals with magnetic circuits and their design aspects. Chapter 12 shows how to simulate power electronic converters using standard

packages available (e.g. PSPICE, ELECTRONICSWORKBENCH). It gives a real-world exposure and deals with practical design aspects.

Appendix covers general aspects of circuits frequently used in power electronic converters. Moreover, different types of software packages, modules, converters and relevant information of devices are also incorporated.

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M.S. JAMIL ASGHAR

1

Introduction to Power Electronics

1.1 INTRODUCTION

A consumer needs electric power according to his requirements. The nature of the requirements may vary from time to time and from consumer to consumer, e.g. ac or dc, fixed or adjustable frequency, low frequency or high frequency, low voltage or high voltage, fixed or adjustable voltage, etc. However, in general, electric power utility systems (or any electrical power company) supply power at a fixed voltage and fixed mains frequency (50 or 60 Hz). The power may also be supplied from a non-conventional energy source (e.g. solar, wind, tidal, geo-thermal, micro-hydroelectric, etc.). These sources, in general, cannot maintain a constant supply of electric power due to variation in the input energy of these sources (e.g. variation in solar insulation or light intensity, variation in wind speed, etc.). The consumers, therefore, require power modulating systems which act as interfaces between the power utility system and the consumer's load. This power modulating system is a power electronic system or controller (Fig. 1.1). It modulates the electric power at a very high efficiency (highest of any other type of controller, e.g. mechanical, pneumatic, etc.) to generate or supply the required voltage, current, frequency, power, etc.

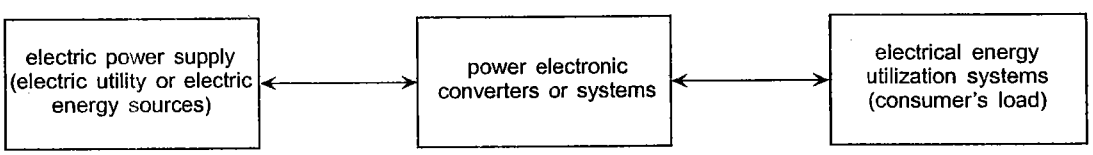


Figure 1.1 A general power electronic system configuration.

Power electronics is a branch of electrical engineering, which is related with an efficient conversion and a flexible control of electrical power for various applications. A variety of power semiconductor devices are used for this purpose. Moreover, the need of conservation of energy has

made it mandatory that energy in all the systems be utilized efficiently. Power electronic systems offer the most cost-effective mean of achieving this goal. Basically, power electronics deals with conversion/control of electric power by wave-shaping of voltage, current or both using fast switching, power-semiconductor devices. The control techniques require the switching-on and switching-off of these devices. Low-cost electronic circuits, consisting of integrated circuits and discrete components, are used to generate control signals which ultimately control these power semiconductor devices.

Earlier it was suggested that the power electronics embraces three disciplines, namely, Power, Electronics and Control. However, nowadays there is a tremendous deployment of digital control logic circuits, programmable logic controllers (PLCs), digital signal processors (DSPs), microprocessor/microcomputer or personal computer (PC) in power electronic controllers. Moreover, sometimes sensing and protective devices are also incorporated with power semiconductor device modules. Power electronics, therefore, can be considered to have several additional building blocks, as shown in Fig. 1.2.

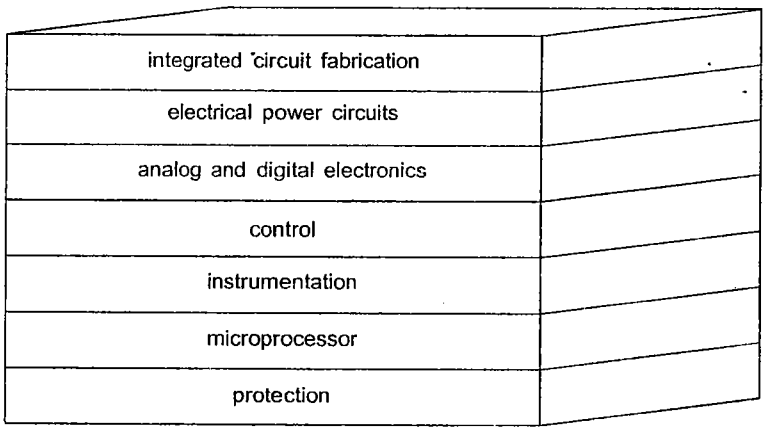


Figure 1.2 Building blocks of modern power electronics.

Moreover, there are several other disciplines too, which are associated with power electronics, namely, (a) circuit theory, (b) solid-state physics, (c) instrumentation & measurement, (d) signal processing, (e) electro-magnetics, (f) computation & simulation, (g) electric machines, (h) power systems, (i) electric energy utilization, (j) traction and (k) non-conventional energy sources. This shows interdisciplinary nature of power electronics. It is interesting to note that this covers almost all the disciplines of electrical engineering.

There has been a significant expansion in the market for power electronic controllers ranging from a few watts to several hundred megawatts, e.g. domestic lighting, air-conditioning, computers, UPS, variable-speed motor drives for compressor and pumps in process control, servo drives in robots for industrial automation, traction control of electrical vehicles, HVDC transmission, aircraft/satellite/space-shuttle power supply, etc.

Keeping in view the present trend of energy conservation, energy exploration and environmental pollution, enormous growth of this field and overwhelming application of power electronic controllers are expected in near future.

1.2

SCOPE AND APPLICATIONS

As discussed earlier, the power electronic converters/controllers have a wide range of applications. These controllers have an edge over other types of controllers (e.g. hydraulic/pneumatic, mechanical, etc.) in respect to the following aspects:

(a) *Efficiency:* The efficiency of a power electronic converter is very high (of the order of 90%). Sometimes, it is as high as 99%. It, therefore, results in low loss in controller circuits.
(b) *Compactness:* Power electronic controllers are lighter in weight and occupy less space.
(c) *Ease and speed:* Power electronic controllers are very fast in comparison to other controllers (mechanical or pneumatic). Moreover, automatic controls with complicated/ sophisticated control strategies are easily accomplished.
(d) *Reliability:* Probability of failure is low and life is longer in case of power electronic controllers as compared to their counterparts.

Power Electronic Applications

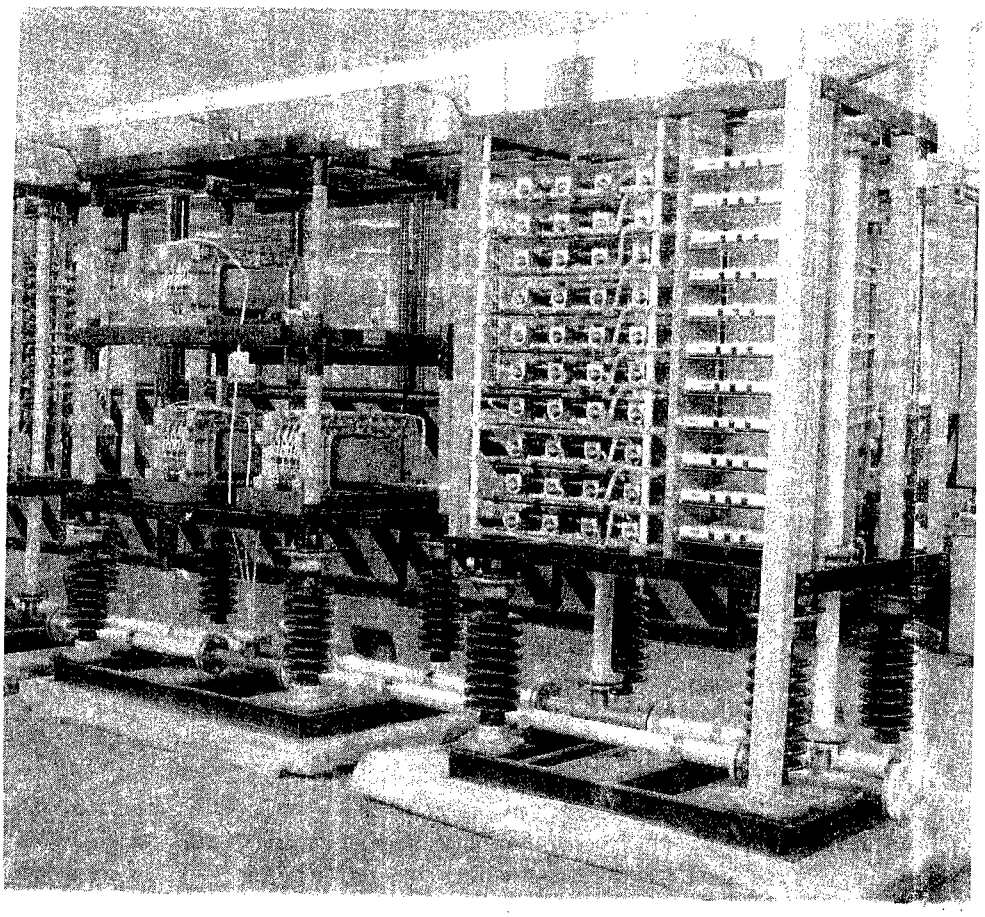
Various avenues of application of power electronics are mentioned below:

(a) *Lighting:* Light dimmer, light flasher, ballast circuit and high frequency converters for fluorescent tubes, fluorescent lamps and compact fluorescent lamps (CFL), display copiers, flash light, photographic processors, food warmer trays, traffic signal controls, night-vision equipments, electronic toys.
(b) *Heating/cooling:* Room heaters, electric blankets, electric dryers, electronic ignition of automobiles, furnaces, heat controllers, temperature controllers, microwave heating/ ovens, hot plates, resistance heating ovens (domestic ovens), resistance heating furnaces, electric arc furnaces, electron bombardment heating, high frequency heating (eddy current heating and dielectric heating), oven controls, air-conditioners, deep freezers and refrigerators.
(c) *Welding:* Electric-arc welding, electric-resistance welding, electron-beam welding.
(d) *Power supplies:* General ac to dc power supply, switched mode power supply (SMPS), aircraft power supply, battery chargers, laser power supply, computer power supply, uninterrupted power supply (UPS), ac voltage regulators, regulated dc power supply, radar/sonar power supply, high-voltage power supply for electronic equipments and cathode-ray oscilloscopes (CRO), furnace power supply, power supply of audio/video systems, power supply of electroplating systems, solar power supply conditioners and maximum power controllers, solar power based systems, spacecraft and satellite power systems, power supply to cordless phones and other telecommunication equipment power supply (dc and UPS).
(e) *Speed control:* Fans, exhaust fans, room coolers, heat convectors, food blenders, grinders, blowers, disk drive of computers, boilers, cement kilns, steel rolling mills, pumps and compressors, air-conditioning and refrigeration plants, process industries, conveyers, cranes and hoists, electric vehicles (EV), elevators, door openers, hand power tools, drill machines, machine tools, electric and diesel traction (engines), ship

propulsion, rapid transit systems, mine winders, motor controls, motor drives, movie projectors, oil-well drilling gadgets, paper mills, textile mills, printing press, photo cameras, photostat/Xerox machines, servo systems (position control), gas turbines and synchronous-machine starting, vacuum cleaners, sewing machines, washing machines, water coolers, robots, trolley buses, metro or subway trains, rapid transit systems, wind energy source systems, and cloth dryers.

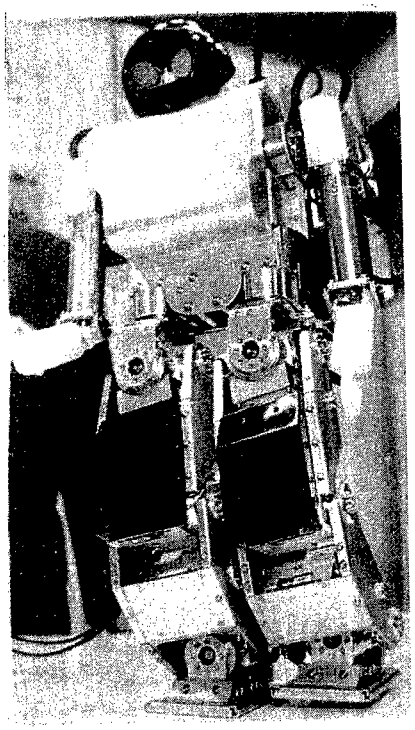
(f) *Miscellaneous:* High-power audio amplifiers, burglar alarms, tank water level controllers, chemical processing, electromagnets, electrostatic precipitators, particle accelerators, electronic toys, high-voltage dc (HVDC) system, flexible ac transmission system (FACTS) controllers, high-power active filters, reactive power control, electrolysis (electroplating, etc.).

Figure 1.3 shows different types of power electronic controllers for different applications. Morever the following examples shall clearly demonstrate the nature of application and usefulness of power electronic controllers.

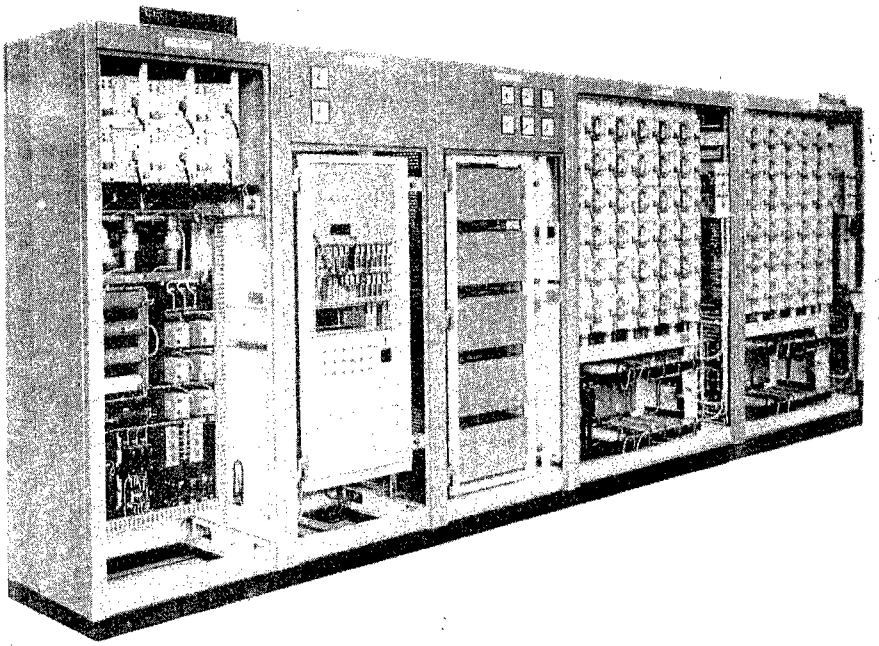


(a) A thyristor-based static VAR controller (SVC) (*Courtesy:* BHEL, Bangalore).

Figure 1.3 (*Cont.*)

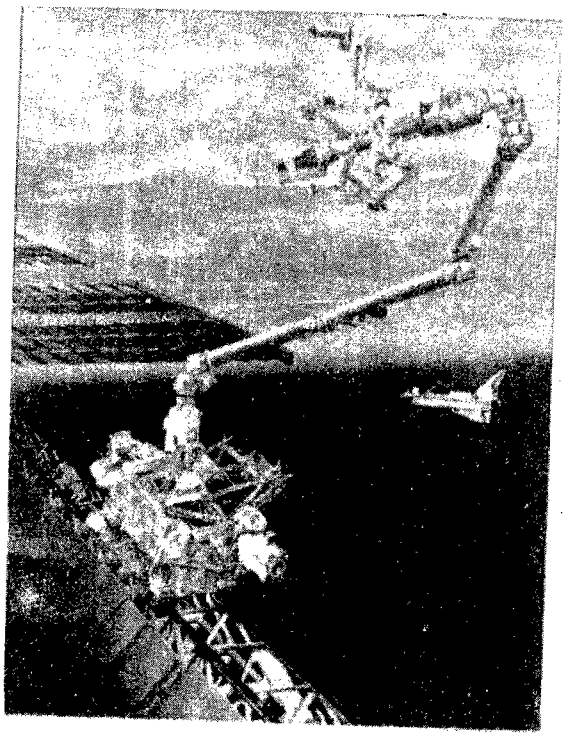


(b) A walking robot contains large number of power electronic controllers and converters.

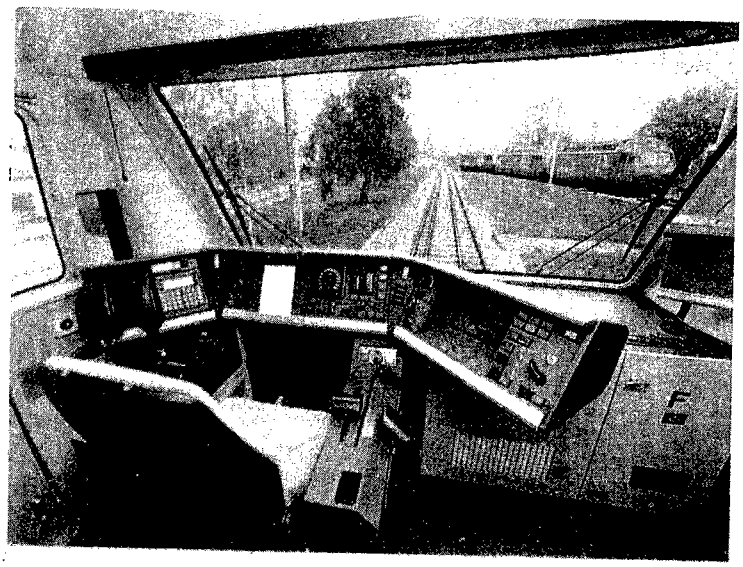


(c) A thyristor-based, three-phase, six-pulse, 50-Hz, 440-V, 3000-kW, full-bridge type, ac-to-dc converter (rectifier), used in mine-winder. (*Courtesy:* GEC, Australia).

Figure 1.3 (*Cont.*)



(d) Destiny space Laboratory with a 17.6-metre long robotic arm (canadarm2) and solar PV-based power supply. US space shuttle, Endeavour, can also be seen in the background. A large number of power electronic converters/controllers are used in each system.



(e) A GTO-based three-phase ac traction control system (MICAS-S2) for rail tractive units. (*Courtesy:* ABB Transportation Systems Ltd., Zurich, Switzerland).

Figure 1.3 Different power electronic controllers and their applications.

Example 1.1 A 90-W *general lighting service* (GLS) lamp, or incandescent filament bulb, is replaced by an equivalent *compact fluorescent lamp* (CFL) of the same light output (1050 lumen). A high-frequency (20 kHz) converter circuit is used for switching this CFL. The CFL and the converter circuit consume 18 W. The average life of a GLS bulb is 1000 h while the life of a CFL is 8000 h. The cost of each CFL including the converter circuit is Rs 200 and cost of the bulb is Rs 10. Estimate the savings, when the tariff of electric energy is @ Rs 2 per unit or kWh. Also, compare the power electronic circuit based CFL arrangement with the conventional lighting methods.

Solution We have

Life span of CFL = 8000 h

Energy consumption during this period = 18 W × 8000 h = 144 kWh

Cost of the electrical energy consumed (in CFL) = 144 × 2 = Rs 288

Total expenditure on CFL including its cost = 288 + 200 = Rs 488

Life of each GLS bulb = 1000 h

Energy consumption of GLS bulbs for the same period (i.e. in 8000 h) = 90 W × 8000 h = 720 kWh

Cost of the electrical energy consumed (in GLS bulb) = 720 × 2 = Rs 1440

Number of bulbs to be used in the same period (i.e. 8000 h) = 8

Total cost of the bulbs = 8 × 10 = Rs 80

Total expenditure on GLS bulbs including the power consumption = 1440 + 80 = Rs 1520

Total savings = (Total expenditure on bulbs) – (Total expenditure on CFL) = 1520 – 488 = Rs 1032

This is the saving in replacing one bulb with a CFL. Imagine the savings, if millions of filament type GLS bulbs being used are replaced by CFL. It shows the advantage of power electronic converters and systems (refer to Table 1.1).

Table 1.1 Comparison of CFL Arrangement with GLS Bulb and Mercury-vapour Tubelight

Comparison parameters	*Incandescent filament bulb (GLS bulb)*	*Tubelight (2 ft., mercury vapour tube) with choke only*	*CFL with power electronic converter circuit*
Power consumption (in watt)	90	42	18 (1/5 of the bulb)
Light (in lumen)	1050	940 (less than bulb/CFL)	1050 (same as bulb)
Cost (investment for one year)* (in Rs)	20 (2 bulbs)	150	200
Bill for one year* (in Rs)			
(365 days* or 1825 h)	328*	153*	66*
(365 days** or 4380 h)	787**	312**	158**
Annual savings/profit*	–	(i) 116% (328 – 153 = Rs 175)*	(i) 131% (328 – 66 = Rs 262)*
		(ii) 316% (787 – 312 = Rs 475)**	(ii) 314% (787 – 158 = Rs 629)**

(*cont.*)

Table 1.1 Comparison of CFL Arrangement with GLS Bulb and Mercury-vapour Tubelight (cont.)

Comparison parameters	*Incandescent filament bulb (GLS bulb)*	*Tubelight (2 ft., mercury vapour tube) with choke only*	*CFL with power electronic converter circuit*
Life span* (in days)	200	800	1600 (more than 4 yrs)
Total savings (in Rs)	–	768 (from 1 tube in 4000 h)	1152 (from 1 CFL in 8000 h)
Reliability (at variations of voltage)	Life reduces to a half, even at 5% higher voltage	Life of choke reduces (choke failure)	Do not fuse even at 20% higher voltage
Installation	Simple and quick	Neither simple, nor quick	Simple and quick

*5 h/day, tariff @ Rs 2.00/unit (for domestic use)
**12 h/day, tariff @ Rs 2.00/unit (for domestic use)
**8 h/day, tariff @ Rs 3.00/unit (for non-domestic use)
**6 h/day, tariff @ Rs 4.00/unit (for industrial 3-phase load).

Example 1.2 At lowest speed setting of a resistance regulator (130 rpm), a ceiling fan (1-phase induction motor) draws 52 W. When the resistance regulator is replaced by an ac phase-controlled switching circuit (power electronic controller), the fan draws 32 W for the same speed (Table 1.2). Find, (a) energy saving per year, when the fan operates 10 h/day under this condition for 150 days in a year, (b) power savings, if 10 million fans in India operate under this condition and (c) monetary savings, if one unit of electricity (1 kWh) costs Rs 2.

Solution We have

(a) Power savings due to the power electronic controller = 52 – 32 = 20 W
Energy savings per day = 20 W × 10 h = 0.2 kWh
Energy savings in 150 days per year = 0.2 × 150 = 30 kWh

(b) Power savings in 10 million fans = 30 × 10 × 10^6 W = 300 MW

(c) Monetary savings in 10^7 fans = 2 × 3 × 10^7 = Rs 600 million/year (Rs 60 crore/year)

Refer to Table 1.2

Table 1.2 Performance of a 1400-mm Sweep, 230-V, 270-rpm, 92-W (Input) Ceiling Fan When Controlled by Resistance Regulator and AC Phase Control (Power Electronic Converters)

Speed of fan (in rpm)	*Input power for resistance control (in watts)*	*Input power for ac phase control (in watts)*
115	52	32
160	66	48
185	73	58
230	86	78
270 (Rated speed)	92 (Resistance = 0)	92 (Switching angle = 0)

Example 1.3 A 1000-MW, double circuit, 3-phase ac transmission system is to be replaced by a HVDC transmission line with converter and inverter plants at the sending ends and receiving end, respectively. Compare the transmission capability of the HVDC system and the old ac system for the same transmission line. (*Note:* Consider the same percentage loss and the same insulation level for both the cases.)

Solution A three-phase double circuit ac line has six conductors, three for each phase-group (Fig. 1.4). Now in HVDC system, three conductors will be at $+(1/2)V_d$ voltage and remaining three at $-(1/2)V_d$. Therefore,

Power transmitted in 3-phase, double circuit, ac system = $2\,(3V_aI_a \cos \phi) = 6V_aI_a$

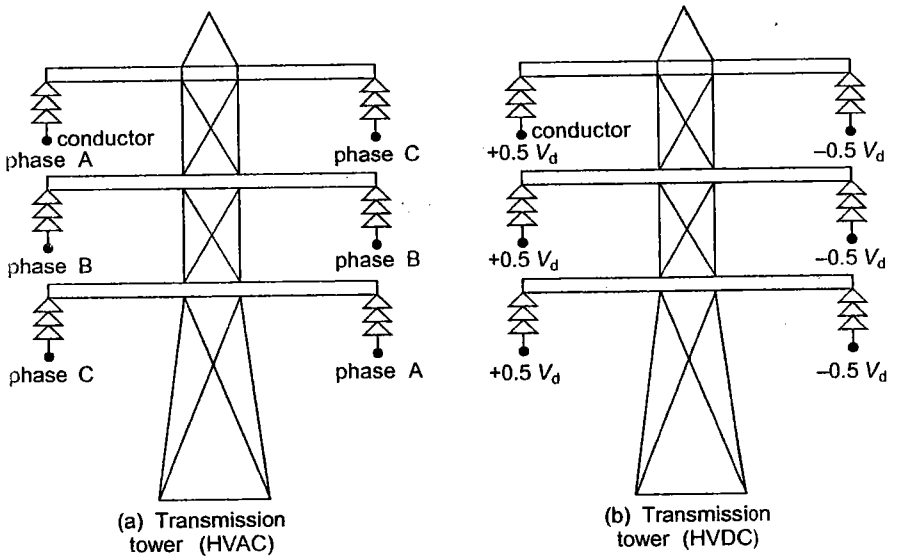


Figure 1.4 For comparision of ac and dc power transmission: (a) HVAC and (b) HVDC.

where V_a and I_a are per phase voltage and current of ac system. Line power-factor, $\cos \phi$, is assumed 1. Then power transmitted in HVDC is given by

$$3\left[-\frac{V_d}{2} - \left(-\frac{V_d}{2}\right)\right] I_d = 3V_dI_d$$

where V_d and I_d are dc voltage and dc current of HVDC transmission line, respectively. For equal insulation level, dc and peak ac voltages should be same with respect to ground potential. Therefore,

$$\frac{V_d}{2} = \text{Peak of } V_a = \sqrt{2}\, V_a \quad \text{or} \quad V_d = 2\sqrt{2}\, V_a$$

Neglecting the skin effect in the conductors with ac, the line loss in each conductor of resistance R is given by

$$I_a^2R = I_d^2R$$

For the same per unit losses,

$$\frac{\text{Loss in ac transmission}}{\text{ac power transmitted}} = \frac{\text{Loss in dc transmission}}{\text{dc power transmitted}}$$

Thus,

$$\frac{6I_a^2R}{6V_aI_a} = \frac{6I_d^2R}{3V_dI_d} = \frac{6I_d^2R}{3(2\sqrt{2}V_a)I_d}$$

or,

$$I_d = \sqrt{2}\, I_a$$

Ratio of dc and ac power transmitted is given by

$$\frac{\text{dc power transmitted}}{\text{ac power transmitted}} = \frac{3V_d I_d}{6V_a I_a} = \frac{3(2\sqrt{2}V_a)(\sqrt{2}I_a)}{6V_a I_a} = 2$$

Thus, the proposed HVDC line can transfer twice the power (2000 MW) of a three-phase, double-circuit ac system without any modification in the transmission line. However, terminal equipments, e.g. dc circuit breaker, converter and inverter plants will be needed. If the skin effect in ac conductors and lower power-factor of the ac line are also taken into account, the ratio of power transfer capability of HVDC will increase further.

1.3 EVOLUTION OF POWER ELECTRONICS

The history of power electronics is as old as ac systems. In the late nineteenth century, resonant circuits and dc-to-ac resonant-converters were proposed. In 1882, Jemin and Meneuvrier had recognized the behaviour of unidirectional current flow in arc (mercury–carbon electrodes). In 1890, Arons had developed the first vacuum (vapour) lamp. Subsequently thermo-ionic valves were developed in the beginning of the twentieth century. Mercury-arc rectifiers (glass envelope type), grid-controlled mercury-arc rectifier (high voltage, impulse firing type) and mercury-arc rectifier (metal envelope type) were marketed by Cooper–Hewitt in 1900, 1903 and 1908, respectively. Hot-cathode mercury-arc rectifier with grid control (thyratron) was developed by Langmuir in 1914. These valves were of two types. In the first type, a heated cathode was used to give a supply of electrons by thermal emission (vacuum or gas-filled rectifier diode). In the second type, a gas-filled triode was in the form of a mercury pool, inside the valve, provided to start emission (e.g. grid-controlled mercury-arc rectifier, high-power steel-tank water-cooled rectifier with rating up to 10 MW and 20 kV, ignitron, poly-phase rectifier, etc.). Vapour lamps were used for rectification (ac-to-dc conversion) and frequency conversion. In 1925, selenium rectifiers were developed. It was the first solid-state power device ever produced (without a glass tube). Subsequently, these devices were used in inverters, phase-controlled converters and cyclo-converters. In 1924, Dunoyer and Toulon successfully demonstrated regulation of the output dc voltage using a phase-control technique. In 1930, cyclo-converters (an adjustable frequency ac power supply from a fixed frequency ac source) was developed by Rissik. In 1933, Lenz used the ac voltage control switching technique for ac voltage regulator (using anti-parallel devices). The second breakthough was in 1948, due to the development of a semiconductor (Germanium) transistor. In 1953, 100-A Germanium power-diode was developed. A revolution in this field took place in 1956, due to the development of a four-layer silicon PNPN device, called *silicon controlled rectifier* or *thyristor* (SCR). The SCR resembles the characteristics of a grid-controlled mercury-arc rectifier (ignitron). Since ignition in the ignitron was controlled by a rod which was made of silicon-carbide or thyrite, SCR and other similar power semiconductor devices are also called *thyristors*. Figure 1.5(a) shows a 3-phase, 380-V, 4.4-kW, grid-controlled mercury-arc rectifier and a 800-V, 8-kW thyristor/SCR. It is evident that the thyristor is a compact device and

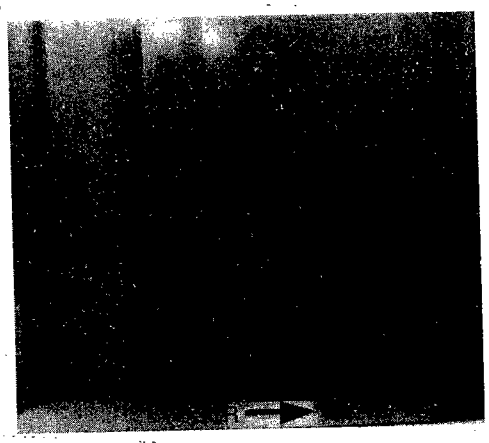
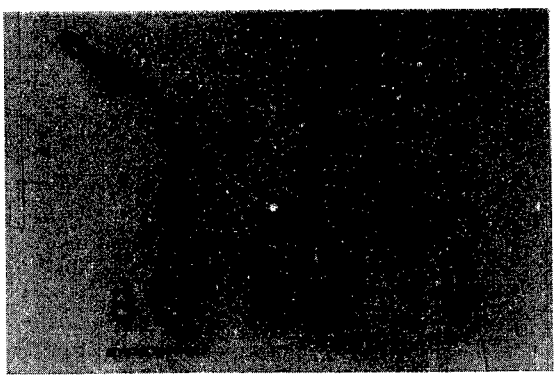


Figure 1.5(a) A grid-controlled rectifier and an SCR (at foreground-indicated by an arrow).

has higher power handling capability (compare the size of these devices). Since late 1980s, a large number of new devices are commercially available. These devices are highly efficient, fast, light-weight and have infinite number (times) of switching capability (unlike of electro-mechanical reed relays or contractor switches). This has opened a new era in power electronics and covers almost all the power related areas. Some of the leading manufacturers of power semiconductor devices are GE, Brown-Boveri, Toshiba Corp., Philips, International Rectifiers, Motorola Inc., Harris Corporation, National Semiconductors, Powerex Inc., Mitsubishi Electric, Siemens, Tokyo-Denki, etc. Figure 1.5(b) shows photographs of different commonly used power semiconductor devices. It is expected that within a decade about 60% power (in USA) will flow through these devices and eventually will extend to almost 100% in future. It is evident that there are perpetual research and development (R&D) activities in the field of power electronics. A large numbers of research journals are published and regular conferences are held worldwide related with power electronics.

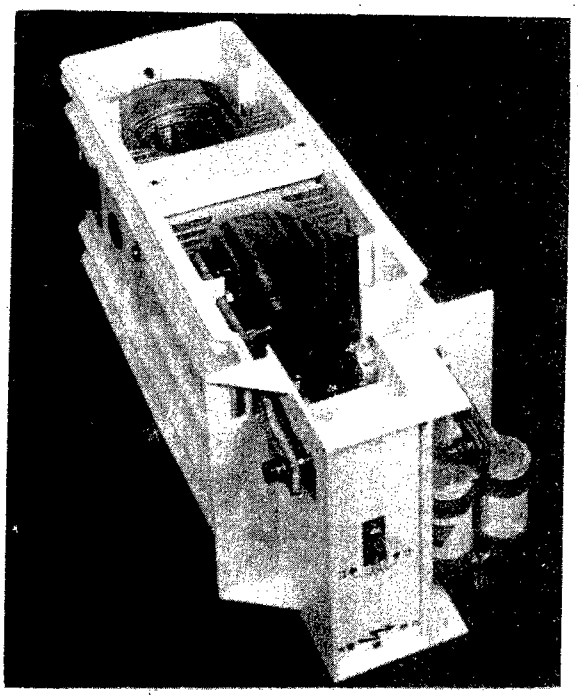


(i)

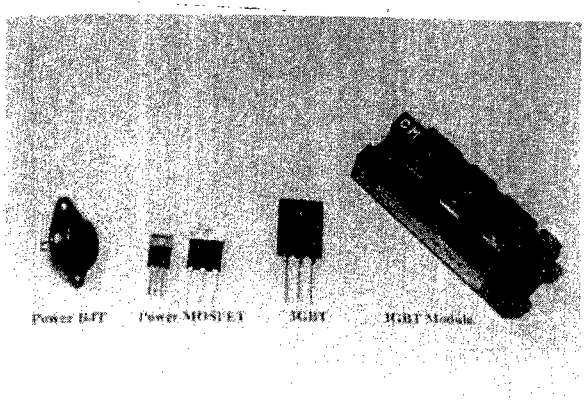
Figure 1.5(b) (*Cont.*)



(ii)



(iii)



(iv)

Figure 1.5(b) Power semiconductor devices: (i) diodes and thyristors, (ii) high-power LASCR, (iii) thyristor modules and (iv) gate-commutation devices and their modules.

Journals Lists of reputed international journals are as follows:

(a) From Institution of Electrical and Electronic Engineers Inc. (IEEE, USA)

1. *IEEE Transactions on Power Electronics*
2. *IEEE Transactions on Power Delivery*
3. *IEEE Transactions on Energy Conversion*
4. *IEEE Transactions on Industrial Electronics*
5. *IEEE Transactions on Industry Applications*
6. *IEEE Transactions on Circuit and System (part I)*
7. *IEEE Power Review.*

(b) Others

1. *Proceedings of Institution of Electrical Engineers*, UK (Proc. IEE)
2. *International Journal of Electronics*, UK
3. *Journal of European Power Electronics Society*, The Netherlands
4. *Journal of Machinery and Power Systems*, USA
5. *International Journal of Renewable Energy Engineering*, Australia.

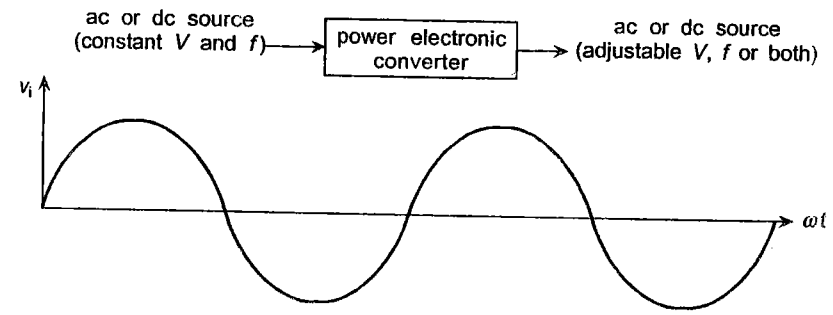
Conferences Following regular conferences are held every year (region-wise as well as country-wise):

1. Power Electronics Specialist Conference (PESC)
2. Applied Power Electronics Conference (APEC)
3. European Power Electronics Conference (EPEC)
4. IEEE Industrial Electronics Conference (IECON)
5. International Conference on Electrical Machines (ICEM)
6. International Conference on Power Conversion and Intelligent Motion (PCIM)
7. International Symposium on Power Electronics (ISPE)
8. International Conference on Power and Energy Systems (PES)
9. IEEE Workshop on Computers in Power Electronics (COMPEL)
10. International Conference on Power Electronics and Motion Control (PEMC)
11. International Telecommunication Energy Conference (INTELECT)
12. International Conference on Power Conversion and Intelligent Motion (PCIM)
13. IEEE International Power Electronics Congress (IPEC)
14. Regular Technical Meetings of IEEE Power Engineering Society (PES)
15. Annual Meeting of IEEE Industrial Applications Society (IAS)
16. IEEE International Conference on Power Electronics and Drive Systems (PEDS)
17. International Conference on Power Electronics, Machines and Drives (PEMD)

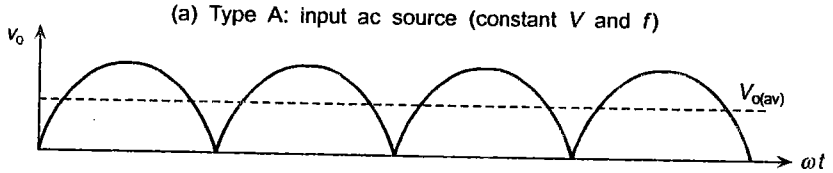
1.4

CLASSIFICATION OF POWER ELECTRONIC CONVERTERS

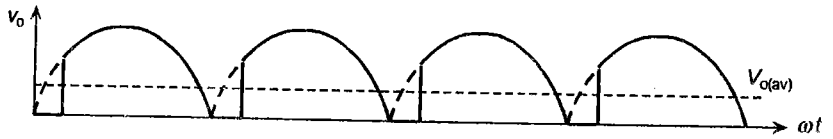
For the above mentioned applications, different types of controllers or converters are used. Power electric converters include rectifiers, inverters, ac regulators, choppers and cyclo-converters (Fig. 1.6).



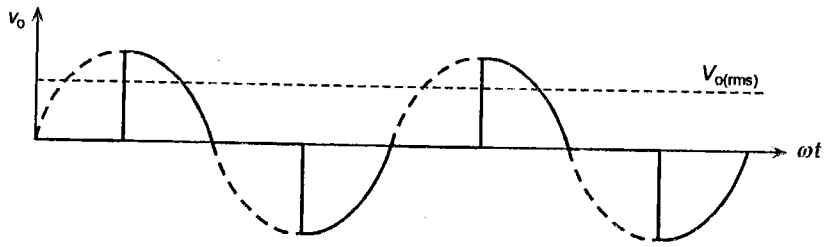
(a) Type A: input ac source (constant V and f)



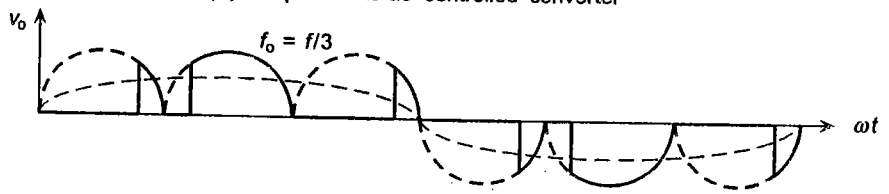
(i) Output: ac-to-dc uncontrolled rectifier converter



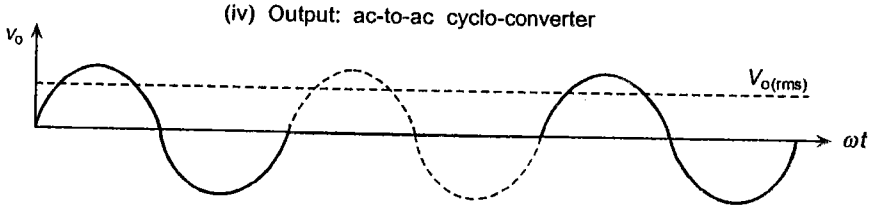
(ii) Output: ac-to-dc controlled rectifier converter



(iii) Output: ac-to-ac controlled converter

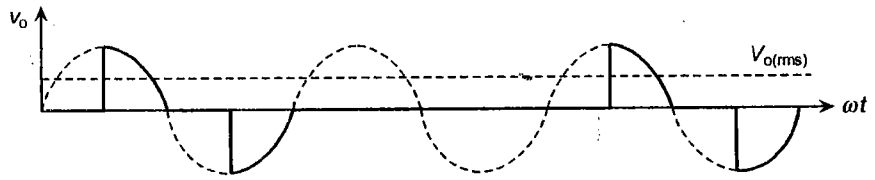


(iv) Output: ac-to-ac cyclo-converter

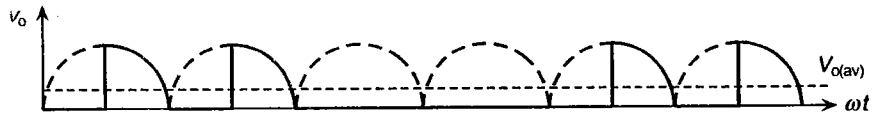


(v) Output: ac-to-ac integral cycle control

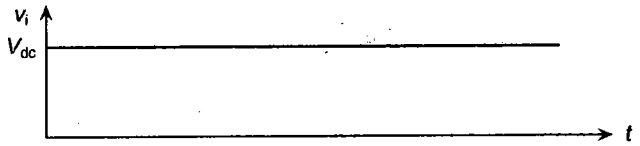
Figure 1.6 (*Cont.*)



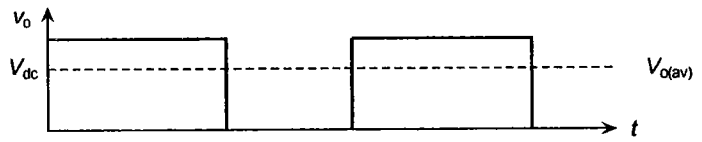
(vi) Output: ac-to-ac discontinous phase control



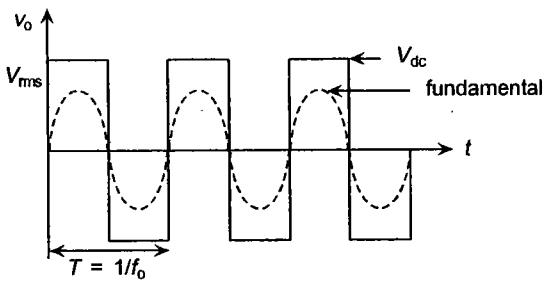
(vii) Output: ac-to-dc discontinous phase control



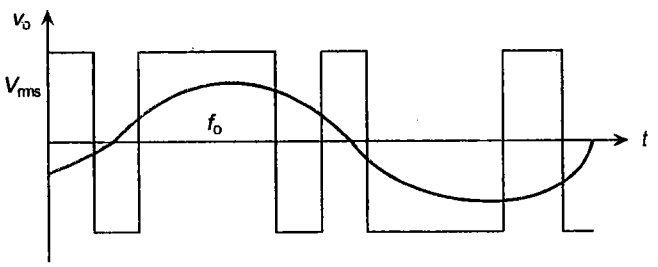
(b) Type B: input dc source (constant V)



(i) Output: dc-to-dc converter (dc chopper)



(ii) Output: inverter or dc-to-ac converter



(iii) Output: pulse-width modulated (PWM) inverter or dc-to-ac converter

Figure 1.6 Output waveforms of different power electronic converters.

They can be classified as follows:

1. *Uncontrolled rectifier (ac to dc):* For fixed dc output voltage from fixed ac input voltage.
2. *Controlled converter (ac to dc):* For adjustable output dc voltage from fixed ac input voltage.
3. *AC phase controlled switching or ac regulator (ac to ac):* For adjustable ac output voltage at the same frequency from a fixed ac input voltage.
4. *Cyclo-converter (ac to ac):* For adjustable output voltage at lower frequency from fixed ac input voltage.
5. *Integral cycle control (ac to ac and ac to dc):* For adjustable (in steps) output voltage by off/on control of input supply.
6. *Discontinuous phase-controlled switching (ac to ac and ac to dc):* Phase controlled switching combined with integral-cycle controlled switching to obtain the fine and the coarse (in steps) controls.
7. *Chopper or dc converter (dc to dc):* For adjustable output dc voltage from fixed dc input voltage.
8. *Inverter (dc to ac):* For variable frequency ac output voltage from dc input voltage.
9. *Pulse-width modulated inverter (dc to ac):* For adjustable output voltage and adjustable frequency from a dc input voltage.
10. *Resonant converter (dc to dc/ac):* For adjustable output dc/ac voltage and adjustable frequency.

1.5 REQUIREMENTS OF AN IDEAL SWITCHING DEVICE

The above-mentioned controllers are often combined to achieve new converter topologies. In fact, there are several thousand power electronic circuit topologies. These converters use different types of fast acting, highly efficient and highly reliable power semiconductor switches. For highly efficient power conversion an ideal switch is required. These switches act as an on/off switch and have only two states like digital circuits. When the switch is ideally on, there is no voltage-drop across the devices and the supply voltage reaches the load (load voltage is equal to the supply voltage) during this period. Similarly, when the device is off, ideally it offers infinite impedance between the supply and the load. Therefore, no current flows through the device and supply voltage does not reach the load. An ideal switch is required for the above-mentioned controllers to achieve a high efficiency. It is desirable that the switch should have the following properties:

1. *Large voltage and current ratings:* So that the device can handle large power.
2. *Zero on-state resistance:* The device carries a full-load current at on-state. It is desirable to reduce on-state power loss (I^2R). Thus at on-state, voltage drop across the device and power loss in it (I^2R) should be zero.
3. *Zero leakage current or infinite off-state impedance:* At off-state (blocking condition), the leakage current should be zero. The device behaves as an open switch. Then the power loss in the device is zero.
4. *Zero switching-time delay:* If a device turns on and off instantly (within no time), the switching loss in the device is zero.
5. *High temperature and radiation withstand capability:* Due to high temperature, there should not be any significant deviation in the characteristics of the device.

6. *Paralleling of devices:* In case of several devices in parallel, the current passing through each device should be same.
7. *Infinite life:* It should be rugged.

It is difficult to materialize the devices with these properties. However, gradual but continuous development is taking place towards this goal. It is found that silicon-based semiconductors are most suitable with respect to above mentioned criteria. The properties of silicon-based devices are listed as follows:

1. Reverse leakage current of silicon pn-junction is very low. Hence power loss at the off-state is low.
2. Avalanche breakdown voltage is high. It therefore can withstand higher blocking (reverse) voltage.
3. It can be operated at a higher temperature due to a large band gap (between valance band and conduction band in silicon).

Although, power devices being used are traditionally silicon based, but with the material growth and device technologies, majority carrier devices with large breakdown voltages are now fabricated using Groups III and V (of the periodic table) compound semiconductor materials. For example, a high-power gallium arsenide (GaAs) Schottky diode has reduced recovery time, high switching speed, almost zero forward recovery time and low on-state voltage as compared to its counterpart, silicon p-i-n power rectifier.

For high density power devices (with high power handling capability), the gate should be wide (for flow of current) and short (for fast transit of electron or current). The invention of gallium nitride (GaN) light-emitting diode (LED), in 1991, led the development of gallium nitride (GaN) based field-effect transistors (FET). It has shown the highest power density 10 W/mm and worked at 7.2 W/mm and 3.5 GHz frequency. Gallium arsenide (GaAs) transistors can handle 10 GHz but at a power density 1 W/mm only. Silicon germanium can operate even at higher frequency (above 10 GHz) but cannot handle high power. Moreover, silicon transistors stop working at about 140°C while GaN transistors are tested successfully even at 300°C. Thermal conductivity of GaN is seven times higher than GaAs. Moreover, GaN has a high breakdown field hence it has high frequency and high power handling capabilities. GaN has a breakdown field of about 3 MV/cm, as compared to 0.4 MV/cm for GaAs. General properties of various features of competitive semiconductor materials are given in Table 1.3.

Table 1.3 General Features of Commonly Used Semiconductor Materials

Semiconductors	*Bandgap (eV)*	*Electron mobility* (cm^2/Vi)	*Saturated electron velocity* ($\times 10^7$ cm/s)	*Breakdown field* (MV/cm)	*Thermal conductivity* (W/cm-K)	*Relative dielectric constant*
Silicon (Si)	1.1	1500	1.0 (peak 1.0)	0.3	1.5	11.8
Gallium arsenide (GaAs)	1.42	8500	1.3 (peak 2.1)	0.4	0.5	12.8
Silicon carbide (SiCa)	3.26	700	2.0 (peak 2.0)	3.0	4.5	10.0
Gallium nitride (GaN/AlGaN)	3.49	1000–2000	1.3 (peak 2.1)	3.0	71.5	9.0

1.6 IDEAL SWITCH

For an ideal switch, the device power loss (p_d) is zero because the device will offer zero resistance during on-state and infinite resistance during off-state. The voltage drop across the device (v_d) during on-state and the current through the device (i_d) during off-state shall be zero. Moreover, the transition period or switching period (t_s) is ideally zero, i.e. change of state from turn-on to turn-off and vice versa is instantaneous, as shown is Fig. 1.7. Thus the switching loss due to this changeover (off to on and vice versa) will also be zero.

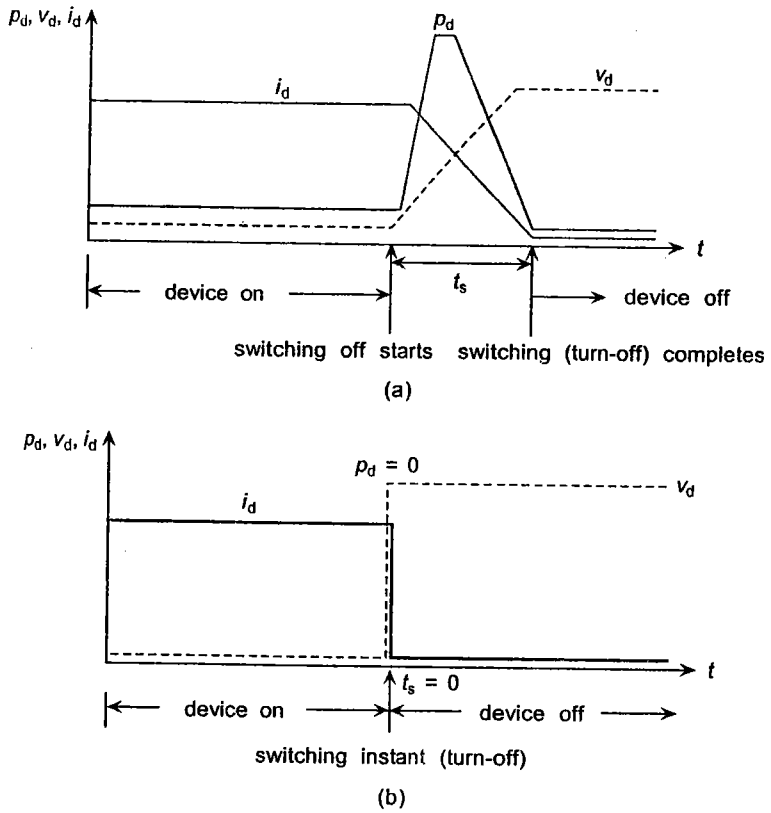


Figure 1.7 Switching power loss of (a) normal and (b) ideal power semiconductor devices.

1.7 CLASSIFICATION OF POWER ELECTRONIC DEVICES

For the above mentioned controllers, various power semiconductor devices are used as a switch to control (modulate) the power supply to the load. They constitute following three categories:

(a) Devices, whose both turn-on (or triggering) and turn-off depend upon the power circuit. For example, diodes—Schottky diode, fast-recovery diode and mains or line frequency diode, etc.

(b) Devices, whose turn-on depends upon trigger signal and blocking (or turn off) is controlled by power circuit. For example, various types of thyristors (SCR, ASCR, RCT, LASCR), triac, etc.

(c) Devices, whose both turn-on and turn-off are controlled by a gate signal. For example, power BJT, power MOSFET, GTO, IGBT, SIT, MCT, etc.

SUMMARY

The invention of thyristor (SCR) in 1956 introduced a new discipline in electrical engineering, i.e. power electronics. Subsequently, other power semiconductor devices had been developed (e.g. triac, GTO, bipolar power transistor, power MOSFET, IGBT, SIT, SITH and MCT, etc). Thus converter/controller circuits with wide applications have become possible. Static power switch, phase controlled ac-to-dc converter, dc-to-ac inverter, and switched-mode power supplies (SMPS) are commonly used equipments based on power semiconductor devices. They vary from a few watt toys and domestic appliances (e.g. cordless mobile phones) to hundreds of MW, HVDC transmission system and steel rolling mills. These controllers are compact, highly efficient and offer flexibility of control. It is expected that in this new millennium-century, the generated power will totally flow through these devices.

REVIEW QUESTIONS AND PROBLEMS

1. What is power electronics?
2. What are the main areas of application of power electronics?
3. What are the advantages of power electronic controllers?
4. What are different methods of voltage control including power electronic converters?
5. Mention various power semiconductor devices used in power electronic controllers.
6. What are the qualities of an ideal switching device?
7. How many types of converters can be used for ac-to-dc and dc-to-ac conversion?
8. "Power electronics is nothing but wave-shaping for an efficient power control". Justify this statement.
9. What is the future of power electronics?
10. A 6000-hp electric train with a conventional tape-hanging arrangement of speed control operates at 70% efficiency. If this controller is replaced by a power electronic converter with regenerative braking facilities (ac-to-dc dual converter), the efficiency increases to 90%. Estimate the energy saving in 10 h of journey.

2

Power Semiconductor Devices

2.1 INTRODUCTION

The power semiconductor devices are backbone of power electronic circuits and controllers. These devices work as a switch and low-power analog or digital circuits control them. When the device conducts, it behaves as an ordinary contactor-switch, which is closed. Therefore, ideally, no voltage drop appears across the device and the supply voltage reaches the load. Similarly, when the device does not conduct (off condition), it offers ideally an infinite impedance. The load circuit virtually gets disconnected and no load current flows from the source to the load.

The characteristics of these devices vary over wide range which are tailored according to the needs of consumers and to improve their performance.

2.2 CLASSIFICATION OF DEVICES

Basically, the power semiconductor devices can be classified into three groups according to the nature of their controllability:

(a) *Group I (Diode rectifiers):* A large number of devices belong to this category. Both on and off states of the devices are uncontrolled and depend upon the conditions of the power circuit. Therefore, both turn-on and turn-off conditions are not externally controllable.

(b) *Group II (Thyristors):* There are several types of thyristors. Most common among them is the silicon-controlled rectifier (SCR). In general, turn-on operation of the devices of this category is controllable using a trigger signal. However the turn-off operation depends upon the condition of the power circuit. Therefore, in this case, only turn-on switching is externally controllable.

(c) *Group III (Gate-commutation devices):* A large number of high switching frequency devices belong to this category. Both turn-on and turn-off operations of the device are controllable by gate or base signals. These conditions are independent of the power circuit conditions. Therefore, in this case, both turn-on and turn-off conditions are externally controllable.

2.3

DIODES (UNCONTROLLED RECTIFIERS)

The diode is the simplest bipolar static switching device. It has two layers of p and n materials. These layers form a junction called pn-junction. These layers are connected with ohmic contacts or terminals, called anode (A) and cathode (K), as shown in Fig. 2.1. A depletion layer or space charge layer (SCL) forms across the junction. The width of the SCL depends upon the applied voltage, temperature of the junction (T_j), and most importantly, the doping (or added impurity of these extrinsic layers). The carrier concentration of intrinsic (pure) silicon is small (1.4×10^{10} atoms per cubic centimetre), while it is as high as 10^{20} atoms per cubic centimetre for a doped silicon in the diode.

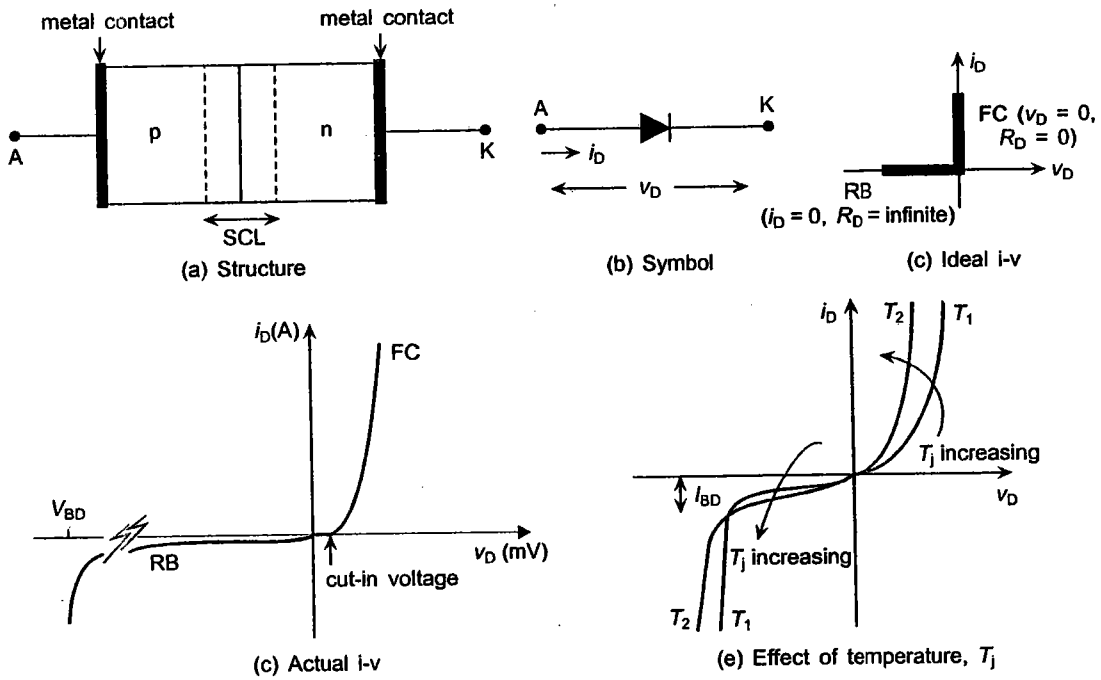


Figure 2.1 A small-signal pn-junction diode.

It conducts and offers ideally zero forward resistance whenever the anode terminal is at higher potential than the cathode (Fig. 2.1). The diode is called *forward biased* and it conducts. During this *forward conduction* (FC) condition, both layers are flooded with carriers. Both the layers, therefore, lose their semiconductor characteristics and behave as a conductor connecting both anode and cathode terminals like a closed contactor-switch. A very small voltage drop (v_D) appears across the diode at FC condition (which is ideally zero). A conducting diode can be turned off by the application of a reverse voltage (i.e. when the anode is at a lower potential than cathode). However, the diode turns off successfully only when the current through it (i_D), reduces to zero. At this condition, the diode is called *reverse-biased* (RB). The reverse voltage causes a

reverse current through the diode and the resultant current (i_D) becomes very small. A negative current then flows that neutralizes the carriers flowing through the device (Fig. 2.2). Ultimately, i_D becomes almost zero and commutation (turn-off) accomplishes. The diode behaves as a contactor-switch with open contacts. Ideally zero and practically very small leakage current flows at this condition. This current is called *reverse-leakage* current and the diode is said to be in *reverse-blocking* (RB) condition. At turn-off, the diode current reverses for a period called *reverse-recovery time* (t_{rr}), before falling to almost zero level. The carriers recombine with the opposite charges during t_{rr}, to get neutralized, as shown in Fig. 2.2. Figure 2.1 shows the static i-v characteristics of a diode. The characteristic is temperature dependent and the diode current can be found with the help of the equation given below:

$$i_D = I_o\left[\exp\left(-\frac{qV_D}{KT_j}\right) - 1\right] = I_o\left[\exp\left(-1.15942\frac{V_D}{T_j}\right) - 1\right] \quad (2.1)$$

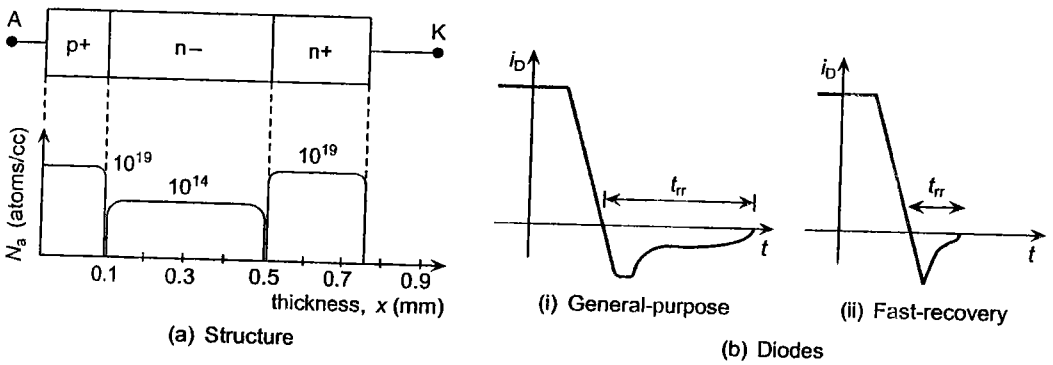


Figure 2.2 Power diode: turn-off switching characteristics.

Here I_o is the reverse leakage current in ampere, q is the electric charge (1.6×10^{-19} coulomb), T_j is junction temperature in kelvin and K is Boltzmann's constant (1.38×10^{-23} joules/K).

The effect of T_j on static i-v characteristics is shown in Fig. 2.1e. There are several types of pn-junction devices described in the further sections. They are evolved to improve both static and dynamic properties of the device.

2.3.1 General-purpose Power Diodes

The performance and structure of power diodes are different from that of small-signal diodes. In fact, power-diodes have to handle high current, high voltage and high power circuits. It consists of an additional lightly doped n– epitaxial layer (drift region) that absorbs SCL or depletion layer formed due to the application of reverse blocking voltage (Fig. 2.2a). The thickness of this layer is adjustable and it depends upon the required reverse or blocking-voltage withstand capability of the power diode. The impurity concentration (N_a or number of impurity or doping atoms per cubic centimetre) varies from layer to layer. When a power diode handles power at the main frequency (50 or 60 Hz) or low-frequency below 1 kHz, it is called a *general-purpose* power diode or *mains* diode. According to their characteristics, they are used for various power electronic applications. Its on-state voltage drop is

kept as low as possible at the cost of turn-off switching time (Fig. 2.2b). For this purpose, doping level is increased. Thus the reverse-recovery time becomes larger (more than 25 μsec), which is acceptable in line-frequency (50 or 60 Hz) or low frequency circuits up to 1 kHz.

The higher rating of the commercially available device is up to 10 kV and 5 kA.

2.3.2 Schottky Power Diodes

It is a high-speed, low forward-voltage drop (< 1 V) and high reverse leakage current device with high temperature-withstand capability. It is formed by metal (e.g. platinum) in homogeneous contact with n-type silicon substrate and a potential barrier forms with a very thin SCL. Unlike a pn diode, it is a majority carrier device. During forward biased condition, electrons from n-layer overcome the barrier potential and reaches the positive potential metal. A large reverse-leakage current flows due to minority carrier in reverse-biased condition. It can withstand higher junction temperature (175°C) in comparison to other types of diodes.

The higher rating of the commercially available device is up to 400 V and 300 A.

2.3.3 Fast-recovery Power Diodes

It is used in high-frequency circuits, where general-purpose power diodes cannot be used due to large t_{rr} as shown in Fig. 2.2b. Their recovery time is in the range of 25–100 ns. Thus, it is used in inverters, choppers, switched-mode power supply (SMPS), uninterrupted power supply (UPS), dc-to-dc converters, resonant converters, etc., where fast switching is done by inverter-grade SCR, GTO, BJT, MOSFET, IGBT, etc. A highly doped p type and n^+ type layers are sandwitched by a lightly doped n^- layer.

The thickness of the n^- silicon diode is increased for higher voltage rating. For fast switching, reverse-recovery time is minimised by reducing stored charge in neutral region and by minimizing carrier life time. Recombination centres are formed by adding gold in neutral region.

For high frequency applications and to improve the switching performance, p-i-n diodes are used. In case of a p-i-n diode, an intrinsic semiconductor layer (i-region) is sandwiched between p and n layer such that overall thickness of the wafer reduces. Due to the high resistivity of the i-layer, SCL and most of the reverse-bias voltage appears across this region.

The higher rating of the commercially available device is up to 3 kV and 1 kA (with $t_{rr} < 5$ μs).

2.3.4 Power Zener Diodes

It is extensively used as a voltage-reference source and a voltage clamp. The reverse-breakover voltage or breakdown voltage (V_z) is used as clamping-voltage level. A transient-suppressing Zener diode can absorb power up to 75 W with a heat sink. It is a fast, compact and most useful transient-voltage suppressor. Its performance is better than snubber circuit which is slow to respond. Its response time is few nanosecond and it can absorb peak instantaneous (transient) power as high as 50 kW. It can be connected in back-to-back mode for clamping high voltage-transient or spikes of both polarity (positive as well as negative). Similarly, for higher voltage applications, several diodes can be connected in series.

The range of the commercially available device is 1.8 V to 300 V and 0.25 W to 75 W.

2.3.5 Thyrectors or Metal-oxide Varistors (MOV)

This is also used as a transient voltage suppressor. It is a fast, compact device and has high energy-handling capability. It is a ceramic, bipolar, non-linear semiconductor, whose characteristic is similar to a pn-junction Zener or avalanche diode (polarized type MOV). It is made of zinc-oxide (90%) and oxide of bismuth, cobalt or manganese. A fine layer of this combination (mixture) is put in between metal contact plates (like a parallel-plate capacitor). The structure of the device develops a high terminal capacitance which limits its application at high frequency due to large charging current. The function of a non-polarized MOV is similar to two back-to-back connected Zener diodes (Fig. 2.3). The pn-junction of the device offers very high impedance at low voltage and provides a non-linear very low resistance at high voltage. The comparative performance of these devices can be understood with the help of Fig. 2.4. The device failure rate increases with increase in applied voltage. The voltage-temperature-coefficient is –0.05% per K, i.e. the breakover voltage (V_{BO}) decreases at higher temperature. The mean-time-before-failure (MTBF) is better for lower temperature (7×10^8 hours for the junction temperature below 40°C).

The rating of the device varies from a few volts to several kV.

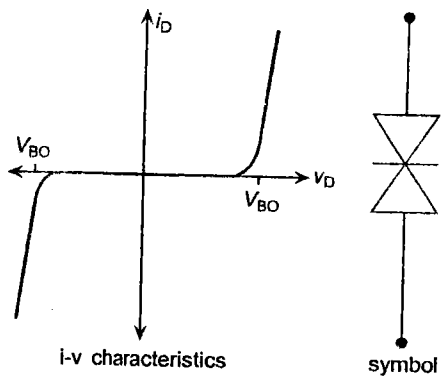


Figure 2.3 Symbol and i-v characteristics of a non-polarized MOV.

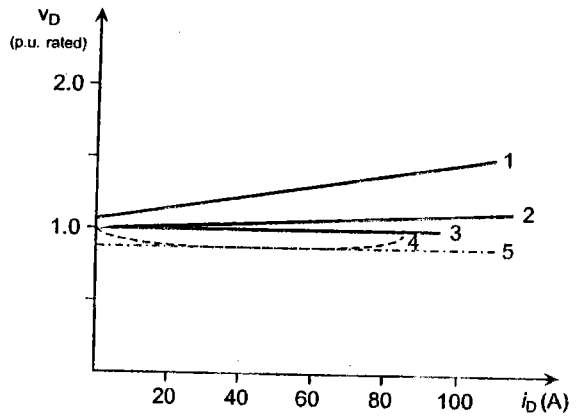
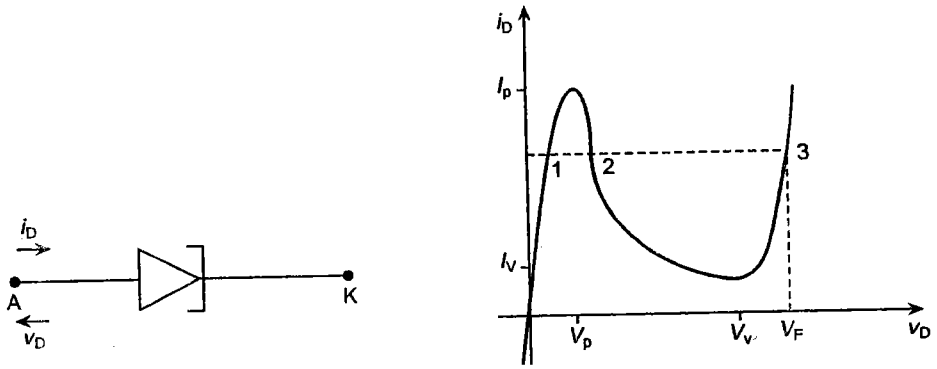


Figure 2.4 Comparison of voltage suppressor devices: silicon carbide varistor (1), selenium varistor (2), modern zinc-oxide varistor (3), power Zenor diode (4) and ideal clamp level (5).

2.3.6 Tunnel Diodes

A general-purpose, pn-junction diode has an impurity concentration of about 1 part in 10^8 and depletion layer of about 1 micron. If impurity is increased greatly (1 part in 10^3), the device characteristic changes completely. The width of the depletion layer reduces to 0.01 micron as the width is inversely proportional to the impurity concentration. For such a thin barrier (depletion layer), according to Schrodinger-wave equation of quantum mechanics, there is a large probability that an electron will penetrate through the barrier. This phenomenon is called *tunneling*. Thus, a high-impurity density pn-junction device is called *tunnel diode*. Figure 2.5 shows static i-v characteristics of the device. In reverse (or reverse biased) condition, it behaves as an excellent conductor. After the peak current (I_p), it has negative-resistance characteristics up to the valley point. From the reverse-biased characteristics to the valley point, the device characteristic is dominated by



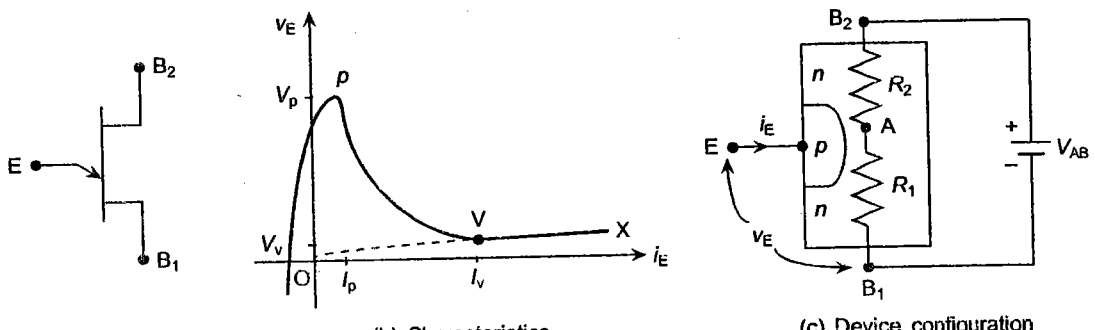
(a) Symbol (b) Characteristics

Figure 2.5 Tunnel diode.

the *tunneling effect*. Later, the normal characteristics of a pn-junction dominate. Due to the peculiar i-v characteristics, a particular magnitude of each current can be obtained at three different voltages between peak and valley points. It is used for very high frequency switching applications, e.g. high frequency oscillator. The switching period is of the order of a nanosecond. They are normally made from germanium arsenide (GeAs) or gallium arsenide (GaAs), which give better current range. The ratio I_p/I_v for germanium, gallium and silicon are 15, 8 and 3.5, respectively.

2.3.7 Unijunction Transistor (UJT)

The UJT is an auxiliary semiconductor device. Normally, it is used to trigger a thyristor. It is a three-terminal, two-layer and one pn-junction device. It shows a high stability over temperature and supply voltage variations. It has n-type silicon based semiconductor between base terminals B_1 and B_2 and a p-type (emitter) is alloyed between B_1 and B_2 (Fig. 2.6c). R_1 and R_2 are resistances of the two parts of semiconductor base material (n-type). When B_2 is positively biased, the potential at A will be ηV_{BB}, where, $\eta = R_1/(R_1 + R_2)$ and η is called *intrinsic stand-off ratio* (which is always less than 1). When $v_E < \eta V_{BB}$, the pn-junction remains reverse-biased and a negligibly small reverse leakage current flows, as shown in Fig. 2.6b. As soon as v_E becomes higher than ηV_{BB} (and equal to ηV_{BB} +



(a) Symbol (b) Characteristics (c) Device configuration

Figure 2.6 Unijunction transistor.

V_D, where V_D is forward voltage drop of the diode), the junction becomes forward biased. This is the peak-point of the device characteristics (V_p, I_p). The emitter-base (B_1) junction begins to conduct. As the carriers in the bottom region (R_1) increases, the resistance R_1 collapses and i_E increases further with decrease of v_E. Thus the device exhibits a negative resistance region till valley point (V_v, I_v) on the v-i characteristics. At the valley point, the entire base B_1 region is saturated. Therefore, the voltage drop does not decrease further. If v_E is increased, v-i characteristic (VX part) is similar to that of a pn-junction diode in forward conducting condition (shown by OVX curve).

2.3.8 DIACS

The *diac* is an auxiliary semiconductor device which is normally used to trigger a thyristor (triac). It is a two-terminal, four-layer, *pnpn*, bilateral-switching device. It behaves like a triac and conducts in both the directions, without a gate signal. When a voltage applied between MT_1 and MT_2, exceeds the breakdown or breakover voltage (V_{BO}), conduction of the device takes place. However, unlike other thyristors, the V_{BO} is a few tens of volts, as shown in Fig. 2.7. A typical V_{BO} varies from 25 V to 35 V.

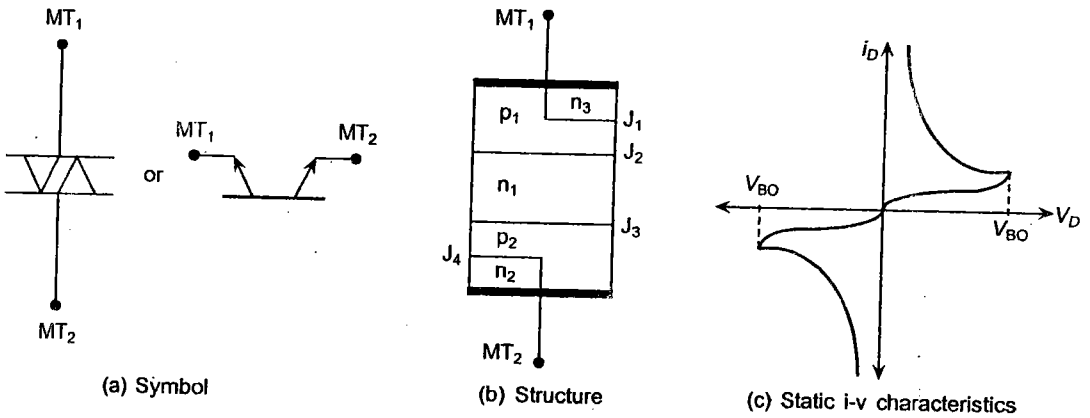


Figure 2.7 Diac.

2.3.9 PHOTODIODES

The photodiodes are used as light sensors. The falling light (photon) on the pn-junction of a diode generates electron-hole pairs. These charges diffuse across the junction and flow in a closed circuit as a current. The magnitude of this current depends upon the intensity of the light. Normally, this current is used as a base current to drive a transistor for further control applications. The principle of photodiodes is extended for the generation of electrical energy by solar photo-voltaic cell.

2.3.10 LIGHT-EMITTING DIODES (LED)

In general, an LED is used as an indicating device. When a current flows from anode to cathode, it emits light. It is used as logic/status indicator. It is also used in a display unit (e.g. seven-segment indicator). It is available in different size (in mm) and colour (red, yellow, green, white, etc.) and shape (circular, rectangular, etc.). Now gallium nitride (GaN) semiconductor is used for high-quality modern LED. Moreover, due to its white light output (like sunlight which has maximum clarity), GaN-LED is now being used in car headlights and for decoration lightings.

2.4

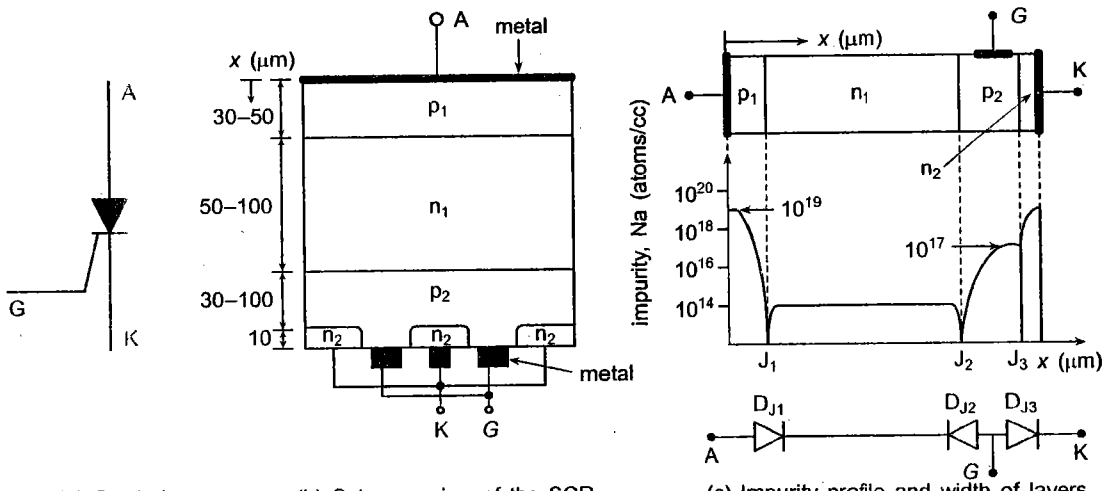
THYRISTORS (CONTROLLED RECTIFIERS)

The *thyristor* (or controlled rectifier) is a generic term and therefore a large number of power semiconductor devices belong to this family, for example, silicon controlled rectifier (SCR), triac, reverse-conducting SCR (RCT), asymmetric SCR (ASCR), light-activated SCR (LASCR), gate turn-off thyristor or SCR (GTO). etc. The conduction of all these devices is controllable by the current supplied to the gate terminal. Except GTO, the commutation (turn-off) depends upon the circuit condition, i.e. when anode current becomes almost zero (holding current level). Among these devices most commonly used device is the SCR which has most simple structure. In general, except triac, all these devices are unilateral (unidirectional) and therefore the load or main current flows from anode to cathode only. A GTO is also a thyristor but it will be discussed in the next section as its commutation or turn-off is achieved from the gate circuit.

2.4.1 Silicon Controlled Rectifiers (SCR)

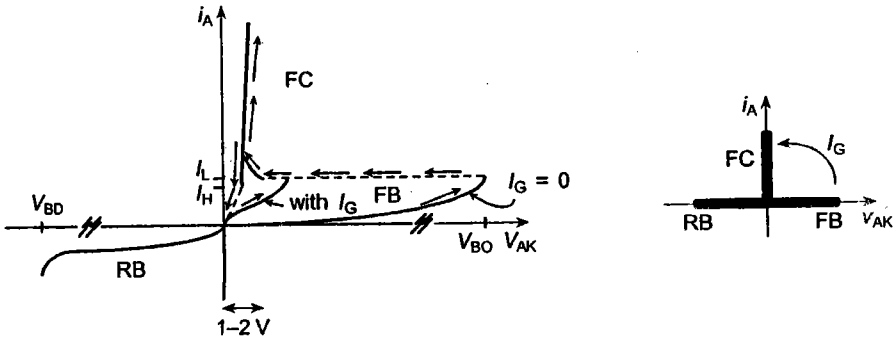
The silicon controlled rectifier is a most widely used device of the thyristor family. It is a robust device and its reliability is better than all other power semiconductor devices (except diode). It is its invention in 1957, which had created a new branch of electrical engineering, i.e. power electronics. Different types of SCR are available with very wide voltage and current ratings (from 1 A to several kA and from a few tens of volts to several kV).

It is a four-layer (*pnpn*) semiconductor device with alternate layers of p and n materials. There are three pn junctions and three terminals (ohmic contacts with different layers), as shown in Fig. 2.8. It also shows the width of each layer and the doping.(impurity) profile of the device. Both p_1 and n_2 layers are highly doped as in case of a semiconductor pn-junction diode. While n_1 region is very wide and lightly doped. The low doping enables wide SCL, thus it provides high forward and reverse voltage blocking capability of SCR. However, the voltage handling capability increases at the cost of



(a) Symbol (b) Cut-away view of the SCR (c) Impurity profile and width of layers

Figure 2.8 (*Cont.*)



(d) Actual characteristics (e) Ideal characteristics

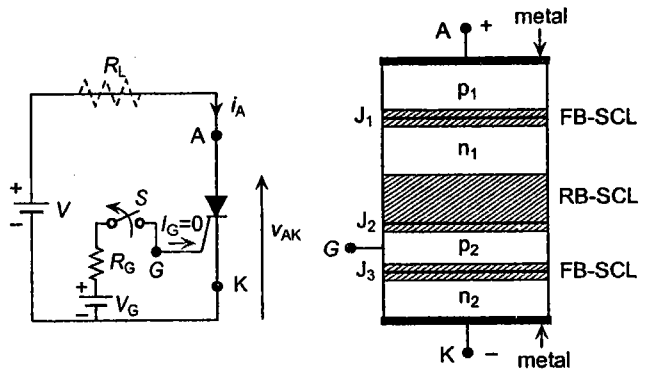
Figure 2.8 Various details of SCR.

the switching speed (turn-off) and on-state losses (which is proportional to the width of n_1 of the device. Therefore, for high speed or fast SCR, width of n_1 layer is reduced and impurity concentration of n_1 layer is increased adjacent to J_1 (it is called *electric field stopper* which prevents punch-through). Thus it reduces reverse-voltage blocking capability and on-state voltage drops at J_1. Reduced width and 'gold-lifetime killing' of n_1 region reduces recombination time of the carrier during turn-off. The thermal diffusion of gold in n_1 increases recombination centres.

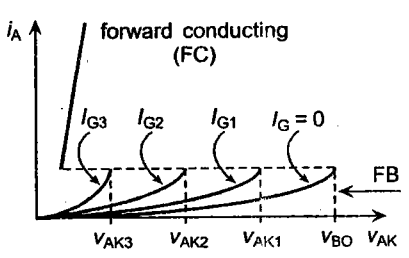
Basically, there are three operating regions of the device, namely, forward-blocking (FB), forward conducting (FC) and reverse-blocking (RB). These regions are shown in the actual characteristics and ideal characteristics (Figs. 2.8d and e).

2.4.2 Forward-blocking (FB) Region

This is a wide operating region, where the device anode current (i_A) and the device voltage (v_{AK}) vary over wide range due to different magnitude of gate current (I_G). Figure 2.9a shows the required gate and anode circuits of SCR. The width of the forward-biased junction SCL (FB-SCL) and the reverse-biased junction SCL (RB-SCL) depends upon doping and biasing. The anode is at

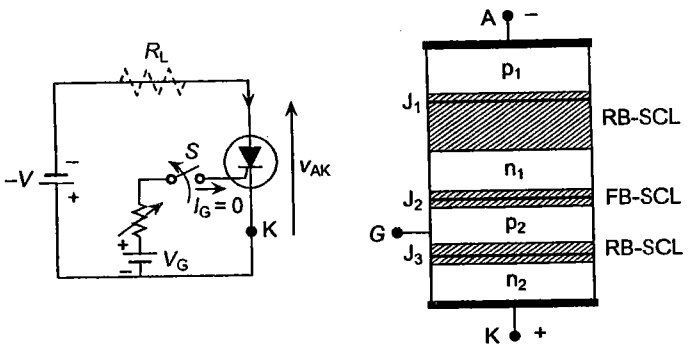


(a) Forward blocking (FB)



(b) Effect of gate current on FB characteristics

Figure 2.9 (*Cont.*)



(c) Reverse blocking (RB)

Figure 2.9 FB and RB conditions of SCR.

higher potential than the cathode. Therefore, junctions J_1 and J_3 are in forward-biased condition and J_2 is in reverse-biased condition. Therefore, SCL at forward-biased condition is thin and at reverse-biased condition, it is thick. Almost the whole supply voltage (V), appears across J_2 as the other two junctions are in forward-biased condition. Let the switch (S) is open, therefore gate current (I_G) is zero. If the device voltage, v_{AK} (which is almost equal to the supply voltage) is gradually increased, SCL grows (mostly in n_1 across J_2). A reverse leakage current (i_A) due to reverse based J_2, flows between A and K terminals. If v_{AK} is continuously increased, i_A is still within mA range. However, if v_{AK} reaches to V_{BO} level, breakdown of J_2 occurs. There are two methods of breakdown in semiconductor devices, namely, punch-through and avalanche. In punch-through, SCL extends far enough to reach the opposite end of the layer (e.g. in this case, SCL of n_1 reaches SCL of J_1). In the later case, peak electric field becomes high enough to cause impact ionization and the carriers (hole or electron) of the leakage current get accelerated and with high energy ($e \times v_{AK}$) strike the covalent bond of the silicon atoms to liberate new electron-hole pair. These are accelerated in opposite directions (being minority carriers and because of high electric field). They again collide and liberate electron-hole pairs, again and again, till breakdown of the junction occurs. Most of the thyristors are designed to operate on this mechanism. Moreover n_1 is purposely widened to avoid punch-through condition.

If a gate current (I_G) is supplied by closing the switch (S), the same phenomenon of breakdown occurs at much lower voltage of v_{AK} for $I_G = I_{G1}$, as shown in Fig. 2.9b. Similarly, it can be further reduced for higher value of the gate current, I_{G3}, where $I_{G3} > I_{G2} > I_{G1} > I_G$. This region is called *forward-blocking* (FB) region, where SCR do not conduct. In general, supply voltage for SCR is maintained far below V_{BO} level and forward-blocking state to forward-conducting (FC) state is switched by the application of the gate current of the low magnitude and low power.

2.4.3 Forward Conducting (FC) Region

When an SCR is in forward biased condition and the required gate current is applied, breakdown of J_2 junction occurs. All the device layers are now flooded with charge carriers. Ideally, the device shows zero impedance (resistance) between A and K, and the device current is now restricted by the external load only (if any). Normally, a few volts of gate voltage (V_G) is enough for conduction of the device. Moreover, v_{AK} is limited to a few volts only. In this region, i-v characteristic follows (approximately) ohm's law and due to increase of the main-terminal current (i_A) ohmic drop, v_{AK} also increases slightly.

2.4.4 Reverse-blocking (RB) Region

When the anode is at a lower potential than the cathode, J_1 and J_3 are in reverse-biased condition and only J_2 is in forward-biased condition (Fig. 2.9c). Due to light doping of n_1, reverse-biased SCL (RB-SCL) of J_1 is wide. Most of the applied voltage appears across J_1. A reverse leakage current (i_A) flows through J_1 and J_3, which is very small. As the supply voltage (V or v_{AK}) increases, i_A increases till breakdown takes place at V_{BD}. This part of i-v characteristics exactly matches with the i-v characteristics of a diode in reverse-biased condition.

In general, the triggering of an SCR is done by supplying a gate signal of sufficient magnitude (few tens of milli-ampere and few volts). However, triggering is only possible when the thyristor (SCR) is in forward biased condition and i_A should be equal to or greater than a minimum level, called the *latching current* (I_L). It is related with the minimum number of carrier in the device that is necessary to flood J_2 such that it loses its semiconductor characteristics (SCL vanishes). After the conduction of thyristor (SCR), if the load current or i_A is made to reduce, at certain level of i_A, called *holding current* (I_H), the thyristor ceases its conduction. It is the minimum anode current (i_A) that holds the conduction of a thyristor. Due to the reduced current, the carriers flowing through J_2 also reduce and n_1 and p_2 regain their semiconductor properties. Therefore, SCL or depletion layer forms again across J_2, which is reverse biased and brings back the device into blocking state. Unlike a BJT or other devices from the transistor family, when the thyristor (SCR) is triggered, no gate signal is further required to maintain the on-state. Only when i_A becomes less than I_H, device turns off. The reswitching needs a new gate-trigger signal and forward-biased condition of the device. The SCR is able to block both forward and reverse voltage of sufficiently high magnitude (several hundred V to several kV). Since it is a unilateral device, current always flows in one direction only. Any attempt of reversal of the direction of the current causes device commutation or device turn-off.

2.4.5 Triggering of Thyristor

There are several methods by which thyristors can be triggered or turned on:

Thermal turn-on When the temperature of a device increases, more electron-hole pairs are generated. Due to the free movement of minority carriers across J_2, reverse leakage current increases. When these charges cross the junction, get accelerated and strike the covalent bonds of the silicon to liberate more elector-hole pairs. This process continues with more new carriers. The layers (n_1 and p_2) become flooded with their carriers and lose their semi-conductor properties. They behave as a conductor due to large number of thermally generated carriers. Ultimately conduction takes place.

Because $I_G = 0$, no current is supplied from the gate terminal. However this method is not used as it increases the junction temperature, which reduces voltage withstand capability of the device.

High forward voltage By increasing forward voltage (v_{AK}) beyond V_{BO}, the device turns-on (as explained for the i-v characteristics). However, this method is practically never used.

Rate of change of voltage (high dv_{AK}/dt) When a thyristor (SCR) is forward biased, the middle junction (J_2) is reverse biased which blocks the conduction of the device. The junction J_2 has a sufficiently large value of capacitance across depletion layer or SCL. Thus if there is a positive spike or a sudden change in applied voltage (high dv_{AK}/dt), it causes a charging current, $i_{Cj2} = C_{j2}(dv/dt)$ to reach p_2 layer of the device (as if a gate current is supplied to p_2 from G). Thus the device turns on undesirably. This method of switching of thyristor is never employed rather it is an undesirable triggering of a thyristor, which has to be avoided. That is why, snubber circuits are used.

Light triggering When a beam of light falls on the blocking junction of the device, it generates electron-hole pairs. Due to the flow of carriers (current) that reaches p_2, it turns-on the device (as if a gate current is supplied to p_2 from the terminal G). However, this method is used in an LASCR which is used for high-voltage and high-current applications (e.g. HVDC transmission system, static VAR control, etc.). Normally, a fibre-optical system is used to trigger LASCR which provides a high level of electrical isolation from control circuit to the device. Both the gate control circuit and the high-voltage power circuit are linked by high-insulation fibre optical cable. Direct radiation of silicon wafer, by the light coming through an optical cable, generates electron-hole pair which (minority carrier) crosses the blocking junction (J_2) under the influence of high electric field and strike the covalent bond of silicon wafer to generate more electron-hole pairs. The process continues till trigger of LASCR takes place.

Gate control In general, thyristors are switched by the application of a gate signal. For reliable operation and successful triggering of the device, the V_G and I_G should be close to their maximum limit without exceeding the limiting values. Normally, integrated circuits (TTL, CMOS and analog/ linear) based low-power control circuits are used. The power output capability of these IC is very poor. In general, these IC are unable to drive the gate of power semiconductor devices directly. Moreover, gate drives are either electrically-isolated type or direct conduction type. In the former case, a pulse transformer or an opto-coupler is used (in a driver and buffer circuit). However, for above a few kV, optical fibre cables are used. The gate triggering circuits are discussed in detail, in Chapter 3.

2.4.6 Dynamic Switching Characteristics of SCR

The transition from one state to another state of thyristor is not instantaneous rather it takes place in a finite time. The static i-v characteristics do not give any indication of the capability or speed at which the SCR jumps from forward blocking state to forward conducting state and also to reverse blocking state. The turn-on characteristic of a thyristor is shown in Fig. 2.10. The reference time starts where the gate current reaches 90% of its final value. The *delay time* (t_d) is the time required

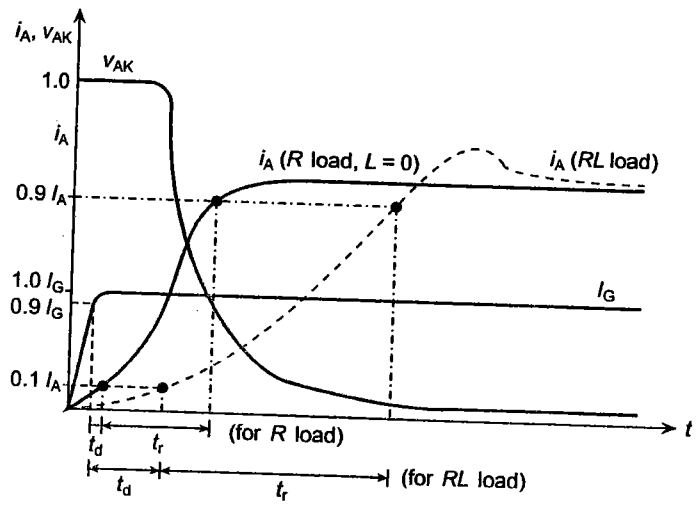


Figure 2.10 Dynamic switching-on characteristics of SCR with R load (L = 0) and RL load.

to reach anode current i_A 10% of the final value (I_A). The *rise-time* (t_r) is the duration, in which anode current (i_A) increases from 10% to 90% of its final value. The *total switching* (*turn-on*) period is ($t_d + t_r$). The switching phenomena can be explained using various models of thyristors described as follows.

Diode Model of Thyristor for Triggering (Turn-on)

With three pn-junctions, an SCR can be represented as three pn-junction diodes, as shown in Fig. 2.11. When it is forward biased, junction J_1 and J_3 shall be forward biased and ideally voltage drop across them is zero. Then the voltage, v_{AK} will appear across the reverse biased junction J_2. If

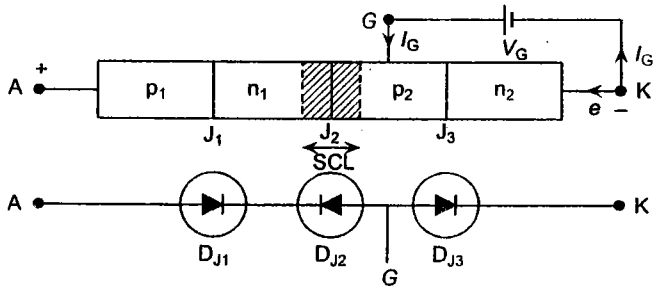


Figure 2.11 Biasing and equivalent diode model of SCR.

gate is biased positively (cathode, K is at lower potential), the gate current (I_G) flows from p_2 layer to n_2 layer or electron (e) reaches from n_2 to p_2. Thus p_2 of gate is flooded by electrons from cathode and it will lose its identity as a p layer (as this layer is lightly doped and electrons from n_2 are in excess). Now, electrons being minority carrier, easily cross the junction and accelerate with energy (eV_{AK}) at J_2. They may strike the covalent bond of silicon atoms to generate electron-hole pairs in n_1 layer. Again hole being minority carriers, reach p_2 and the same phenomenon repeats in p_2. Thus J_2 becomes flooded by crossing of the minority carriers from both the sides and conduction of the device takes place. Now, there is no more blocking of current by the reverse biased depletion layer as it does not exist due to flow of large number of carriers.

Two-transistor Model or Analogy

The pnpn wafer of the thyristor can be considered as two transistors, T_1 and T_2 connected in cascade mode, as shown in Fig. 2.12. T_1 and T_2 are pnp and npn transistors such that the collector of T_1 provides the base drive for T_2. The gate current and collector current of T_1 provide the base current for T_2. When a small gate current is supplied to the base of T_2, the amplified collector current (which is also base current of T_1) generates very large collector current of T_1. This current is again supplied to the base of T_2. Thus a positive feedback is initiated and, within a few microseconds, saturation is immediately reached. The current is only limited by the external load connected with transistor (thyristor).

For any bipolar transistor,

$$I_C = \alpha I_E + I_{CBO} \tag{2.2}$$

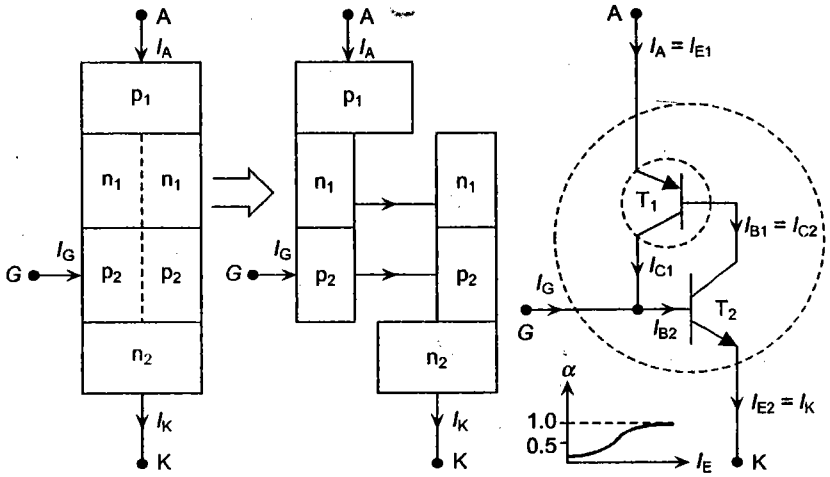


Figure 2.12 A transistor model of SCR.

where α is the dc current gain of a transistor and I_{CBO} is the collector leakage current with zero base current.

For transistor T_1,

$$I_{C1} = \alpha_1 I_{E1} + I_{CBO1} \tag{2.3}$$

$$= \alpha_1 I_A + I_{CBO1} \tag{2.4}$$

For transistor T_2,

$$I_{C2} = \alpha_2 I_{E2} + I_{CBO2} \tag{2.5}$$

$$= \alpha_2 I_K + I_{CBO2} \tag{2.6}$$

Applying Kirchhoff's current law (KCL) at transistor T_1 (small dotted circle shown in Fig. 2.12), we get

$$I_A = I_{C1} + I_{B1} = I_{C1} + I_{C2} \tag{2.7}$$

$$= (\alpha_1 I_A + I_{CBO1}) + (\alpha_2 I_K + I_{CBO2}) \tag{2.8}$$

Applying KCL at device terminals (larger dotted circle),

$$I_K = I_G + I_A \tag{2.9}$$

Putting this value of I_K in Eq. (2.7),

$$I_A = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_G + \alpha_2 I_A + I_{CBO2}$$

$$= (\alpha_1 + \alpha_2) I_A + \alpha_2 I_G + I_{CBO1} + I_{CBO2} \tag{2.10}$$

or

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)} \tag{2.11}$$

On application of a small magnitude of I_G, I_K increases. Since $I_K = I_{E2}$, α_2 also increases. The increase of α_2 increases I_{C2} (as $I_C \cong I_E$). Thus I_{B1} hence I_{E1} increases (as $I_{E1} = I_{C1} + I_{B1}$), which in turn increases α_1. Ultimately, the increase of loop gain $(\alpha_1 + \alpha_2)$ reaches 1, i.e. each transistor

drives another one into saturation. The device reaches a conduction state, and I_A becomes ideally infinite. However, practically it is limited by the external circuit impedance only. The voltage drop across the device is approximately that of a single pn-junction.

Dynamic or Transient Model

Each pn-junction of a thyristor can be represented by a resistance and a capacitor connected in parallel (Fig. 2.13). When a junction is forward-biased, the junction resistance can be considered to be zero. Thus junction capacitance becomes insignificant (as if short-circuited by the resistance).

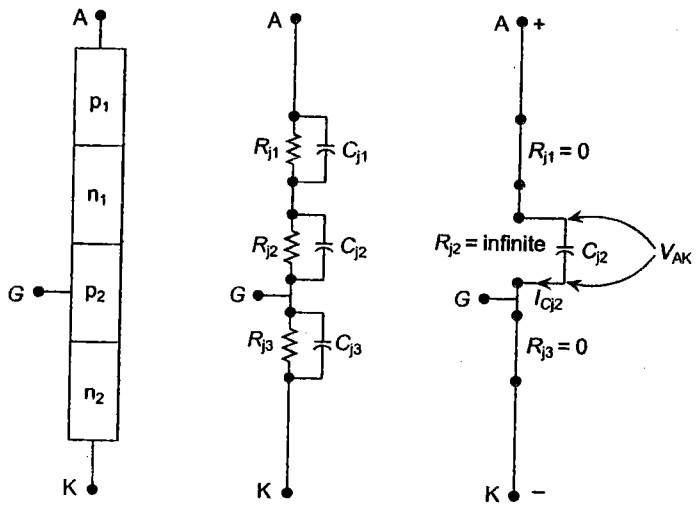


Figure 2.13 A dynamic (switching-on) model of SCR.

Similarly, when a junction is reverse-biased, the junction resistance can be considered to be infinite. Now, the junction capacitance (C_j) becomes significant. However, under a dynamic or transient condition, due to change of status of junction, the capacitance of each pn-junction becomes significant and they influence the thyristor characteristics. The charging current of a capacitor is given by

$$i_C = \frac{dq}{dt} \tag{2.12}$$

where q is the charge on capacitor. When the thyristor is in forward blocking state, J_1 and J_3 are in forward-biased condition, thus offer ideally zero impedance. However J_2 is in reverse-biased condition and offers ideally infinite impedance. Thus C_{j2} becomes significant, as shown in Fig. 2.13. The charging current of J_2 is given by

$$i_{j2} = \frac{dq_{j2}}{dt} = \frac{d(C_{j2}v_{j2})}{dt} \tag{2.13}$$

$$= V_{j2}\frac{dC_{j2}}{dt} + C_{j2}\frac{dv_{j2}}{dt} = C_{j2}\frac{dv_{j2}}{dt} \qquad \text{(as } C_{j2} \text{ is constant)} \tag{2.14}$$

$$= C_{j2}\frac{dv_{AK}}{dt} \qquad (v_{AK} \text{ is almost equal to } v_{j2}) \tag{2.15}$$

If a rapidly rising voltage (large *dv/dt*) is applied across anode and cathode (V_{AK}), the magnitude of i_{j2} becomes large. It reaches to p_2 (gate p-layer) as if a gate current is supplied. If i_{j2} is sufficiently larger than I_L (the latching current level of I_A), SCR comes into conduction mode undesirably (without applying the gate pulse).

Example 2.1 Find the absolute maximum operating or switching frequency of a converter grade SCR whose turn-on time and turn-off time are 3 μs and 200 μs, respectively.

Solution A device turns on and turns off in each switching cycle of a converter. The absolute minimum period of the switching cycle should be greater than or equal to the total switching period (turns on and turns off). The minimum period is, therefore, given by

$$T_{min} = t_{turn\text{-}on} + t_{turn\text{-}off} = 3 + 200 = 203 \ \mu s$$

The absolute maximum operating frequency of the SCR is given by

$$f_{max} = \frac{1}{T_{min}} = \frac{1}{203 \times 10^{-6}} = 4.9 \text{ kHz}$$

2.4.7 Effect of *dv/dt* and Snubber Circuits

When there is an abrupt change of current, a high voltage is produced by the circuit inductance (*Ldi/dt*). This may be as high as 1000 V/μs. If this voltage pulse, or a voltage with steep wavefront (high *dv/dt*) is applied across a thyristor, this may undesirably push the device into conduction state even though no gate current is supplied. The charging current, $i_C = C_{j2}(dv/dt)$, flows through the central-junction capacitor (of dynamic model) due to steep rising voltage (step or ramp). If this current (i_C) is sufficient in magnitude, i.e. (more than I_L), a regeneration action may begin (as if a gate current is injected) and ultimately thyristor turns on. To avoid this condition snubber circuits are used. In general, there are four types of snubber circuit, namely:

1. Turn-off snubber circuits to reduce sudden rise of voltage (*dv/dt*) across the device,
2. Turn-on snubber circuits to reduce sudden rise of current (*di/dt*) through the device,
3. Snubber circuits for reducing voltage and current stresses on the device during switching, and
4. Energy recovery snubber circuits.

If a step voltage is applied on a thyristor with a resistive load, the circuit behaves as a simple RC circuit due to J_2 junction capacitor (Fig. 2.14a). The voltage across the device (anode–cathode voltage, v_{AK}) varies, as shown in Fig. 2.14b. If another capacitor C is also connected, the rise of v_{AK} reduces. Thus *dv/dt* limitation can be improved by connecting a RC network across the thyristor which is called a *turn-off snubber* circuit (Fig. 2.14c and 2.14d). It reduces *dv/dt* and also undesirable switching of the device.

An inductor of low value is normally connected in series to reduce a sudden rise in the current (*di/dt*) through the device, which otherwise may be destructive for the device. It is called *turn-on snubber* circuits (it is discussed in detail in the next section).

Moreover, the snubber circuits improve the switching trajectory locus of the device's i-v plane, which is used to prevent high voltage and high current stresses on the devices at high frequency switching. Thus, during switching, the snubber circuit does not allow both voltage and current to rise or fall simultaneously, thereby reduces switching losses.

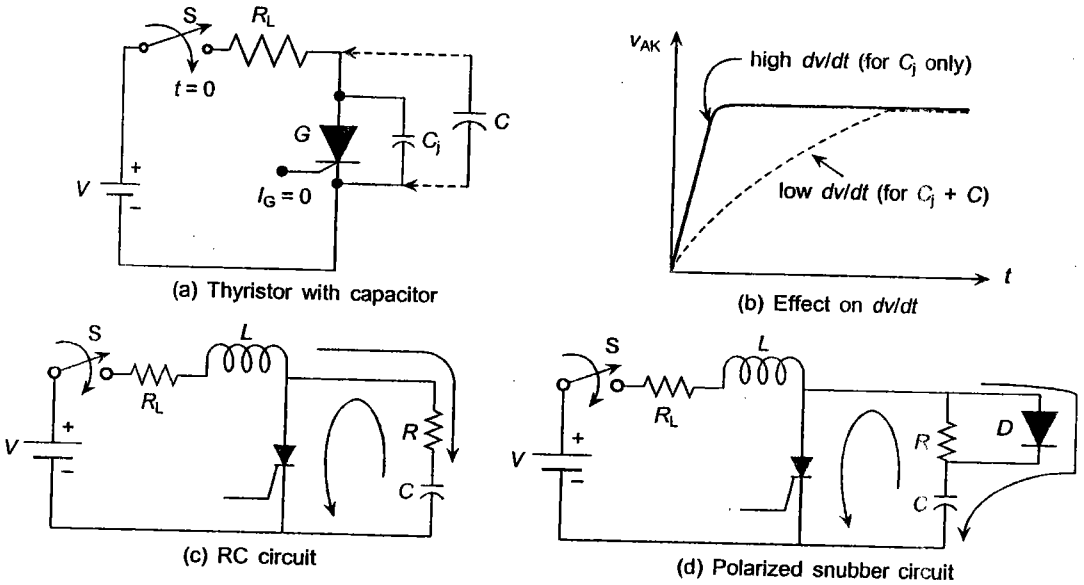


Figure 2.14 Snubber circuits.

For high-frequency switching applications, the losses in the snubber circuit becomes considerable. Therefore, the energy recovery snubber circuits are used to re-supply the energy trapped in L and C, back into the source or the load.

In RC snubber circuit, C gets charged up to the maximum applied voltage during forward-blocking state. When the thyristor conducts, the capacitor discharges through it. With a very small on-state resistance, the discharge current may be undesirably high. To limit this discharge current, a resistance (R) is also connected in series (Fig. 2.14c). Since there is no forward-blocking state for power diodes, C does not retain high positive voltage and diode conducts smoothly as soon as it becomes forward biased. Therefore, only C is enough for diodes and R is not needed. A polarized snubber circuit (Fig. 2.14d), is used with thyristors as well as transistors to enhance the performance. For a polarized snubber circuit, the charging is quick and through the diode when a thyristor is switched on, the capacitor discharges through R. The diode bypasses R to reduce response time of RC for positive spikes (which may turn on the device).

The voltage, across the snubber circuit (v_{RC}) also appears across the device. With the line inductance and load inductance (if any), the RC branch forms an RLC under-damped circuit (Fig. 2.14). A low value of R reduces the switching losses of the device but the damping ratio (ξ) also reduces. The reduced value of ξ causes a higher overshoot in the output voltage (second-order system) which appears across the device. When the value of ξ varies between 1 and 0.5, the voltage overshoot varies between 0% and about 15%. Therefore, ξ is normally maintained between 0.5 and 1.

When a step input voltage (or the worst-case peak ac voltage) is applied, v_{RC} can be found using the current response equation of an RLC under-damped circuit (given in Appendix A). It may be noted that v_{RC} gives the value of the transient voltage including the overshoot that appears across RC or device. Similarly, dv_{RC}/dt gives the rate of change of the transient voltage.

When C is charged with maximum or peak voltage (during forward-blocking condition), it discharges through the thyristor (or SCR) and R limits the peak current. Therefore, the value of R can also be selected from the maximum or rated current of the device (I_T). That is

$$R = \frac{V}{I_T} \tag{2.16}$$

It is necessary to keep the worst-case transient voltage (V plus overshoot voltage) less than the forward-blocking voltage of the device. Moreover, the sudden rise of the transient voltage across the device should be less than the rated *dv/dt* of the device. The snubber circuit should be designed according to these two considerations. Normally, the transient voltage is of the order of 1000 V/μs in a converter/device circuit. While the maximum device (thyristor/SCR) *dv/dt* rating varies from a few tens of V/μs to 200 V/μs. Therefore, to protect the device, specially to avoid undesirable or false triggering, the use of snubber circuits are necessary.

Example 2.2 A 400-V, 50-Hz ac source is connected with an SCR (OE-C50N) and a resistance load circuit. During the forward-blocking condition, the blocking junction capacitance (C_{j2}) is 1.6 nF. The parameters and rating of the SCR at 25°C are: I_T (rms) =110 A, $V_{DRM} = V_{RRM} = 800$ V, $V_{RSM} = 900$ V, $V_F = 2.0$ V, $V_{GT} = 2.5$. $I_{GT} = 50$ mA, $T_{jmax} = 120°C$, $dv/dt = 100$ V/μs and $di/dt = 30$ A/μs.

Show that if snubber circuit is not used, even a spike of 250 V and 2-μs duration will be sufficient to trigger the device undesirably (when the device is in forward-blocking condition).

Solution The rate of the rise of the voltage of the spike is given by

$$\frac{dv}{dt} = \frac{250\text{ V}}{2}\ \mu\text{s} = 125\text{ V/}\mu\text{s}$$

This value is higher than the *dv/dt* limit of the device (i.e. 100 V/μs). The charging current through the capacitor, that reaches p_2, is

$$i_{Cj2} = C_{j2}\frac{dv}{dt} = 1.6 \times 10^{-9}\,(125\text{ V/}\mu\text{s}) = 200\text{ mA}$$

Since this current is greater than the minimum gate current required to trigger the SCR, (i.e. $I_{GT} = 50$ mA). SCR will be falsely triggered. It may be noted that this current is negligibly small at the normal forward-blocking condition with a higher steady-state voltage (i.e. 400 V). That is

$$I_{Cj2} = \frac{V}{1/(\omega C_{j2})} = V(2\pi f C_{j2}) = 400 \times 100\pi \times 1.6 \times 10^{-9} = 201\ \mu\text{A}$$

Example 2.3 Design an RC snubber circuit for a given SCR (OE1600 series) used in a converter circuit. The supply voltage is 230-V ac and the stray (or line) inductance is 150 μH.

Solution From the data sheet (Section 2.7), *dv/dt* limit, $S = 20$ V/μs. The peak or maximum supply voltage, $V = \sqrt{2} \times 230 = 325.3$ V. To reduce the overshoot voltage across the device, during the transient condition, ξ is kept between 0.5 and 1. For $\xi = 0.5$, the voltage overshoot is about 15%. If ξ is selected 0.6, the overshoot voltage will reduce further. From the expression of S, for $\xi > 0.5$, the value of R is given by

$$R = \frac{SL}{V} = \frac{20 \times 10^6 \times 150 \times 10^{-6}}{325.3} = 9.2\ \Omega$$

When C is charged with peak supply voltage (during forward-blocking condition), it retains the charge at the peak voltage. When SCR conducts, C discharges through SCR and R limits the peak

current. The value of the discharge current should not exceed the rated SCR current (16 A). Therefore, the value R can also be selected from this condition. Then

$$R = \frac{V}{I_T} = \frac{325.3}{16} = 20.3\ \Omega$$

Therefore, $R = 20\ \Omega$ will be a good choice. The value of C is given by

$$C = \frac{4V\xi^2}{RS} = \frac{4 \times 0.6^2 \times 325.3}{20 \times 20 \times 10^6} = 1.17\ \mu F$$

Take, $C = 1.22\ \mu F$.

2.4.8 Effect of Rate of Rise in Current (di/dt)

An SCR can be considered to consist of a large number of elementary SCR adjacent to each other (Fig. 2.15). When the gate signal is applied, electrons flow from cathode to gate and some of them

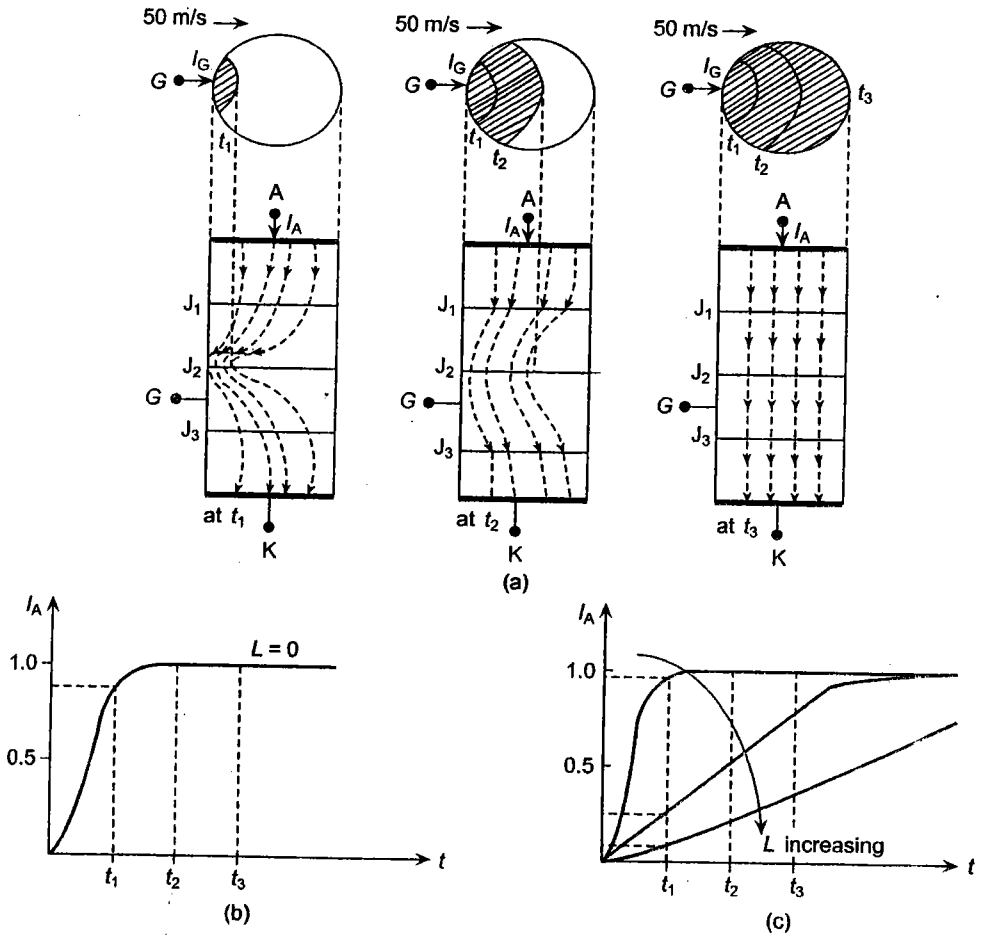


Figure 2.15 Thyristor conduction and effect of di/dt.

diffuse across J_2 in the region nearest to gate connection. It causes collapse of reverse biased J_2 junction near the gate terminal. Hence, at first, the elementary SCR nearest to gate (i.e. the left most) turns-on and thereafter the next adjacent elementary SCR turns on and so on, in a finite time. This happens due to a finite spreading velocity of carriers (50 m/s) along J_2 layer. Hence device takes some finite time (2–4 μs) to turn on completely. A fast rising anode current (i_A) reaches to the steady state level quickly, which may result in high current density in the elementary SCR (near the gate). This high I^2R loss in small area may lead to excessive localized heating at J_2 and therefore destruction of the thyristor. Thus a thyristor needs protection against high rate of rise in current (*di/dt*). A protective circuit used to protect a power semiconductor device during turn-on condition is called turn-on snubber circuit.

Remedies of *di/dt*

Following steps may be taken to reduce the steep change in the device current during turn-on:

- By improving gate structure by incorporating amplifying gate structure (a pilot SCR). The pilot SCR supplies large current to the gate of the main SCR.
- By connecting an inductor in series to slow down fast rising current, I_A.
- By fast rising gate pulse (hard gate driving) cause fast spread of carriers, along the blocking junction (J_2). Thus whole surface of J_2 comes into conduction quickly and no concentration of current or hot spot develops.

Both turn-on and turn-off snubber circuits modify the device switching trajectory and therefore reduce switching losses. The snubber circuits temporarily store energy in inductors and capacitors and usually dissipate it in resistors.

At a high frequency the switching losses become significant. Besides energy wastage, the heat transfer from the converters becomes a serious problem. Energy recovery snubber circuits are therefore used to either pump back the energy into the supply (power source), or to the load. Both active and passive snubber circuits are used for this purpose. In active snubber circuits, additional semiconductor switching devices are used.

2.4.9 Thyristor Gate Characteristics

Normally, a dc signal is required for triggering the thyristors. It may be a constant magnitude dc signal, single pulse, a slow-rising dc signal or a train of high frequency (5–20 kHz) pulses. A typical gate characteristic for a dc signal is shown in Fig. 2.16. In this case, the minimum V_G and

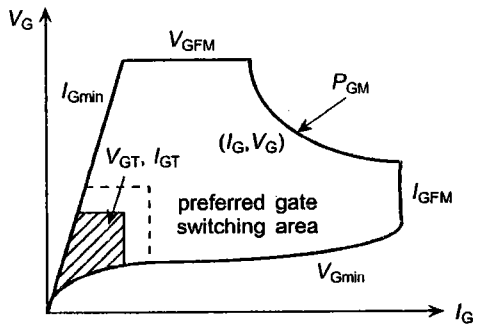


Figure 2.16 Gate characteristics of thyristors.

minimum I_G are required. For high-frequency gate signals, the limiting values of gate characteristics increase due to some initial recombination of charge in gate p-region. If a gate switching pulse duration is reduced from 100 μs to 1 μs, then V_G and I_G are required to increase by 2 and 10 times, respectively. The gate characteristics are also affected by the junction temperature. For different temperature, the possible minimum-trigger values of V_G and I_G are V_{GT} and I_{GT}. For a particular temperature (say 25°C), the preferred gate drive area is beyond these typical values (shown by the shaded area in Fig. 2.16). These values increase if the temperature decreases, as shown by the broken line, thus preferred gate drive area changes. The V_{GT} and I_{GT} have a negative temperature coefficient of the resistance. For a reliable turn-on of all devices, the trigger circuit must provide a dc signal (V_G, I_G) outside the shaded area and within the preferred switching area. Here V_{GFM}, I_{GFM} and P_{GM} are maximum forward gate voltage, current and power ratings, respectively. Therefore, the most preferred value of the gate current and voltage are close to its maximum values of the gate current and voltage (I_{GFM} and V_{GFM}).

2.4.10 Turn-off Characteristics

When an SCR is conducting with an anode current i_A and if a reverse voltage is applied, all the excess carriers (electron from n_2 and holes from p_1 layers) sweeps out from the outer layers and a reverse recovery current sets up. This negative current (reverse recovery current, I_r) may be much greater than the rated reverse blocking current. The duration for which the reverse recovery current flows is known as *reverse-recovery time* (t_{rr}) and the charge ($I_r \times t_{rr}$) is known as *recovered charge* (Q_r). The excess carrier in the inner two layers (n_1 and p_2) decay only due to their recombination. The minimum time required for it is t_{qr}. Thus t_q (the total turn-off time) is equal to ($t_{rr} + t_{qr}$), where t_{qr} is called *gate-recovery period*. At the end of t_q, a depletion layer develops across J_2 and the device can withstand now the forward voltage.

The turn-off period (t_q) varies (approximately proportionally) upon the magnitude of peak anode current (i_A), reapplied voltage gradient (dv/dt) and temperature (T_j). Also, it is inversely proportional to the magnitude of the reapplied voltage (v_{AK}), as shown in Fig. 2.17.

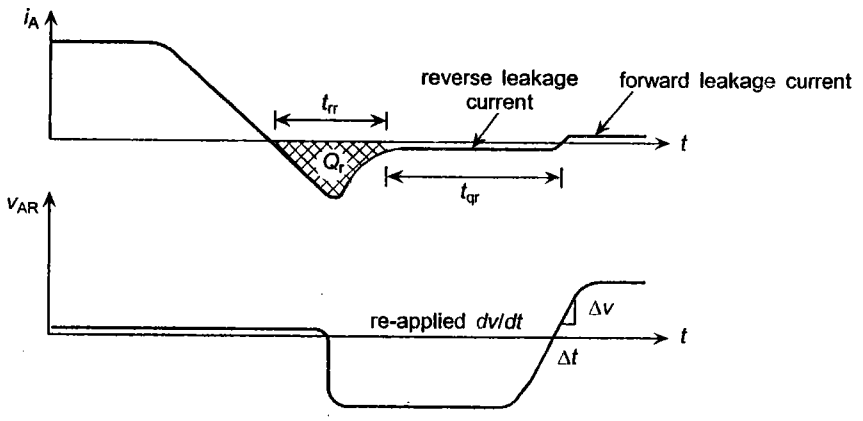


Figure 2.17 Waveforms at forced turns-off.

2.4.11 Thyristor Ratings

Each power-semiconductor device has a limited capability of handling the power, i.e. voltage and current. Basically, it depends upon the temperature-withstand capacity of pn-junctions at the steady-state and dynamic conditions. After thoroughly testing a particular device, manufacturers prepare the device specifications. It specifies critical values of different parameters and the boundaries of the recommended safe operating area (SOA) of the device:

Ratings It depends upon the condition of thyristors/SCR. The ratings can be classified as:

(a) *Continuous rating:* These ratings are related with the continuous working condition of the device. It is expressed in terms of average or RMS values, depending upon whether the device experiences unilateral or bilateral voltages.

(b) *Repetitive rating:* This rating is useful when the device is switched on periodically.

(c) *Surge or non-repetitive rating:* A surge rating corresponds to the maximum permissible non-repetitive current and voltage peak (that rarely appears), which the device can withstand during a surge. At this condition, the junction temperature exceeds the permissible value for a short time only.

A device is specified by different current and voltage ratings in both forward and reverse directions, as shown in Fig. 2.18.

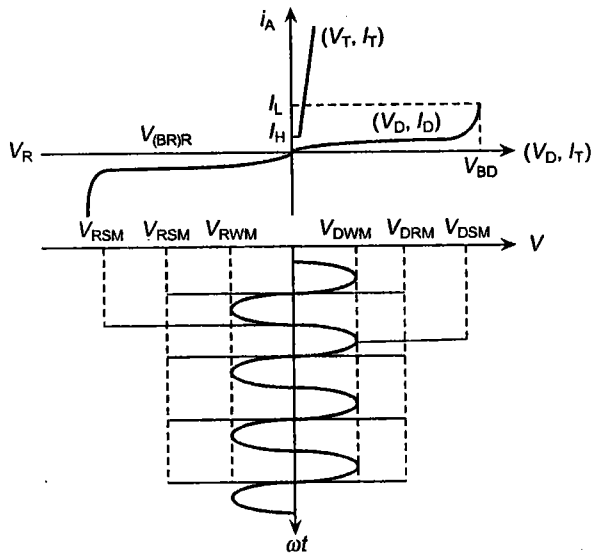


Figure 2.18 Different critical/limiting ratings of thyristors.

List of Subscripts

The instantaneous value of current, voltage and power is represented by lowercase letters. Normally, the maximum or peak value, dc or average value and rms value are represented by uppercase letters. A list of subscripts is given here, which is used for showing different ratings:

Av, av	Average values
D, d	Forward off-state; non-trigger (for gate) values
F, f	Forward
G, g	Gate terminals
H	Holding values
M, m	Maximum or peak values
P	Pick up or latching
Q	Turn-off values
R, r	Reverse, as first subscript; repetitive, as second subscript
RMS, rms	rms values
S, s	Surge or non-repeatitive (as second subscript)
T, t	Forward on-state; trigger (for gate) values
W	Working

Here, for thyristors, D and T are used for forward-blocking and forward-conducting conditions, respectively.

List of Symbols

The following is a list of symbols for diodes and thyristors:

I_D	Off-state current (dc)
I_F	Forward current (dc or average)
I_{FAV}	Total average forward current (to distinguish between average and dc, if necessary)
I_{FGM}	Forward maximum (peak) gate current
I_{FRM}	Repetitive maximum (peak) forward current
I_{FSM}	Non-repetitive maximum (peak) forward current
I_H	Holding current
I_{GT}	Gate current to trigger the device
I_P	Pick-up current or latching current
I_R	Reverse current (dc)
I_{RG}	Reverse gate current
I_{RRM}	Repetitive reverse maximum (peak) current
I_T	Forward on-state current (dc)
I_{TAV}	Average (forward) on-state current
$I_{T(RMS)}$	rms value of (forward) on-state current
I_{TRM}	Repetitive maximum or peak (forward) on-state current
I_{TSM}	Non-repetitive maximum or peak (forward) on-state current
P_{GAV}	Average gate power dissipation
P_{GM}	Maximum or peak gate power dissipation
P_{RAV}	Average reverse power dissipation
P_{RRM}	Repetitive maximum or peak reverse power dissipation
P_{RSM}	Non-repetitive maximum or peak reverse power dissipation
t_{off}	Turn-off time
t_{on}	Turn-on time
$V_{(BO)}$	Breakover voltage (forward)

$V_{(BR)R}$	Reverse breakdown voltage (reverse)
V_D	Continuous off-state voltage (forward)
V_{DRM}	Forward repetitive maximum (peak) off-state voltage
V_{DSM}	Forward surge or non-repetitive maximum (peak) off-state voltage
V_{DWM}	Forward working maximum off-state voltage
V_F, V_T	Continuous forward on-state voltage
V_{FGM}	Forward maximum or peak voltage, gate-cathode
V_{GD}	Gate-cathode voltage not to trigger the device
V_{GT}	Gate-cathode voltage to trigger the device
V_R	Continuous reverse voltage
V_{RGM}	Reverse maximum or peak voltage, gate-cathode
V_{RRM}	Reverse repetitive maximum or peak voltage
V_{RSM}	Reverse non-repetitive or surge, maximum voltage
V_{RWM}	Reverse maximum working voltage.

2.4.12 Thyristor Protection

The operating condition of thyristors should be within the specified limits or ratings, supplied by the manufacturers. A fault or overload condition may cause excess load current to flow through the device which may cause its destruction. Similarly noise, voltage transients or spikes may cause undesirable effects including device turn-on. The protection against fault current can be avoided by connecting a fuse arrangement in series. The effect of (di/dt) is reduced by connecting an inductor in series with the device. Similarly, transient voltage or voltage spikes are diverted by snubber circuits, or reduced to safe limit by surge absorbing device like varistor, power Zener diodes, etc.

General considerations In general, different devices are at different potentials in a converter. For high-voltage applications, several devices are connected in series. The potential level of each device varies among themselves as well as with respect to the ground. Proper insulation coordination is, therefore, necessary.

Each device needs proper fastening with heatsink for maximum heat-transfer. Usually, manufacturers specify and recommend a maximum torque value (in kg-cm or lbs-in as a mechanical parameter). At lower torque fastening, contact resistance will appear between the device terminals (A, K, D, S, E, C, etc.) and the connecting wire/cables. Similarly, at higher torque, the device may break. A wrench with torque measurement facility or a special bolt-nut arrangement for a given torque may be used. Moreover, placements (position) of several devices are also important. An unsymmetrical placement for parallel connection on the same heatsink may cause unsymmetrical current distribution as well as a non-uniform heat flow. The device in middle position will have more inductance due to more flux linkage with it. Therefore, it may share less current, specially during the transient and switching conditions. Thus these problems are removed by the symmetric placement of the devices on the heatsink.

The stray magnetic fields reduce the performance of device and may contribute a high voltage stress, $v = Ldi/dt$ to the device (due to sharp rise or fall of current during turn-on or turn-off). Also, series inductance with stray capacitance causes a higher voltage oscillation in the gate circuit and limits high-frequency operation of the device.

Over-current protection A high-rapturing capacity (HRC) fuse, semiconductor fuse or even rewirable fuse can be used for this purpose. Sometimes, for sensitive power electronic systems

'crowbar' protection technique is used. In this arrangement, at abnormal condition (voltage or current), disconnection of sensitive system is done by quick forced-blow of fuse. For HRC fuse, the fuse is coordinated with thyristor such that thyristor I^2t rating should be less than the I^2t withstand ability of the fuse. Fuse protection is mainly applicable to thyristors and diodes, which are robust devices. The response of a fuse is not fast enough to protect transistors or other fast switching gate-commutation devices, successfully.

Over-voltage protection Normally voltage transients are generated due to different types of switching e.g. insulation breakdown, arcing, blow of fuses, closing or opening of contactors, freewheeling diode snap, switching of transformers, etc. A large voltage spike for a few microseconds may result in a permanent device failure. Similarly extensive noise may be injected into a low-power logic control circuit causing spurious fault.

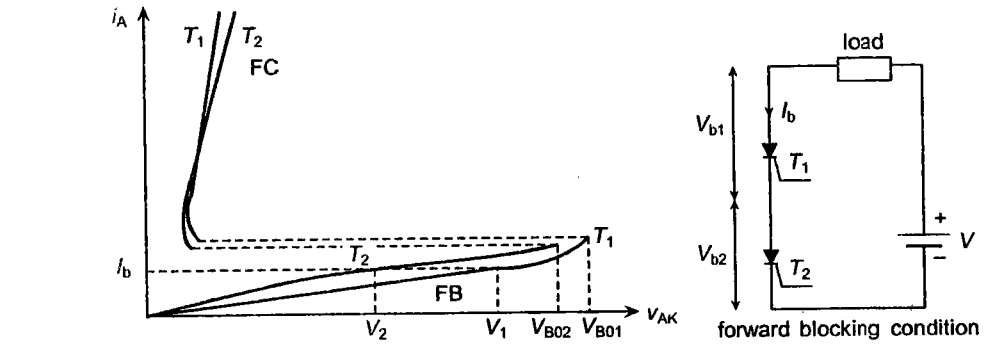
Low-pass filters (to divert high-frequency transients), diverters (reverse selenium rectifiers, Zener diode, varistors or thyrectors) and snubber circuits are used for this purpose. Crowbars are also used for voltage clamp. However crowbars and snubber circuits are usually slow to respond. The most useful, effective, compact and fast suppressors are the Zener diodes and varistors. Their response time is of the order of few nano-seconds.

2.4.13 Series and Parallel Operation of Thyristors

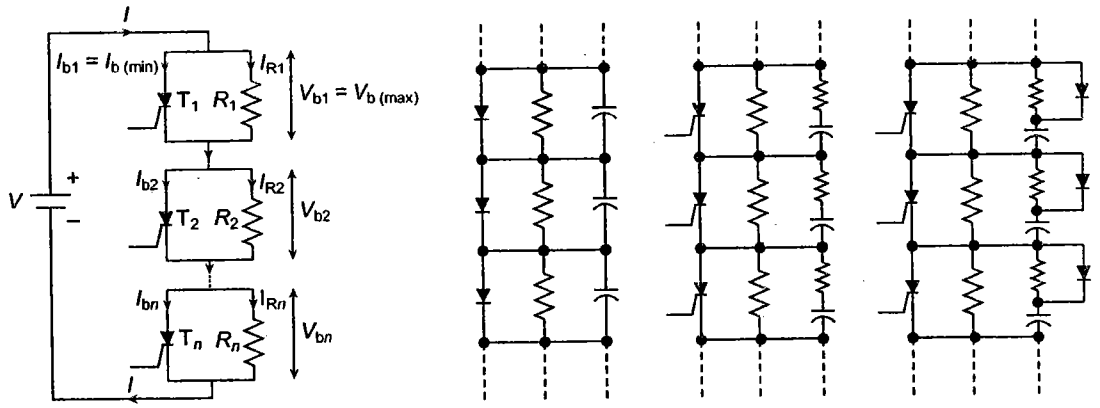
The power handling capacity of a device is limited. It depends upon device area utilization, encapsulation and cooling efficiency. For high-power applications, series and parallel combinations are used, where current and voltage requirement exceed the device current and voltage ratings. Therefore, the devices are connected in series to increase the voltage handling capability, and in parallel to increase total current rating. Series and parallel connections of devices are normally employed in converter plants of an HVDC transmission system. Similarly, several MOSFETs are connected in parallel to increase their current rating in PWM inverters.

Series Connections

When the devices are connected in series for high voltage applications, at both steady-state and dynamic conditions, the voltage must be shared equally by each device individually. Otherwise, an unequal voltage distribution may take place. This variation of voltage in forward and reverse blocking conditions are due to blocking current, junction capacitance, delay time, on-state voltage drop and reverse-recovery of individual power-semiconductor device. At the steady-state condition, the device having the highest leakage-resistance supports the maximum voltage. Figure 2.19a shows the forward voltage-current (blocking) characteristics of two typical devices (SCR). Although the same off-state leakage current or forward blocking current (I_b) flows through both the devices, but each supports different voltages: V_1 and V_2. The total voltage blocked is ($V_1 + V_2$), which is less than $2V_1$, where both the devices can individually withstand V_1). Moreover, the different response-time causes non-simultaneous switching (due to individual device characteristics and junction temperature). Also, a large voltage drop appears across a particular device which responds slowly and which is yet to conduct. It is the device with maximum turn-on time. For this purpose, an external voltage equalizing network and special triggering or gate drive circuits are required for simultaneous switching of all the devices in a string.



(a) Two series connected devices (SCR) in forward blocking condition



(b) A static equalizing circuit for diodes and SCR

(c) Strings of static and dynamic voltage equalizing circuits for diodes and SCR.

Figure 2.19 Series connection of devices (diodes and SCR).

Static voltage equalization To force voltage sharing equally at steady-state, a suitable resistance (R) is connected across each device, as shown in Fig. 2.19b. This arrangement is called the *static equalizing circuit*. The magnitude of these resistances are kept as high as possible to reduce I^2R loss in them. Manufacturers normally specify only the maximum leakage or blocking current (I_b). For the worst case, I_b through the device which shares the maximum voltage will be almost zero. Let only the first device, D_1 shares the maximum blocking voltage (V_{D1}), and the other devices symmetrically support the remaining voltage, equally. Then V_{b2}, V_{b3}, ..., V_{bn} are equal. Therefore,

$$V_{b(max)} = V_{b1} \tag{2.17}$$

$$V_{b2} = V_{b3} = \cdots = V_{bn} \tag{2.18}$$

$$I_{b2} = I_{b3} = \cdots = I_{bn} \tag{2.19}$$

$$I_{R2} = I_{R3} = \cdots = I_{Rn} \tag{2.20}$$

where I_{R1}, I_{R2}, ..., I_{Rn} are current through each resistance R. Also, the device with a maximum blocking voltage, offers maximum internal resistance. Therefore, I_{b1}, the blocking current through the device, is a minimum. Then,

$$I_{b1} = I_{b(min)} < I_{b2} \quad \text{and} \quad I_{R1} > I_{R2} \tag{2.21}$$

Now, the total current I, in series which is given by,

$$I = I_{b(min)} + I_{R1} = I_{b2} + I_{R2} \tag{2.22}$$

Therefore,

$$I_{b2} - I_{b(min)} = I_{R1} - I_{R2} \tag{2.23}$$

or

$$\Delta I_b = I_{R1} - I_{R2} \tag{2.24}$$

where $\Delta I_b = I_{b2} - I_{b(min)}$, the difference of maximum and minimum leakage current of the devices during blocking conditions.

Total voltage drop across all n devices of the string is

$$V = V_{b(max)} + (n-1)V_{b2} \tag{2.25}$$

$$= V_{b1} + (n-1)RI_{R2} = V_{b1} + (n-1)R\,(I_{R1} - \Delta I_b) \tag{2.26}$$

$$= V_{b1} + (n-1)V_{b1} - (n-1)R\Delta I_b \tag{2.27}$$

or

$$R = \frac{nV_{b1} - V}{(n-1)\,\Delta I_b} \tag{2.28}$$

In general, manufacturers specify the maximum value of I_b (i.e. $I_{b(max)} = I_{b2}$) and not ΔI_b for both forward and reverse blocking conditions. In such cases, $I_{b(min)}$ or I_{b1} can be neglected. Otherwise, these values can be determined experimentally at maximum rated junction temperature and rated voltage for $I_{b(max)}$. Similarly, for $I_{b(min)}$, test can be conducted at 25°C and at the rated voltage.

The power loss in R corresponds to the rms voltage (V_R) across it. This voltage corresponds to the blocking period of the device. Thus the power loss in the resistances are given by

$$P_R = \frac{V_R^2}{R} \tag{2.29}$$

The performance of an equalization circuit varies with the devices used. In case of transistors (power BJT/MOSFET/IGBT), the equalization circuit has to share the forward blocking voltage only (v_{CE} or v_{DS}) during off-period. In case of diodes, only reverse-blocking voltage is to be shared. However, for thyristors, both forward-blocking and reverse-blocking voltages have to be shared. A derating factor is normally used to increase the reliability of series string. The *series-derating factor* is defined as

$$\text{SDRF} = \frac{1 - V}{nV_{b(max)}} \tag{2.30}$$

where $V_{b(max)}$ is the maximum allowable blocking voltage (e.g., V_{CEO} (sustaining value) for transistors, V_{RRM} or PIV for diodes, and V_{DRM} and V_{RRM} for SCR).

Transient or dynamic voltage equalization At a very low frequency and at the steady-state, the static equalization circuit is sufficient to protect the individual device against over-voltage. The

turn-on and turn-off characteristics of individual devices of same rating vary. The variation in turn-on delay (time) of thyristors (also transistors) can be reduced by triggering/gate drive signal. For this purpose, a high (maximum voltage/current) magnitude and very small rise time (hard drive with sharp pulse) signal is required. During turning-on, the device with maximum turn-on time (delayed turn-on) has to bear the full supply voltage. Thus, it could lead to destruction of the device (when voltage drop exceeds the maximum forward blocking voltage of the device). Similarly, during turning-off, all devices with least reverse-recovery period (t_{rr}) recover first and support the highest transient voltage (Fig. 2.20)

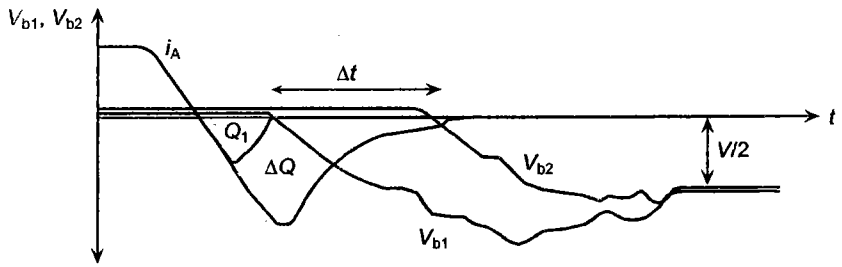


Figure 2.20 Voltage and current during turn-off of mismatched series thyristor string.

To equalize the voltage distribution, capacitors are connected across each element. During turning-off when one device recovers, the flow of reverse current stops through it. The capacitor provides a bypass path for the reverse current of the string (for thyristors and diodes). Also due to the capacitor in parallel with the device, voltage across the recovered device does not build up quickly to a dangerously high level. Thus other devices (slower devices in the series string) recover and support the supply voltage, V. A resistance is connected in series with capacitor, to limit the discharging current of capacitor through the device (thyristor and transistor) at turn-on. The RC or polarized RC snubber circuits used for *dv/dt* protection, also serve this purpose, as shown in Figs. 2.14c and 2.14d. A polarized ac snubber circuit is used to reduce delay period (RC) by shorting the resistance through a diode. It helps in forward blocking state or during turn-on. It is more suitable for transistors which has to experience only unidirectional supply voltage.

The unbalance of voltage in the string occurs both during turning-on and turning-off. Turn-on is quick for most of the power semiconductor devices (few microseconds). While turn-off may take a few microseconds to a few hundred microseconds. Therefore, the maximum imbalance of voltage occurs for considerable period during turn-off. It appears due to dissimilar reverse recovery i-v (dynamic) characteristics of the devices in a string (Fig. 2.20).

Let the worst case assumption for the analysis, i.e. the maximum unbalance in the voltage will occur when one device (T_1) recovers, while all other devices, T_2 to T_n are slow. Let all the other devices have identical reverse-recovery characteristics. Also, for the sake of simplicity, let us consider that only capacitor is connected in parallel instead of R and C for dynamic equalization. If V_{b1} and V_{b2} are the blocking voltage of fast and slow devices, respectively, then the total voltage is the sum of the recovered device (one) and slow devices ($n - 1$). Then the supply voltage is given by

$$V = V_{fast} + (n - 1)V_{slow} \tag{2.31}$$

$$V = V_{b1} + (n - 1)V_{b2} \tag{2.32}$$

Now, the voltage build up across the capacitor of T_1 during Δt depends upon the difference of charge, $\Delta Q = Q_2 - Q_1$, because T_1 is now recovered and the reverse-recovery current of other slow devices flows through this capacitor only. Thus voltage across each slow device (V_{b2}), is given by

$$V_{b2} = V_{b1} - \Delta V \quad \text{and} \quad V_{b2} = V_{b1} - \frac{\Delta Q}{C} \tag{2.33}$$

Also,

$$V = V_{b1} + (n-1)\left(V_{b1} - \frac{\Delta Q}{C}\right) \tag{2.34}$$

Therefore,

$$C = \frac{(n-1)\Delta Q}{nV_{b1} - V} \tag{2.35}$$

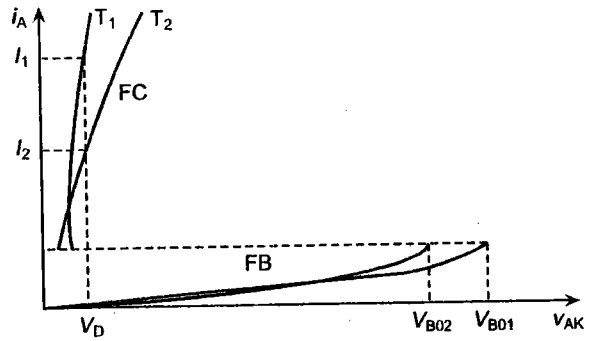
Normally, manufacturers specify maximum reverse recovery charge Q_2 (not Q_1). We may assume, $Q_1 = 0$, then $\Delta Q = Q_{max} = Q_2$. If V_{b1} is maximum allowable blocking voltage, then C can be found. Moreover, for the worst case and lower tolerance of the capacitor, the minimum sharing capacitance requirement is

$$C = \frac{(n-1)Q_2}{(nV_{b1} - V)(1 - K)} = \frac{(n-1)Q_{max}}{[nV_{b(max)} - V](n - K)} \tag{2.36}$$

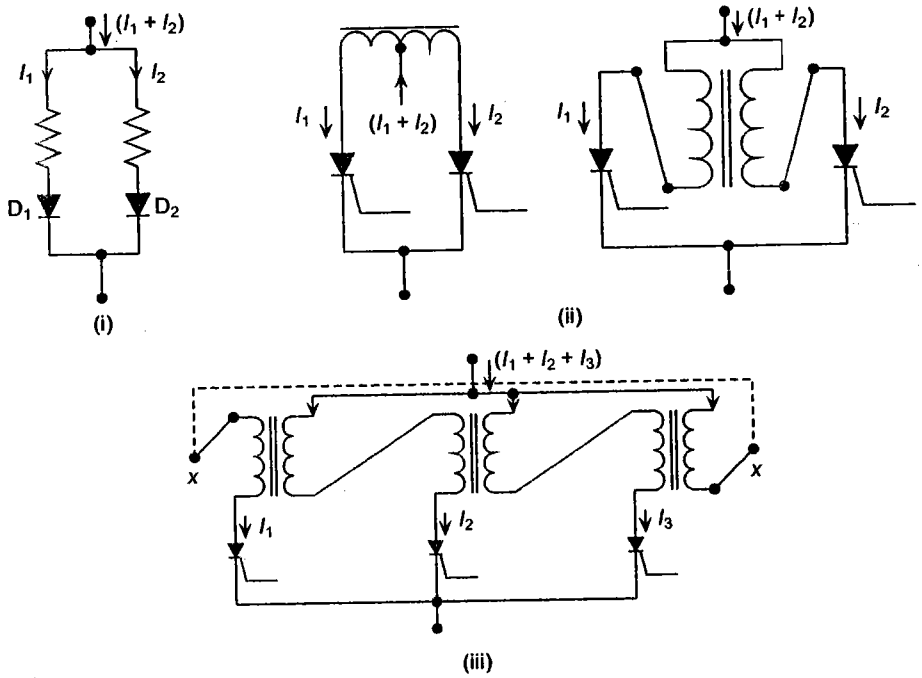
where K is the capacitor tolerance and $V_{b(max)}$ is maximum permissible device voltage (during turning-off). Sometimes, a low value inductor (with full rated current handling capability) is also connected in series with the string. It provides transient turn-on protection in addition to *di/dt* protection. The inductor supports the main voltage, during the transient condition of turn-on process of all the devices of the string, till the switching of first to the last (or slow) device is accomplished.

PARALLEL CONNECTIONS

The devices are connected in parallel to achieve a higher current rating or lower on-state voltage drop. It improves the cooling condition. Sometimes there is saving in cost (may be due to smaller or low rating cheaper devices). For example, three 35-A, 800-V SCR are quite cheaper than one 100-A, 800-V SCR. Devices connected in parallel should have equal voltage drop during on-state to share the current equally. This is the main design consideration. A slight mismatch in on-state characteristics may cause a large discrepancy in the current share. It may cause heating of a particular device with higher current share. The semiconductor device has normally negative temperature-coefficient of resistance (except MOSFET). Therefore, on-state resistance decrement will cause more current to flow through it, eventually leading to thermal runaway and device destruction. This effect is less severe in diodes because diode characteristics are more uniform than other devices. Since MOSFET has positive temperature-coefficient of resistance, it can be easily connected in parallel (in comparison to other devices). The forward conduction current through two mismatched devices (e.g. thyristors) is shown in Fig. 2.21a. Due to mismatch characteristic, the total current ($I_1 + I_2$) is less than $2I_1$. Therefore, the current handling capability reduces (instead of $2I_1$). There are two types of current equalization methods: for matched devices and external forced current sharing.



(a) Current shared by two mismatched parallel devices (SCR)



(b) External forced current sharing using: (i) resistance, (ii) reactors and (iii) reactors for many devices

Figure 2.21 Transient or dynamic voltage equalization.

For matched devices In general, matched devices are available for parallel operation. The current rating of the combined unit is reduced to increase the reliability of the arrangement. The *parallel-derating factor* is defined as

$$\text{PDRF} = 1 - \frac{I_T}{nI_{max}} \tag{2.37}$$

where I_T = total current through the parallel arrangement ($I_1 + I_2 + \cdots + I_n$), n = number of parallel devices and I_{max} = maximum current rating of each device.

During turning-off due to mismatched device characteristics, these devices do not share voltage equally, as shown in Fig. 2.21a. Devices are usually mounted on same heatsink to maintain equal junction temperature, which minimizes current unbalance. A hard drive gate signal helps reducing turning on dissimilarities of the devices. Otherwise, it may cause a particular device to conduct first, resulting the total current to flow through this device only leading to its damage due to overloading. Actually, a hard drive gate signal (sharp pulse of maximum gate voltage) reduces turn-on time. Moreover, when there is fluctuation in the load current during a conduction period, a particular device current may be less than the holding level. Thus, it will be commutated and the increased load current has to be shared by the remaining devices only. This type of phenomenon occurs in converters for DC motor drive. Thus, it is desirable to supply the gate trigger signal to each device for whole conduction period.

External forced current sharing For unmatched devices to be connected in parallel, this arrangement is required, as shown in Fig. 2.21b. In case of a resistance balancing arrangement, the power loss is significantly high because each resistance has to carry full load current (I^2R loss). Although coupled reactors can be used instead of resistances, this arrangement is efficient but costly. In this arrangement, if the current I_1 increases and it is higher than I_2, more voltage (proportional to unbalance in current) will induce across L_1 to oppose current flow through it. Thus more current will flow through L_2. This is most effective ac current equalizing circuit. However, the core should not saturate at the rated current. Thus the core should be designed for the flux density less than knee point, or an air core reactor should be used. This arrangement can be used for any number of devices.

2.4.14 Commutation of SCR

A conducting thyristor can be turned off successfully by (i) the application of a reversed voltage across it and (ii) reducing the anode current below the holding current (I_H) level. The process of turning off the thyristor is called *commutation*. There are three types of commutation:

Natural commutation When i_A becomes zero or attempts to reverse due to reversed or negative supply voltage across anode and cathode, the thyristor turns off. This happens with the ac-supply voltage, where the polarity of the supply voltage changes twice in each cycle. This process is called *natural* commutation.

Load commutation If resonating load current falls below the holding current level (e.g. in case of an under-damped RLC dc circuit), a thyristor turns off. This is called *load* commutation.

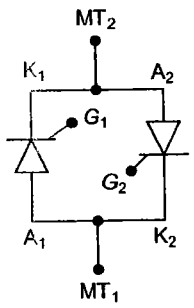
Forced commutation If i_A does not reduce to zero, the above two methods do not apply. The thyristor can be turned off by interrupting or forcing i_A to fall below I_H using an external circuit. This is accomplished by applying a reverse voltage across anode and cathode and forcing i_A to fall below I_H. This is called *forced* commutation.

2.5 OTHER THYRISTORS

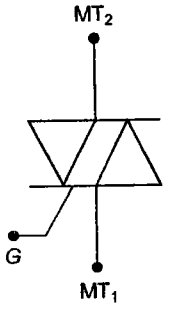
There are large number of devices that belong to the thyristor family. Most important types are being discussed here.

2.5.1 TRIAC

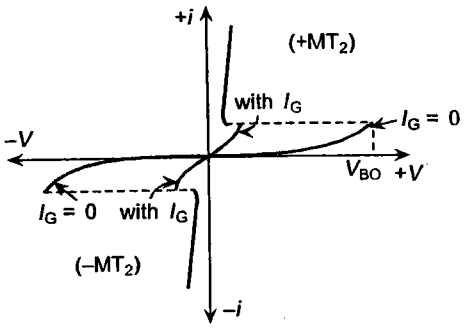
Functionally, a *triac* is an integration of a pair of converter-grade SCR connected in anti-parallel mode (Fig. 2.22a). The structure and switching mechanism is slightly different from SCR.



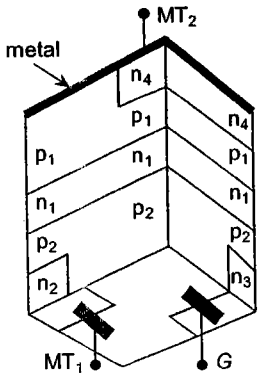
(i) Equivalent of triac



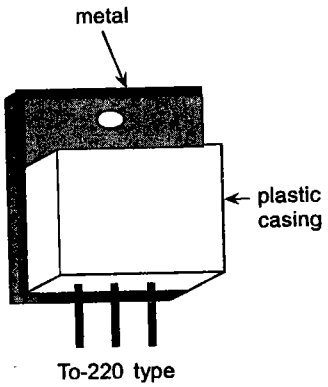
(ii) Symbol

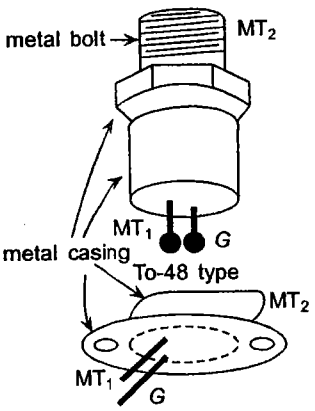


(iii) i-v characteristics



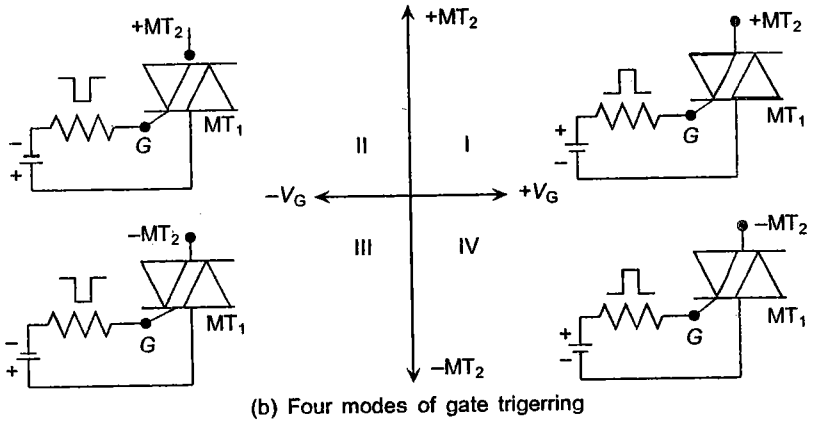
(iv) Triac structures (two SCRs p_1-n_1-p_2-n_2 and p_2-n_1-p_1-n_4)





(v) Different casings

(a) Symbol, package and characteristics



(b) Four modes of gate trigerring

Figure 2.22 Details of a triac.

Moreover, an equivalent two anti-parallel SCR are more robust than a triac. However switching a triac is simpler than two anti-parallel SCR. The triac conducts in both the directions through the main terminals (MT_1 and MT_2), unlike all other power semiconductor devices. Therefore, in general, it is used to control ac power. The name triac is derived from *triode* and *ac*. There are four mode of switching of a triac. This three-terminal device can be triggered into conduction in both positive-half and negative-half cycles of the supply voltage by applying either positive or negative gate signal (Fig. 2.22b). Gate is less sensitive and sensitivity varies in different modes. Its switching turn-off time is more and *dv/dt* rating is less than SCR. Thus it is not suitable for inductive and high-frequency load circuits. Normally, it is used in an ac circuit for high power factor loads and operated at mains frequency (50 or 60 Hz) or frequency below 400 Hz. However, the cost of triac is less than that of two SCR. Moreover, it is triggered by both positive as well as negative gate signal (I_G or V_G).

2.5.2 Light Activated SCR (LASCR)

A pulse or beam of light, guided by a fibre-optical cable is used to trigger an LASCR. The application of direct or photon energy ($E = h\nu$) on the silicon wafer near the gate layers (n_1, p_2) generate electron-hole pairs. The minority carriers cross the junction J_2, get accelerated with energy (eV_{AK}) and strike the covalent bonds of silicon atoms produce more electron-hole pairs. The process continues till avalanche or conduction takes place.

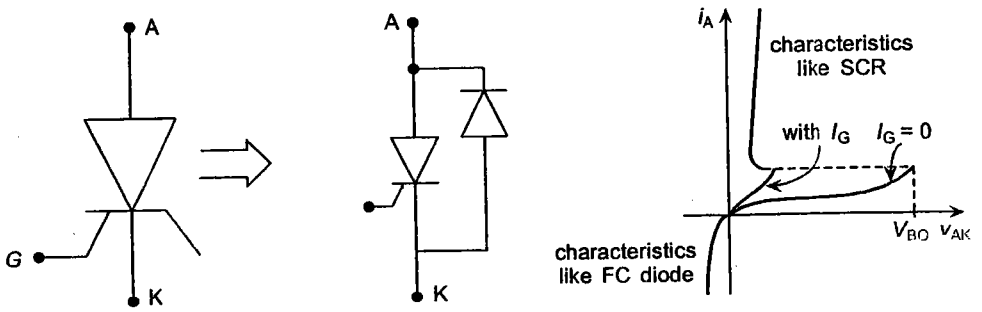
In general, an LASCR is used for high voltage (HV) applications, e.g. HVdc transmission or static VAR-compensation systems (SVS). It provides complete electrical isolation from the power circuit, where thyristors are connected in series and each of them float at different HV levels. A very low-power light source is enough to trigger the device. A 4-kV, 3-kA LASCR can be triggered by a 5-milli-Watt (mW) light source.

2.5.3 Reverse Conducting Thyristor (RCT)

An RCT is an equivalent of a fast switching SCR with a fast-recovery anti-parallel diode, integrated in the same wafer (Fig. 2.23a). Thus it allows a reverse current to flow, in case of an inductive load. Since no diode is required to be connected externally, it minimizes interconnecting lead inductance. Thus stray inductance reduces which is important for high frequency applications. It reduces numbers of devices to be used in chopper and inverter circuits, where the diode is connected with each SCR.

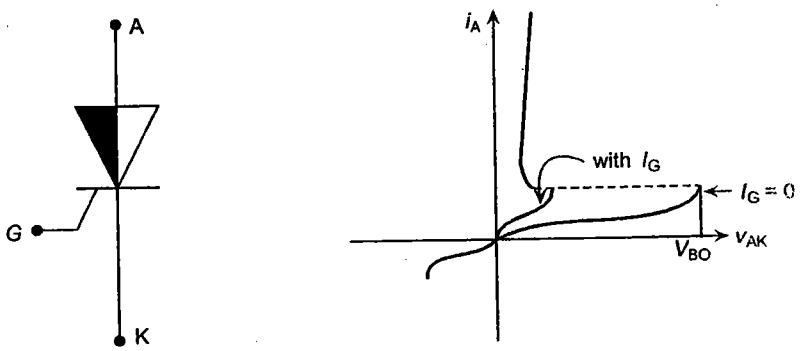
2.5.4 Asymmetrical SCR (ASCR)

As the name indicates, ASCR has a very low reverse-voltage blocking capability in comparison to the forward blocking capability. Higher forward-blocking voltage, low on-state drop and faster turn-off characteristics are obtained by sacrificing the reverse-blocking capability. This is done by control of doping or impurity-concentration profile. As discussed in Section 2.4.1, for fast turn-off, width of n_1 is reduced (e.g. 0.24 mm to 0.16 mm) and doping layer of n_1 adjacent to J_1 is increased from 10^{14} to 10^{17} atoms/cc. The breakdown voltage (V_{BD}) and the reverse-repetitive maximum voltage (V_{RRM}) are few tens of volts while the forward breakover voltage (V_{BO}) and forward-repetitive maximum voltage (V_{DRM}) may be several hundred volt (Fig. 2.23b).



(i) Symbol of RCT (ii) Equivalent circuit (iii) Characteristics

(a) Detail of an RCT



(i) Symbol of ASCR (ii) Characteristics

(b) Details of an ASCR

Figure 2.23 Symbols and characteristics.

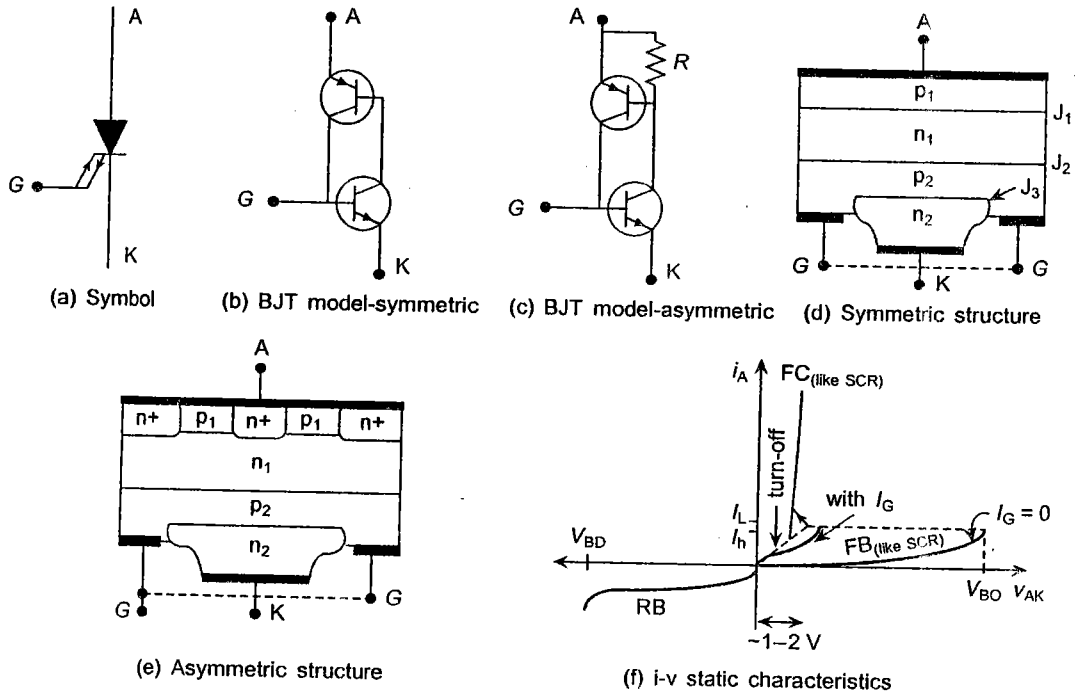
2.6 GATE COMMUTATION DEVICES

Here those devices are discussed, whose both turn-on and turn-off are controlled by the gate/base voltage/current signal. Normally, a very low power gate drive circuits are required for all these devices (except for GTO).

2.6.1 Gate Turn-off Thyristors (GTO)

A gate turn-off thyristor (GTO) is a member of the thyristor family. It has three terminals: anode (A), cathode (K) and gate (*G*). It can be turned-on by a positive gate pulse (like an SCR) and turned-off by a high-power negative gate pulse. Since no separate forced commutation circuit is required (as in case of an SCR), cost, size (volume) and weight of controllers reduce, whereas the efficiency improves. It has high frequency and high power-handling capability but requires a large gate power source (negative) to turn it off. For example, 2000-A anode current requires a negative current pulse of 500-A, i.e. the required I_G is 1/4 of I_A.

A GTO is normally manufactured with two configurations (Fig. 2.24). It can withstand both positive and negative voltage (v_{AK}) at the blocking condition. An asymmetrical GTO is like a reverse-conducting SCR (RCT), where a reverse-parallel diode is integrated on the same silicon wafer of GTO. Such GTO are used, where they need not to experience or block a negative voltage (e.g. a GTO based dc-to-ac inverter).



(a) Symbol (b) BJT model-symmetric (c) BJT model-asymmetric (d) Symmetric structure

(e) Asymmetric structure (f) i-v static characteristics

Figure 2.24 GTO symbol, structures and i-v characteristics.

The basic structure of a GTO is similar to a thyristor (a four-layer pnpn SCR). A GTO is turned on by forward biasing the gate-cathode junction and turned off by reverse biasing the same junction (contrary to SCR). Although the symmetric structure is common, an asymmetric structure is also used by providing base-emitter shorts. It reduces pnp transistor gain (transistor model) and both turn-off and temperature properties are enhanced. However, it is achieved at the cost of the reverse-blocking capability of the device. The turn-off current gain of a GTO (β) is the ratio of anode current (i_A) and the reverse gate current ($-I_G$) at turn-off. The typical value of β is about 5.

The turn-on mechanism is similar to that of an SCR. However, the gate of a GTO is purposely made insensitive compared to the gate of an SCR. A small but continuous positive gate current is usually supplied during the entire desired on-period, to ensure conduction even at a low-anode current. A considerable magnitude of the gate current (negative, low-energy) is required for turn-off. The turn-off time reduces with increase in the negative gate current. However the rate of rise of negative gate-current (di_G/dt) must be held below the rated value specified by the manufacturer. It has similar effect on GTO as that of di_A/dt on a thyristor during turn-on. An inductor is normally used in the gate drive circuit to limit di_G/dt. A snubber circuit is must for a GTO. The turn-on of a GTO is faster than a thyristor due to many cathode elements. It

increases initial turn-on area unlike the thyristors, where conduction starts adjacent to gate only (as discussed earlier in *di/dt* limitation of thyristors). Therefore, a GTO has higher *di/dt* capability.

For turn-off operation, a high-negative current pulse is supplied to the gate using a driver circuit connected between the gate and cathode. It makes the gate-cathode pn-junction reverse-biased by extracting the holes from the gate p-layer. It squeezes the conduction area and the anode current forms a high-current-density lengthy path (filament). A higher negative gate voltage extinguishes the current filament (with high-resistance path) quickly. It may otherwise cause a local hot spot leading to device failure.

2.6.2 Power Bipolar-junction Transistors (Power BJT)

A bipolar-junction transistor (BJT) is a minority carrier device. It has three terminals, namely, emitter (E), collector (C) and base (B). For small-signal processing of electronic circuits, both npn and pnp type transistors are available. However, to handle large-power of power electronic circuits, npn power transistors are normally used in common-emitter configuration. Due to higher mobility of electron than holes, an npn transistor is faster than its counterpart pnp transistor. Since it is used for switching purposes (not as an amplifier), it operates either in saturation region or cut-off region. It minimizes the losses in the device ($v_{CE} \times I_C$). The device comes into conduction mode (saturation region), when a positive base current (i_B) is supplied. The voltage across the collector and the emitter terminal (v_{CE}) collapses and the collector current (i_C) flows from collector to emitter. The current gain of the device (β or $h_{fe} = I_C/I_B$) varies between 5 and 10 while v_{CE} at saturation is about 1 to 2 volts. In general, β increases with i_C and the collector supply voltage (V_{CC}). However, β falls at both high and low level of i_C. In order to bring the conducting device from saturation-state to cut-off state, the excess minority carriers in the base are removed by the reverse or negative base current. The period from the end of positive base (switching) current until the device enters linear (active) region is called *saturation time*. The saturation time increases the turn-off-switching time. Therefore, a power BJT, which is used for switching applications (i.e. either operate in saturation region or cut-off region), may be held in quasi-saturation region (on the verge of saturation) by reduced i_B. Although on-state losses slightly increases at this condition but the saturation time hence the switching turn-off time reduces. At the forward-blocking condition, the reverse-biased collector junction supports the applied voltage and a wide depletion layer or space charge layer (SCL) develops across it. If the supply voltage (V_{CC}) is increased, SCL becomes wide and it penetrates deep into the base layer to overlap with emitter-base SCL (forward biased). The overlapping of SCL is called *punch-through*. At this condition, the collector junction voltage breakdown occurs due to avalanche multiplication of carriers (like V_{BO} of SCR), created by a high electric field at the collector junction. This is called *first* or *primary breakdown*. The first breakdown is the limit of V_{CE} voltage that BJT can sustain when it carries a high collector current. If the junction temperature is within the safe limit, this breakdown is not destructive. However, if a hot-spot develops because of a non-uniform current-density distribution, second breakdown occurs. There appears a large drop in V_{CE} for the high collector current. It results in high power loss in the device leading to silicon crystal melting and irreparable damage. In general, the phenomenon of the second breakdown is related to BJT only. Various details of the device are shown in Fig. 2.25. The second breakdown can be avoided by control of power dissipation, control of rapid change in base current at turn-off, use of snubber circuit and keeping switching trajectory (instantaneous voltage and current) within the safe-operating area (SOA) of the device. Two SOA namely, forward-bias SOA (FBSOA) and reverse-biased SOA (RBSOA), are used for this purpose. A SOA is confined by second breakdown limit,

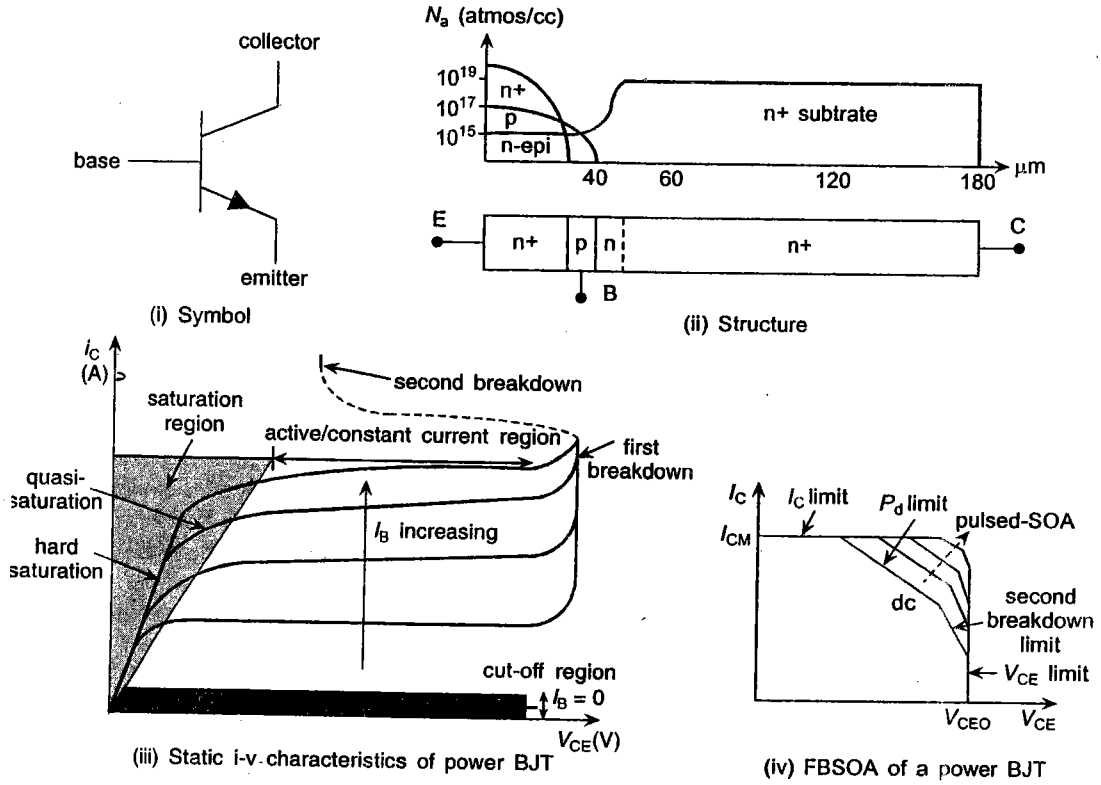


Figure 2.25 Various details of a power BJT (npn-type).

rated or maximum I_C (I_{CM}) and maximum thermal dissipation. Moreover, inductive loads cause more power dissipation of the device than in case of a resistive load. Also, in case of pulsed i_C the limit of SOA increases, as there exists a cooling or idle period in between each on-condition. RBSOA is related with the negative i_B as well as v_{EB}. Below the V_{CEO} level, RBSOA is limited by the maximum i_C (rated value) only. However, above the V_{CEO} level, i_C must be under control, which depends upon v_{EB}.

Since the current gain of power transistors are limited (5–10), they are also manufactured in pairs, in a single chip or casing. The emitter current of the first transistor drives the second transistor. Therefore, the overall current gain increases. This arrangement is called *monolithic darlington* (MD).

2.6.3 Metal-oxide Semiconductor Field-effect Transistors (MOSFET)

The metal-oxide semiconductor field-effect transistor (MOSFET) is a majority carrier device. It has three terminals: drain (D), source (S) and gate (*G*). Since mobility of majority carriers is faster than the minority carriers and due to absence of minority carrier stored base charge (common in BJT), the storage time (which reduces switching speed) is absent in MOSFET. Therefore, switching of the MOSFET is ultra faster than a BJT. Moreover, higher switching speed allows efficient switching at a high speed which reduces cost, size and weight of the MOSFET based controllers. It is a voltage-

controlled current-source device and requires a continuous-gate voltage signal to maintain its conduction. A gate current flows only during the switching transition period for charging and discharging of the gate capacitors. Therefore, a simple, low power, gate drive circuit is required for turn-on and turn-off operations. The MOSFET can easily be paralleled due to its positive temperature-coefficient of the device resistance. Due to the positive temperature coefficient, the on-state resistance of the high-current-carrying device, becomes high and it forces more current to flow through another low-current carrying device, due to low on-state resistance. In this way, a uniform current distribution is maintained.

The power MOSFET is evolved from the conventional small-signal (signal processing) MOSFET used in low-power electronics circuits. The conventional small-signal MOSFET had long structure resulting in low current capability, low reverse-resistance and more on-state conduction loss (Fig. 2.26a). In case of a power MOSFET, a lateral double-diffused structure (DMOS) was used for high voltage and current rating (Fig. 2.26b). This structure offered a very short channel length, high package density and low on-state resistance hence low on-state losses. The DMOS technology was improved further and a vertical structure was adopted. In this case, drain terminal is placed at bottom of the wafer to increase the channel package density. Initially, V-shape structure (VMOS) was used, where deep V-shape surface was developed (etched) for the gate terminal. Finally, vertical DMOS structure, shown in Fig. 2.26c, was used. This structure gives maximum area for both source and drain current. The gate structure (polysilicon) is sandwiched between two silicon oxide layers (SiO_2) and the source metal covers the entire active

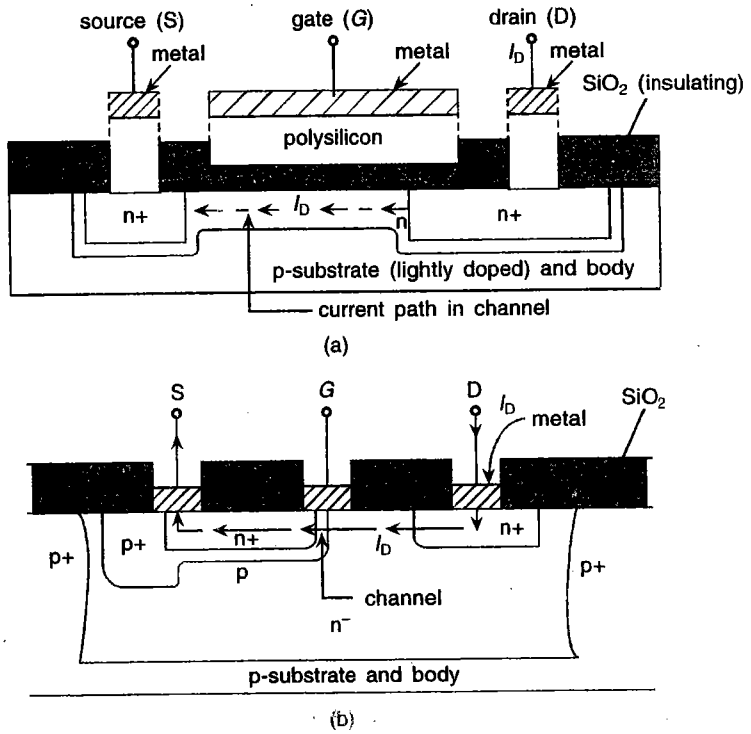


Figure 2.26 (*Cont.*)

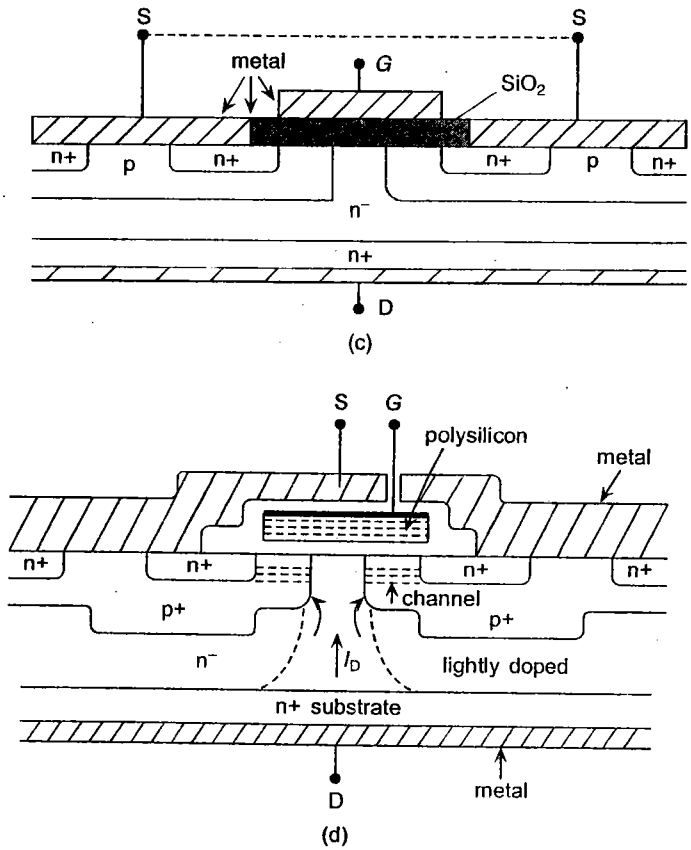


Figure 2.26 Evolution of MOS structure.

area. Thus on-state resistance, hence on-state losses reduce. Practically, all power MOSFET is being manufactured with this structure (Fig. 2.26d). However, minor modifications are often done to improve device capabilities. The pattern of gate and source (well structure), if viewed from the top, appears as rectangular, hexagonal (HEXFET-MOSFET of International Rectifiers) or T-shape (TMOS-MOSFET of Motorola).

For small signals and low-power applications, all the four type MOSFETs are used. However for power applications, in general, an n-channel enhancement type power MOSFET is used. Since MOSFET is a majority carrier device, the mobility of electron is faster than holes. Moreover, the on-state resistance $r_{DS(on)}$ is inversely proportional to the carrier mobility. Therefore, $r_{DS(on)}$ of the p-channel MOSFET is approximately 2.5 to 3 times that of a similar n-channel MOSFET of the same die size. When both p-type and n-type MOSFETs are used together, in order to have matched complementary on-characteristics, larger die (size) is required for a p-channel MOSFET for the same $r_{DS(on)}$ and the same breakdown voltage. Thus the cost and the device capacitances of a p-channel MOSFET shall be higher. Both drain and source are made of heavily doped n-type silicon and the body or substrate (p-type) is lightly doped. The gate is a conductive plate, normally made of polysilicon, which is electrically isolated from the rest of the device by an oxide insulator. No current flows between D and S as they form n^+p and pn^+ structure (two back-to-back diodes). Let

both S and D are kept at ground potential and a positive voltage is applied at the gate. It causes concentration of positive charges at the gate (plate) and negative charge just beneath the insulation, as holes flow away (action of a parallel plate capacitor). Thus SCL grows into the silicon. When the gate voltage is increased, the concentration of electron increases and forms a thin layer of effectively n-type silicon, called a *channel*. When this condition occurs there is no longer n^+p and pn^+ junction between D and S, instead it is an n^+nn^+ structure that acts as a semiconductor resistor (very large value) and permits the current (i_D) to flow. If v_{GS} is kept on increasing, a condition comes ($v_{GS} = V_T$), when the electron concentration becomes equal to the original hole concentration (of p-type). At this condition, the resistance of the channel begins to fall and it becomes a function of the gate voltage. The term, *enhancement* type refers to the channel conduction, which is enhanced by the gate voltage. The lightly doped n-type region permits the device to block a high voltage during off-condition. This region is called *extended drain* or *drift region*, it allows a long SCL due to low impurity concentration. When SCL grows due to high voltage, it pinches-off (depletes) the region between p-well (as discussed in the beginning).

In the vertical structure, p-type material is connected with the source and it is called *body region* of the device. The channel of the power MOSFET forms on the surface of the body just beneath the gate (Fig. 2.26d). The lightly doped n-type drain region (extended or drift region) allows growth of a long SCL, which increases the device voltage-withstand capability (blocking). On application of voltage across D and S, SCL grows. It depletes or pinches off the p-type region. When a positive gate voltage is applied, it induces an inversion layer in the channel region of the drain and a current (i_D) begins to flow. The *on-state resistance* of the device is defined as the total resistance encountered by the drain current, between source and drain terminals. It includes the resistances of the inversion channel, gate-drain accumulation region, the junction FET-pinch region and the highly doped drain region. Moreover, parasitic capacitances exit in-between p^+ and n^- layers (C_{ds}), source (metal and n^+) and polysilicon (C_{gs}), and polysilicon and n^- (C_{gd}), as shown in Fig. 2.27. These capacitances play an important role in switching characteristics, switching speed limitation and designing the gate drive circuits. Effects of these capacitances are discussed in detail in gate-drive circuits of power MOSFET (Chapter 4).

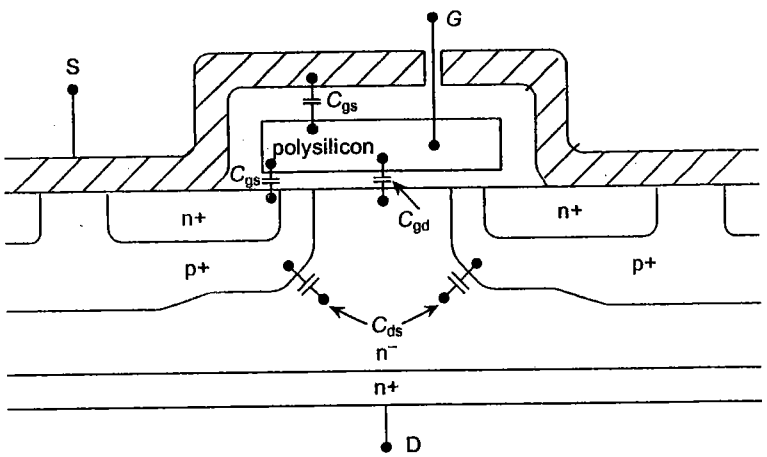
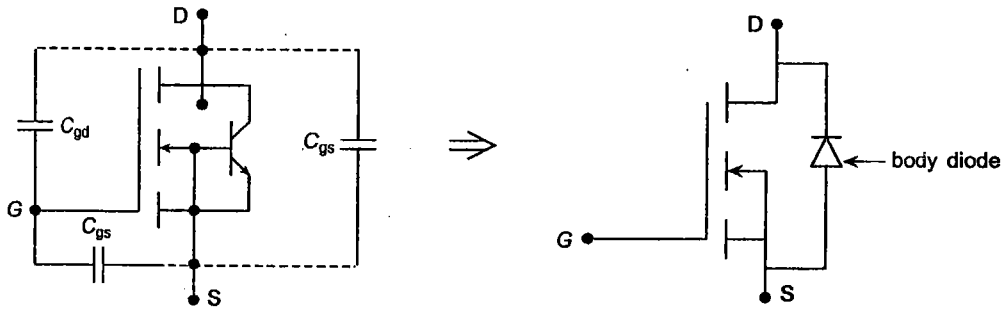


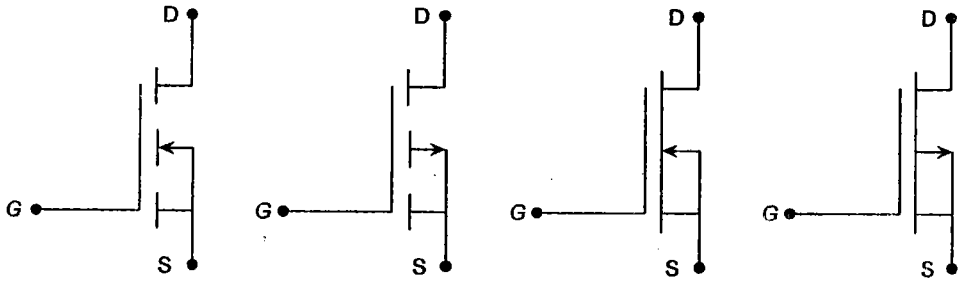
Figure 2.27 Capacitances of MOS structure.

The breakdown voltage, $V_{(BR)DSS}$, or reverse blocking voltage of power MOSFET is defined as in BJT [$V_{(BR)CES}$] related with avalanche breakdown (first breakdown), with gate and source terminals shorted. This corresponds to the condition when carriers within depletion region of reverse biased pn-junction require sufficient kinetic energy and strike with the covalent bonds of silicon atom to liberate electron-hole pairs thus generate more carriers (or cause ionization).

During fabrication of a power MOSFET, the pn-junction forms, which results in C_{ds}. Similarly C_{gs} and C_{gd} are developed due to glass insulator. If voltage exceeds, breakdown occurs and a permanent destruction of MOSFET takes place. The internal structure of a power MOSFET can be represented, as shown in Fig. 2.28a.



(a) MOSFET equivalent and symbol



(b) Symbols of different MOSFET

Figure 2.28 Details of power MOSFET.

Figure 2.28b shows the symbols of different types of power MOSFET. In enhancement type structure, no physical channel exists between heavily-doped n^+ silicons. The presence of positive voltage at the gate (v_{GS}) attracts electron from p-substrate (body). If sufficient electrons are accumulated beneath the SiO_2 layer of the gate, a virtual channel forms and conduction takes place between drain to source. Therefore, on-state device resistance $r_{DS(on)}$ depends upon this condition. For a successful and maintained conduction, v_{GS} should be greater than a threshold voltage (V_T). Its value varies between 4 and 6 V and depends upon the device temperature. However, the value of $r_{DS(on)}$ depends upon the magnitude of both v_{GS} and the drain current (I_D), as shown in Fig. 2.29. The static output characteristics of the channel enhancement type device is shown in Fig. 2.30.

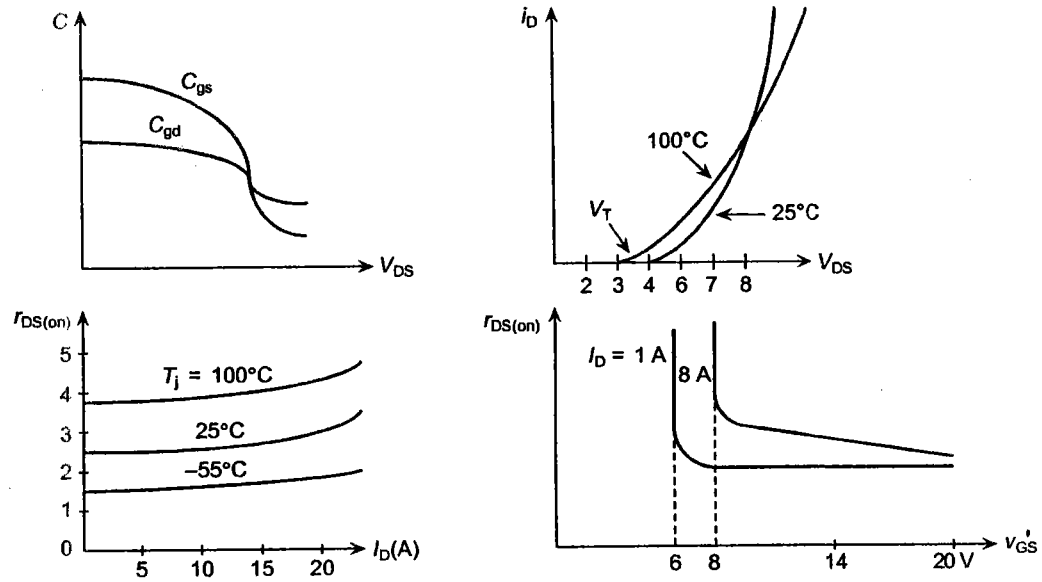


Figure 2.29 Different parameter characteristics of MOSFET.

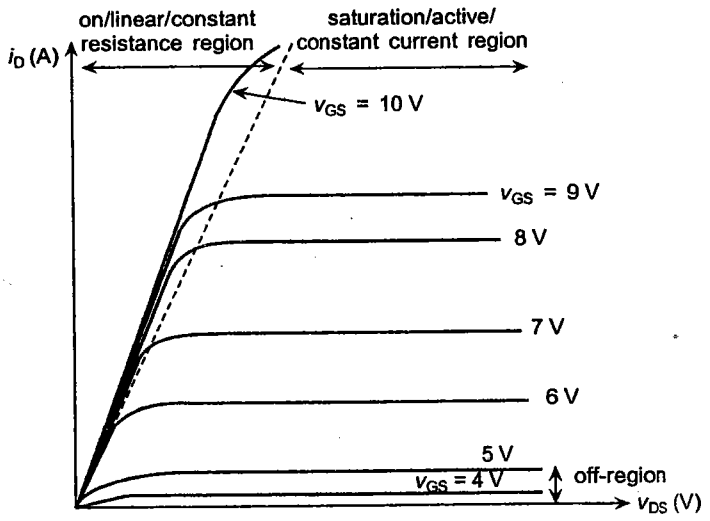


Figure 2.30 Static i-v output characteristics of MOSFET.

In case of a depletion type MOSFET, an n-channel is formed between the two heavily doped n^+ silicon layers. On application of a positive v_{GS} voltage, this channel becomes wider. Then drain-to-source resistance r_{DS} decreases and i_D flows. On the other hand, when v_{GS} is negative, some of the electrons will be repelled in the *n*-channel area and a depletion layer forms below SiO_2 layer. Thus the effective channel area becomes narrower and r_{DS} increases and I_D decreases. If v_{GS} (negative) is further increased, a condition comes when i_D becomes zero. This critical value of v_{GS} is called *pinch-off voltage* (V_P).

The physical construction of a p-type MOSFET is a replica of n-type device.

STATIC CHARACTERISTICS

There are three regions of the static characteristics, as shown in Fig. 2.30. The operating point may be either in the linear-region (triode, constant resistance region or the saturation region) or off-region (with very high r_{DS}, ideally infinite). The operating point depends upon the value of v_{DS}, as:

Linear region: $v_{DS} < v_{GS} - V_T$
Active region: $v_{DS} > v_{GS} - V_T$
Off region: $v_{DS} < V_T$

The power MOSFET operates in two regions only, i.e. the linear (or triode) region and the off-region. For switching or power electronic circuits, MOSFET is not used in the saturation or active region. Since both voltage drop and the device current are high, device losses are very high in this region. On application of the gate voltage (v_{GS} positive and greater than V_T), a channel between drain (D) and source (S) forms. After the turn-on, no gate current is required ($I_G = 0$, ideally). It is a voltage-controlled device. At both on and off conditions, the gate current requirement is almost zero. However during turn-on and turn-off conditions, the device capacitors are required to be charged and discharged, respectively. Therefore, the gate power supply should have high source and sink capabilities (of the order of 1 A).

When the MOSFET is in linear region, $r_{DS(on)}$ of the device (the resistance between D and S) behaves like a constant resistance. Therefore,

$$r_{DS(on)} = \left[\frac{\partial v_{DS(on)}}{\partial i_D}\right]_{v_{GS}=\text{constant}} \tag{2.38}$$

The on-state device loss (P_d) is given by

$$P_d = I_D^2 r_{DS(on)} \tag{2.39}$$

The value of $r_{DS(on)}$ varies from a few tens of milli-ohm to a few ohms for low-voltage and high-voltage MOSFET, respectively. Therefore $r_{DS(on)}$ of MOSFET is higher than the on-state resistance (v_{CE}/i_C) of the power BJT.

SAFE OPERATING AREAS (SOA)

The safe operating area of a device provides the maximum voltage and current limits, which the device can handle without destructive failure. There are two different safe operating areas defined for the power MOSFET: (i) the *forward biased safe operating area* (FBSOA or simply SOA) and (ii) *switching safe operating area* (SSOA). Normally, SSOA curves are used for the voltage and current limitations during turn-off. They resemble the voltage and current curves of *reverse-biased safe operating area* (RBSOA) of power BJT.

An FBSOA curve defines the limiting values of current, voltage and power dissipation, that a device can safely handles during the switching, and at on and conditions (Fig. 2.31a). The most important limiting value is the maximum v_{DS}. If a device experiences a higher voltage, even momentarily, it can be damaged permanently. Even a high magnitude, short-duration transient voltage (spikes) may be destructive for the device. Therefore, the snubber circuits are important for power MOSFET. Similarly, the device current (I_D) should not exceed the I_{Dmax} limit, even momentarily. Otherwise, the switching inrush current of transformer or induction motor etc. may damage the device.

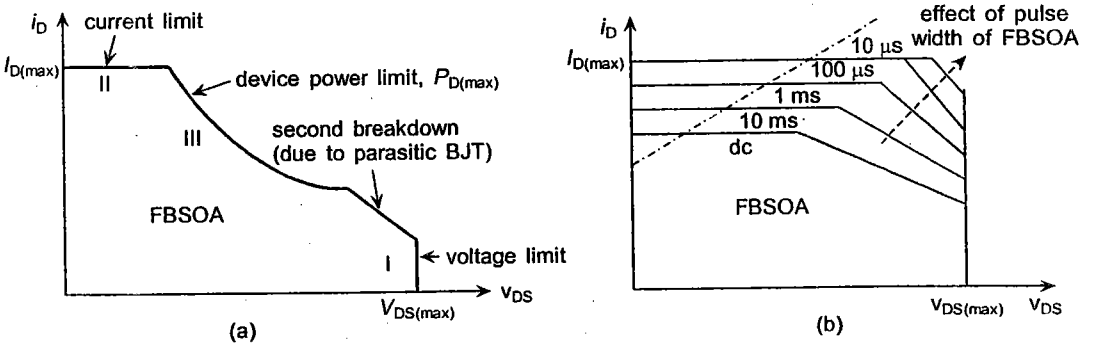


Figure 2.31 Different SOA of MOSFET.

The curve of FBSOA changes greatly for a continuous dc current and for a pulsed current (Fig. 2.31b). Similarly, at low value of v_{DS}, the allowable i_D limit reduces (below dotted lines). At blocking condition and high v_{DS}, second breakdown may occur in the device due to parasitic (inherent) npn BJT.

2.6.4 Insulated-gate Bipolar Transistors (IGBT/IGT)

Although a power BJT has good on-state conduction characteristics but its switching characteristics is inferior to a power MOSFET. It needs a high base drive current and turn-off time is considerably high. On the other hand, power MOSFET has better switching characteristics (simple, low-power gate drive, high operating-frequency, etc.), but it exhibits poor characteristics as the voltage rating goes up (above 200 V). Moreover, the conduction drop strongly depends upon the temperature and voltage rating. Also, the inherent (or body) diode of the device shows inferior reverse-recovery characteristics at high voltage and therefore switching losses increase.

Insulated-gate bipolar transistors (IGBTs) are developed to remove these drawbacks. Since it is a minority-carrier device, its switching speed is slightly inferior to that of a power MOSFET. Even then, it has many appealing features of both power BJT and MOSFET, e.g. low-conduction voltage drop, ease of drive, wide SOA, peak current capability, no turn-off saturation time, no second breakdown and ruggedness.

It is a hybrid MOS-gated turn-on/turn-off bipolar transistor that combines the attributes of MOSFET, BJT and thyristors. It has a high impedance gate (like a MOSFET), low on-state voltage drop (like a BJT) and bipolar voltage blocking capability (like a thyristor/SCR, e.g. in both half-cycles of ac supply). It is used for medium power (up to few 100 kW) and medium frequency (up to 50 kHz) power-converter applications.

The basic structure of IGBT comprises a combination of MOSFET and BJT in a monolithically integrated-darlington like connection (Fig. 2.32). It has three terminals, namely, drain (D), source (S) and gate (G), according to a MOSFET model; or emitter (E), collector (C) and gate (G), according to a BJT model. The n-channel MOSFET acts as a driver for a low forward-drop (v_{CE}/i_C) per unit area, of pnp BJT. This arrangement is also similar to a pilot SCR used for triggering of a main SCR. The turn-on time of the IGBT is same as its inherent BJT. Due to the presence of the driving MOSFET, which turns off quickly, the turn-off of an IGBT becomes faster than a BJT alone. The IGBT has a parasitic thyristor or SCR (both pnp and npn from a two-transistor model of SCR, as shown in Fig. 2.32b). Therefore, the voltage spikes (high rate of

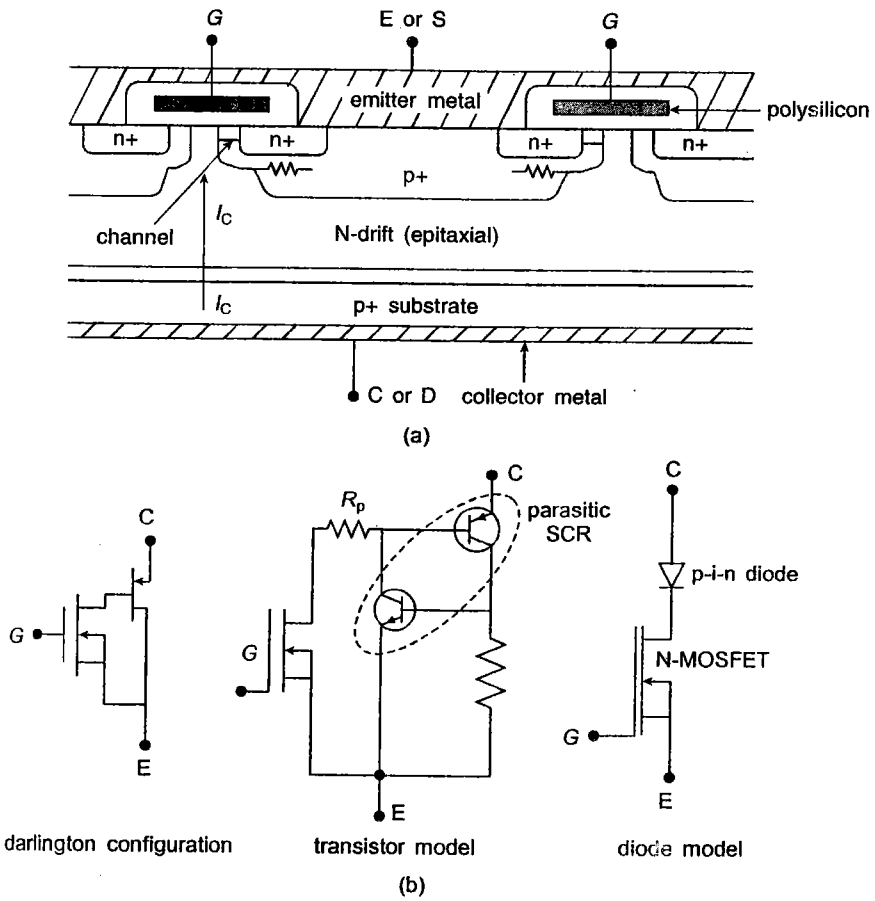
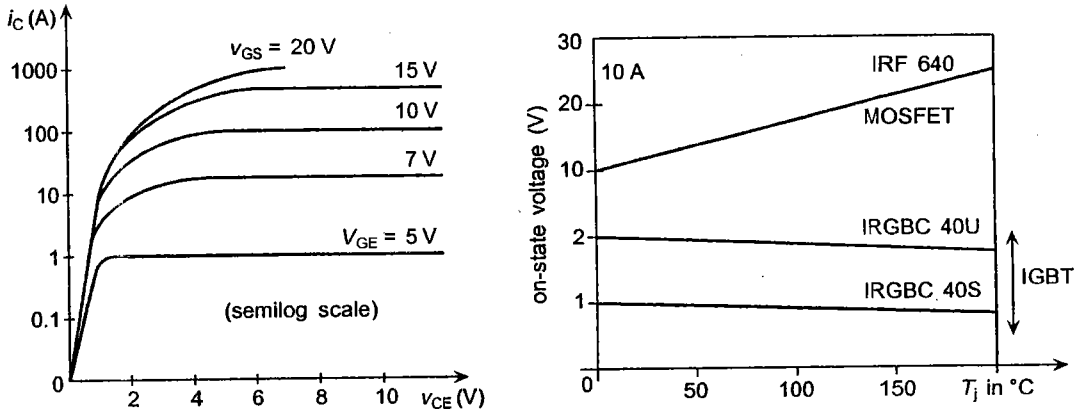


Figure 2.32 Structure of IGBT.

rise of voltage or *dv/dt*) or high device current may turn on the device. When this happens, it cannot be turned off from the gate (like an SCR). This maximum device current limit [$I_{C(max)}$] decreases with increase in temperature.

The basic structure of an n-channel IGBT is similar to that of a double diffused (DMOS) power MOSFET except an additional p^+ substrate layer between wide n^- drift region and collector or drain metal. These two semiconductor layers form a pn-junction. This allows only positive current to enter the collector terminals. Other layers form two pnp, npn and MOS transistors, as shown in Fig. 2.32a. The static i-v characteristics of IGBT are shown in Fig. 2.33a, which are similar to that of power MOSFET (Fig. 2.30). Except for p^+ substrate, the silicon cross-section of an IGBT is almost identical to that of a power MOSFET. Both devices share a similar polysilicon gate structure and p wells with n^+ source (or emitter) contacts, like MOSFET. The n-type material under the p wells is sized in thickness and resistivity to withstand the rated device voltage (full-rated value). In spite of these physical similarities, the behaviour of the device (IGBT) is closer to a BJT than to that of a power MOSFET. This is due to the presence of a p^+ substrate, which forms a pn-junction (p^+ substrate and n^- drift).



(a) Static i-v characteristics of IGBT

(b) On-state drop of MOSFET and IGBT of same die size

Figure 2.33 Comparative voltage drop with respect to temperature of IGBT and MOSFET.

When the device is properly biased ($V_C > v_E$) and a positive gate voltage applied ($v_{GS} > V_T$), an n-channel forms between n^+ (emitter) and n^- (drift) region. It provides a path for electron to flow into n (drift) region, which acts as a base current of the parasitic pnp transistor. The holes being minority carriers are also injected to n-drift region due to the forward biased pn-junction (p^+ substrate and n^- drift).

Since p^+ substrate is highly doped, surplus holes (after recombination) collect at the emitter and current flows from C to E. Thus the resistivity of the drift region and the on-state voltage drop reduce with increased current (i_C), unlike to a power MOSFET. Figure 2.33b shows a comparative voltage drop with respect to temperature of IGBT and MOSFET of the same die sized.

The turn-off process is similar to a power MOSFET. Here, the gate turn-off is achieved either by application of a negative voltage, shorting *G* and E terminals or using a high-sink gate driver circuit. It discharges the gate-to-source capacitor (parasitic) and turns-off the parasitic n-channel MOSFET. Therefore, the collector current also suddenly reduces, as n-channel no more exists. The trapped carriers of the lightly doped n-drift region recombine and take a considerable recombination time, which is independent of the supply voltage condition and depends upon the carrier's lifetime. To reduce the on-state losses, like other minority carrier devices, doping level is increased but it simultaneously increases switching turn-off time and reduces voltage withstand capability of the device (as discussed for SCR and ASCR in sections 2.4.1 and 2.5.4, respectively). In case of a punch-through IGBT structure, by adding a heavily-doped n buffer region (between n-drift and p^+ substrate), the switching time is reduced. This layer prevents punch-through of depletion layer (SCL) to p^+ substrate. It reduceds the thickness of the drift region, which reduces on-state losses. However, due to high doping of n buffer, reverse-voltage withstand capability of the device reduces drastically.

When the device is properly biased ($v_{CE} > 0$), it injects minority carriers into n-region, which results in conductivity modulation. Contrary to a power MOSFET, it is a minority carrier device. Due to the absence of conductivity modulation in a power MOSFET, its on-state conduction loss is significantly high in n-region (about 70% in a 500 V class power MOSFET).

When the IGBT is on, the pnp transistor part of the device is never in heavy saturation, which makes turn-off faster than a power BJT. Moreover, the emitter of an IGBT covers the entire area of the die, therefore the injection efficiency and conduction voltage drops are superior to that of a power BJT of the same die area (size). The biggest limitation of the switching speed of an IGBT is due to turn-off delay caused by the lifetime of the minority carriers in n^--drift region (i.e. the base of pnp). Since this layer is not accessible, the external circuit cannot be used to sweep the carriers and to reduce the recombination time. The charge stored in the base of pnp causes the trail characteristics in i_C at turn-off. This increases turn-off losses and requires an increase in the dead time between the conduction of two devices in a half-bridge converter configuration (to avoid short circuit). Moreover, the common-emitter inductance (common to gate and collector circuits), also slows down the switching. The voltage developed across it (Ldi_E/dt) subtracts from the applied gate voltage during turn-on and adds to it during turn-off. Therefore, twisted or parallel gate drive lead/cable is used. This improves immunity to *dv/dt* based turn-on and reduces ringing of the gate voltage signal. A higher resistance to gate drive circuit increases turn-on loss but reduces ringing effect at the gate by increasing damping factor of the gate circuit.

The safe-operating area (SOA) of an IGBT describes its capability to withstand high levels of voltage and current at the same time. Like other minority carrier devices uneven current distribution may take place within the die beyond the safe limit. It may cause device failure. Safe-operating area (SOA) of an IGBT is similar to a power MOSFET. According to the positive and negative rate of change of current (*di/dt*), forward-biased SOA (FBSOA) and reverse-biased SOA (RBSOA) are defined, respectively. Thus FBSOA related to the turn-on transient of the inductive load switching and RBSOA is related to turn-off transient. It is to be noted that the square-SOA or snubberless switching SOA (SSSOA) only gives the absolute maximum current and voltage rating of the device (Fig. 2.34a). However, during turn-off, v_{CE} exceeds the dc-supply voltage (V_{DC}), because of the dc-loop inductance ($v_L = Ldi/dt$). Similarly during turn-on, the collector current exceeds the output current (I_O), because of the reverse-recovery current of the diode.

However, in case of switching of an IGBT with snubber circuit, the voltage and current stresses are greatly reduced (Fig. 2.34b). Similarly, in case of zero-voltage switching (ZVS)/zero-current switching (ZCS) of the device, these stresses are further reduced. Therefore, a designer should know the worst case dynamic switching load lines without a snubber circuit and with a snubber circuit. The dynamic switching load line should fit within the SOA. Moreover, the effective SOA or RBSOA becomes wide for higher frequency (Fig. 2.34c), and the edge is a conditionally defined i.e. frequency dependent switching SOA.

2.6.5 Static Induction Devices

There are a large number of static devices that are in general used for high frequency applications. These devices are from the static induction family. It includes static induction thyristors (SITH), static induction transistors (SIT), static induction-diodes (SID), and lateral punch-through transistors (LPTT), static induction transistor logic (SITL), static induction MOS transistors (SIMOS) and space-charge limiting load (SCLL). However, the first-two are very commonly known and commercially available devices.

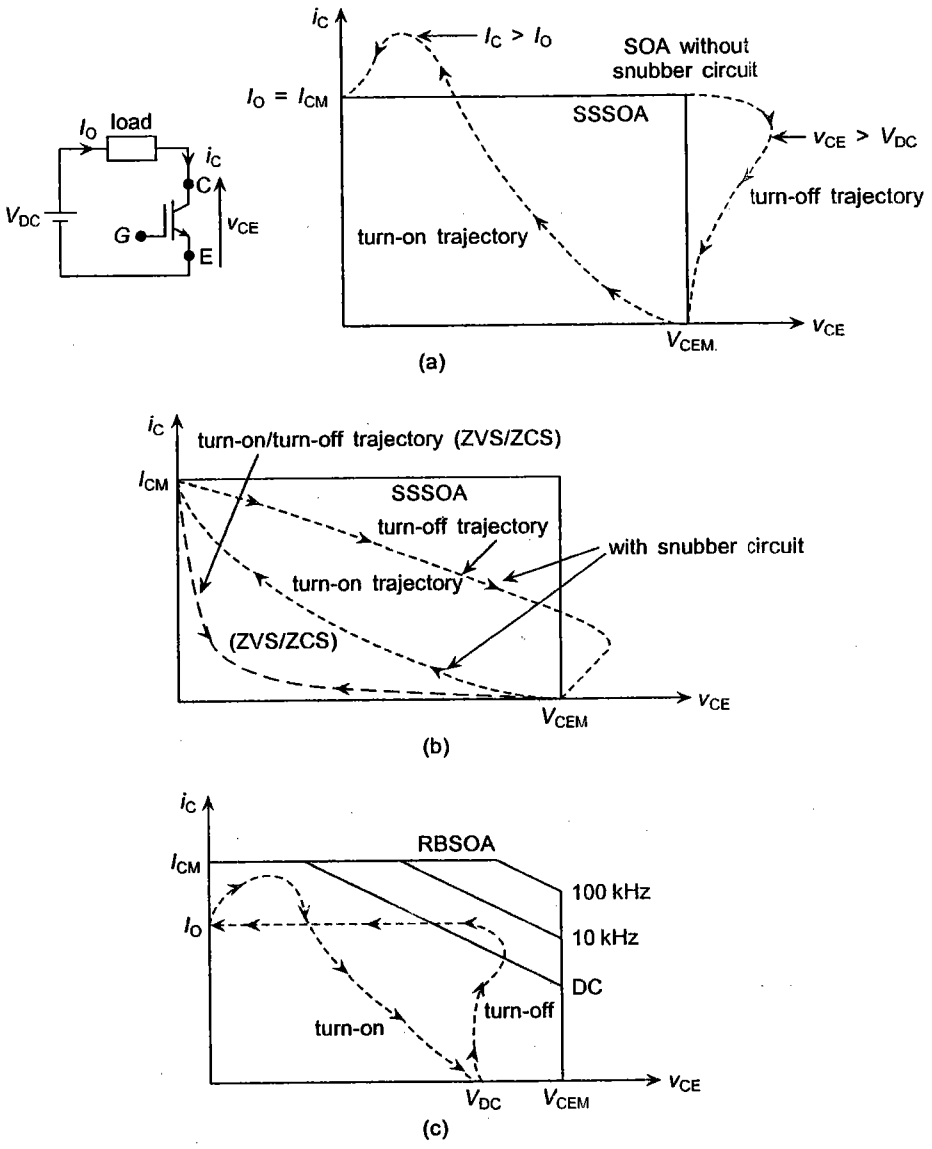


Figure 2.34 Different SOA of IGBT.

Static Induction Transistors (SIT)

It is a high-power high frequency device, which is a solid-state version of a vacuum triode. The device is normally on type and has an unsymmetrical blocking capability (Fig. 2.35). It is faster than MOSFET, but voltage drop is quite higher.

The SIT is used for frequency and high power applications (up to 100 kW at 100 kHz or 10 W at 10 GHz). It is a majority carrier device and can be easily paralleled like MOSFET. It has JFET-type structure except the gate electrodes are baried within the n-epitaxial layer, which

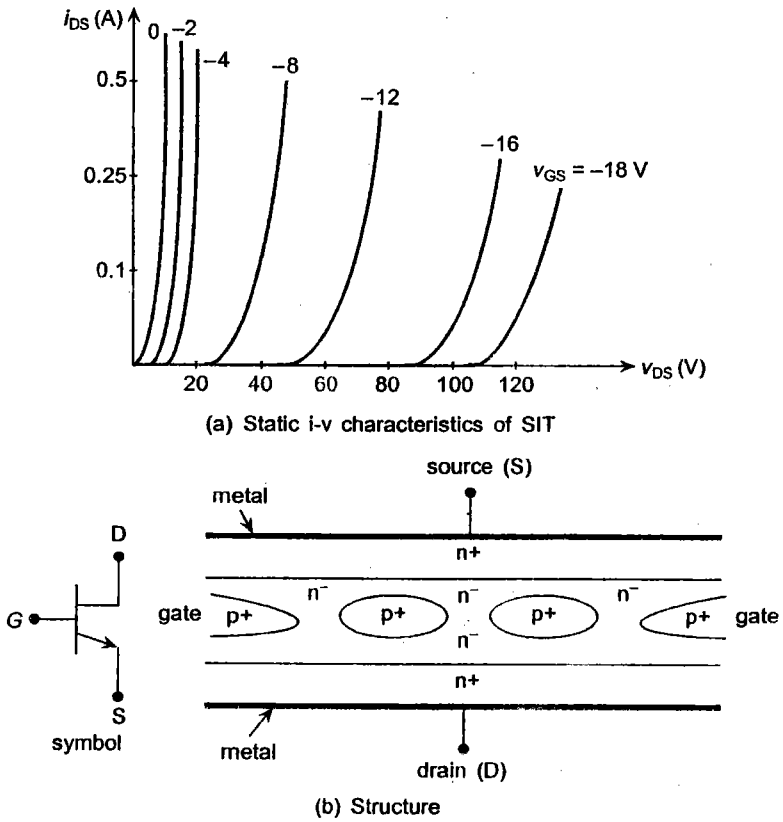


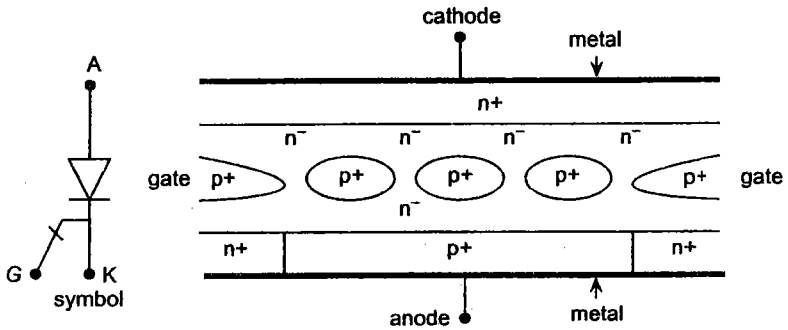
Figure 2.35 Symbol, structure and static characterstics of an SIT.

reduce channel resistance causing a lower on-state voltage drop. Moreover, the induced electrostatic potential barrier by these electrodes controls the current in static induction devices. For $V_{GS} = 0$, majority carrier drift current (as in FET) flows. Similarly for $V_{GS} < 0$, the reverse-biased depletion layer ($p^+ n^-$ junction) pinches-off the conducting area (channel). Ultimately, it cuts-off completely at higher bias voltage (e.g. $V_{GS} = -18$ V). It is evident from the static output characterstics that the forward voltage blocking capability depends upon the negative gate voltage. When the gate voltage is zero, the devices conduct and behave like a diode. Similarly, the device comes into blocking condition. When a negative voltage is applied with respect to the source. There was a large on-state voltage drop in the older SIT design (90 V at 180 A), which is now reduced significantly.

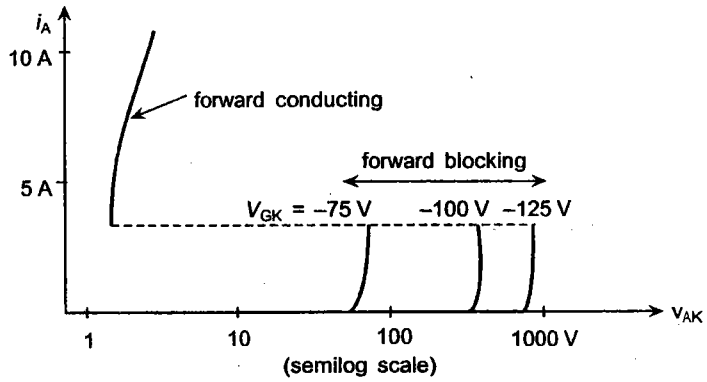
Static Induction Thyristors (SITH)

The device structure is analogous to SIT except an additional p^+ layer near the anode (Fig. 2.36). It consists of a p-i-n diode (intrinsic semiconductor layer between p and n) with a buried p^+ gate structure. The device turns-off when a negative voltage is applied, moreover, as in case of SIT, the voltage blocking capability also increases with increase in the negative voltage ($-V_{GK}$). When the gate voltage is negative with respect to cathode, the anode current ceases. An SITH is also

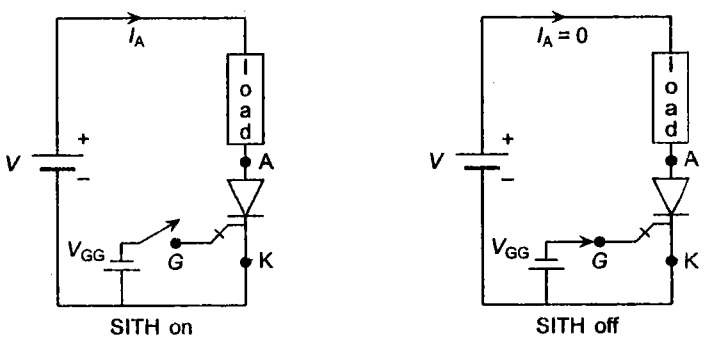
called *field-controlled* thyristor. It is normally an on-device, i.e. with $I_G = 0$, the device behaves as a diode. The gate circuit should have good sink capability (like MOSFET) to discharge the gate-capacitor during turn-on condition. However, very-high-negative-gate current (1/3 of I_A) is required to turn-off the device. It does not have reverse-blocking capability (like RCT).



(a) Symbol and structure of SITH



(b) Static i-v characteristics of SITH



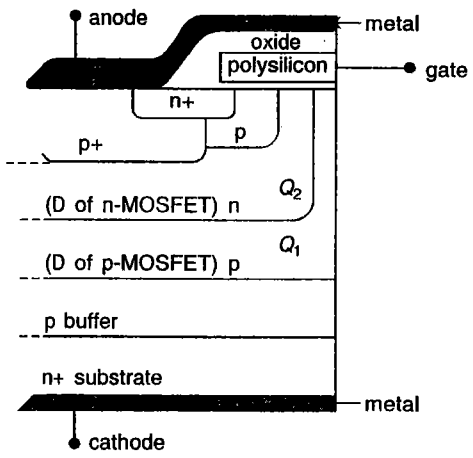
(c) Switching arrangement of SITH

Figure 2.36 Details of static induction thyristors (SITH).

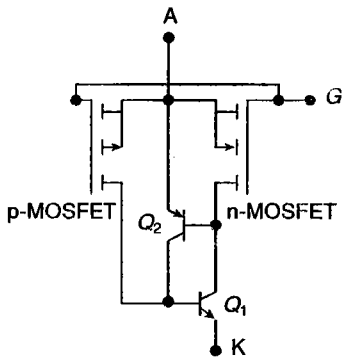
2.6.6 MOS-CONTROLLED THYRISTORS (MCT)

A *metal-oxide semiconductor field-effect transistor controlled thyristors* (MCT) is a four-layer pnpn device. It is a high power, high frequency, high current density and on condition-drop device. An MCT is an improvement over a thyristor with a pair of driving MOSFET to turn-on and turn-off the device. The current density is about 70% higher than that of an IGBT. Actually, it contains a large number of tiny cells (about a hundred thousand).

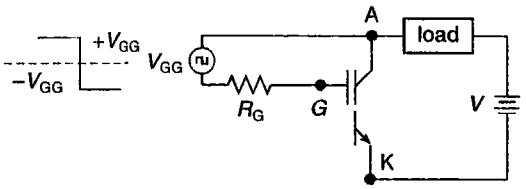
A half-cell of an MCT, equivalent cell and symbol of the device is shown in Fig. 2.37. Contrary to other thyristors (SCR), the gate referred with respect to the anode terminal. Due to better switching properties, it is being used as a static circuit breaker. It is a competitive device to an IGBT. Similar to a power MOSFET, MCT can also be paralleled with slight derating. There are several types of devices of this family, e.g. p-channel MCT, n-channel MCT, MOS turn-off thyristor (MTO or MTOT) etc. However, the p-channel MCT is common which is being discussed here.



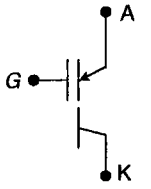
(i) A half-cell of an MCT structure



(ii) Equivalent circuit



(iii) Switching circuit of an MCT



(iv) Symbol

Figure 2.37 Various details of MOS-controlled thyristors.

The MCT can be turn-on or turn-off by a short pulse on the MOS gate. It is similar to GTO but the turn-off current gain is very high (i.e. contrary to GTO very small current is required for turn-off). It is a high power, high frequency, low conduction drop switching device. It appears that MCT is going to replace shortly most of the present generation devices. It uses p-channel MOSFET to turn on. The regenerative action in the device speed up switching (reduces turn-on time) and keeps it in on-condition. For turn-off operation, an n-channel MOSFET is used to divert the base current of one of BJT, which ceases the regeneration action.

Only a small per cent (4%) of pnp transistors are provided with p-channel MOSFET for turn-on (as small current is enough for turn-on). However, a large number of n-channel MOSFET cells are provided for turn-off. When the device is in forward-biased condition, it can be turned on by application of a negative voltage pulse at the gate with respect to anode. It turns on the p-channel MOSFET, whose drain current becomes base driving current for Q_1 (npn) transistor. The collector current of Q_1 drives Q_2 (pnp transistor) and the collector current of Q_2 supplies additional base current to Q_1. Thus, a regenerative action takes place between Q_1 and Q_2 to bring the device into full conduction, within very short period of time. This part of the driving mechanism of the devices is similar to the driving mechanism of an SCR (two-transistor model). Now, no driving gate pulse is required to maintain condition (as in case of an SCR).

The device will cease its conduction only when the anode current is reversed, or a positive pulse is applied to its gate with respect to the anode. This pulse turns on the n-channel MOSFET which diverts the base current of Q_2 to anode (by shorting its emitter-base of pnp). It breaks the regenerative action and turns off the device, the highest current the device can commutate with the help of a gate pulse is called *peak controllable* current.

Normally, the device switching is controlled by a bipolar gate signal, i.e. either $-V_{GG}$ or $+V_{GG}$ with respect to anode for turn-on and turn-off, respectively.

MOS Turn-off Thyristors (MTO/MTOT)

This device is developed for replacement of GTO for high-power applications (in tens of MVA range). It requires much smaller gate drive current to turn-off and the voltage blocking capability is as high as 9 kV. Two separate terminals are used for turn-on and turn-off of the device. The turn-on action is similar to an ordinary SCR using a gate current pulse at G_1 terminal (Fig. 2.38). It causes direct regeneration of Q_1–Q_2 BJT pair. The turn-off is similar to an MCT (as discussed earlier) by application of a gate signal at G_2.

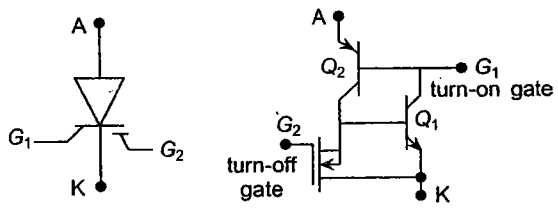


Figure 2.38 Symbol and equivalent circuit of MTO/MTOT.

2.7 A GENERAL COMPARISON OF DEVICES

Table 2.1 clearly shows the relative merits and demerits of each device as well as the highest rating (state-of-the-art) device commercially available.

2.7.1 General Performance of Devices

From Table 2.1, it is clear that diodes and SCR are available with the highest power handling capability. They are extensively used at main frequency (50 or 60 Hz). As they lack controlled commutation facility, gate-commutation-controlled devices became popular. For low-voltage and

Table 2.1 State-of-the-art Power Semiconductor Devices

	Diode	*SCR*	*TRIAC*	*BJT*	*MOSFET*	*IGBT*	*GTO*	*SIT*	*SITH*	*MCT*
Blocking voltage (volts)	10,000 3000# 400&	10,000 1200#	1200	400 1200@	1200 100*	3300 1700* 600**	5000	1200 600* 300**	4000	1200 500*
Maximum current (amp)	5000 1000# 300&	5000 1500#	300	250 400@	20 100*	1200 1800* 2000**	3000	300	2200	100 300*
Switching-on period (μ-sec)	2–5	2–5	2–5	2	0.1	0.2	3–5	0.25	0.2 0.4*	0.2
Switching-off period (μ-sec)	100 2–5# 0.15&	200	200–400	9 30	0.3–0.5 0.6*	1	10–25	0.3	6.5	2.2 1.25*
Maximum operating frequency (kHz)	1 10# 100&	1 10#	0.4	20 10@	300	50	10	4000	2000	20
On-state resistance (milli-ohm)	0.16 1.00# 2.00&	0.25 0.50#	3.5	4 10@	60 9*	60	2.5	1200 7* 4**	6	18

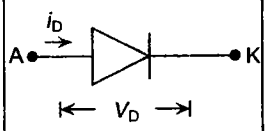
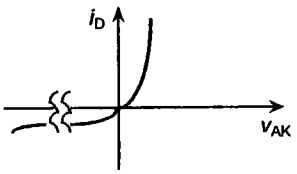
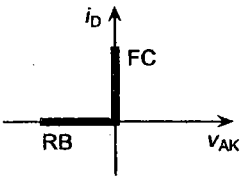
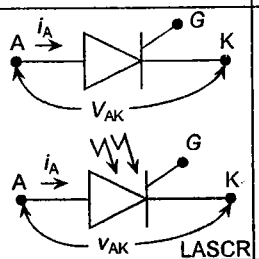
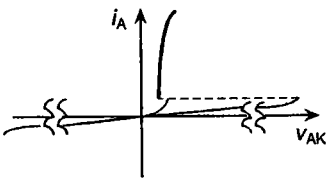
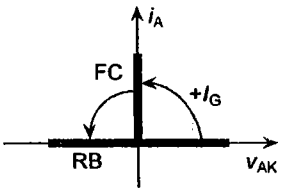
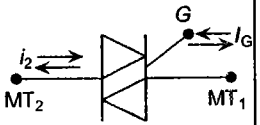
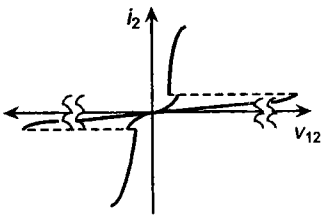
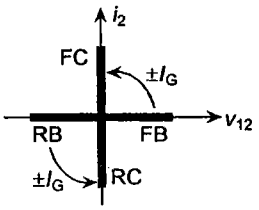
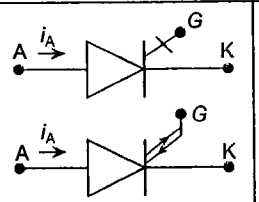
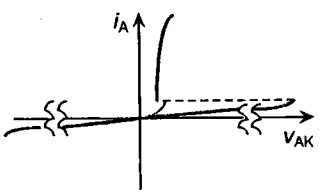
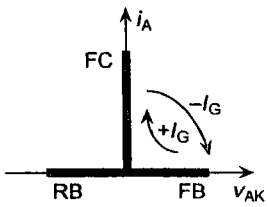
#, Fast-recovery diode/SCR; &, Schottky diode; @, Monolithic Darlington (MD); *, Type-2; **, Type-3 (low voltage).

high-current applications, power BJT were used. Because of the high-base drive (current) requirement, they are becoming obsolete. Moreover, it reduces the efficiency of the converter/controller. For example, a half kVA, BJT based dc-to-ac inverter has 60% efficiency. Contrary to this, a MOSFET/IGBT based inverter of the same rating has 85% efficiency. Therefore, due to negligible gate drive power requirement, better switching performance and flexible commutation facility (independent of circuit conditions) the gate-commutation-controlled devices became popular. IGBT and MOSFET have almost entirely replaced the power BJT. For a high-frequency (above 100 kHz) and high-current (connecting several devices in parallel) applications, are MOSFET preferred. However, for high voltage, high current and low on-state losses, an IGBT is preferred over a MOSFET. However, the cost of an IGBT is significantly high in comparison to a MOSFET. Normally, IGBTs are available, starting from hundreds of voltage, while MOSFET are available with a few tens of voltage rating. In general, a GTO is used for a high-power and high-current applications (e.g. above 150 A). But requirement of a very high rating gate driver circuit (almost one-third of the device rating) for commutation is the main drawback of this device. Due to continuous increase in power and voltage rating of IGBT, a GTO is also being slowly replaced. Static induction devices (SIT, SITH), which have limited applications for very-high-frequency applications (above 1 MHz). The main drawback with them is high on-state losses. MCT has attributes of both MOSFET(IGBT) and SCR. Therefore, due to low switching losses and gate commutation facility, it is expected that it is going to replace most of the power semiconductor devices. However, a high-rating economical MCT is still awaited and it is not commercially available.

2.7.2 Ideal Characteristics of Devices

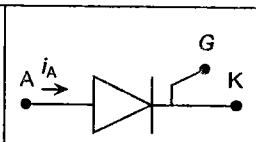
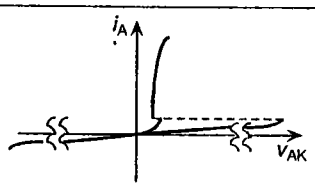
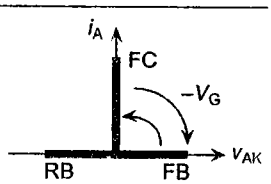
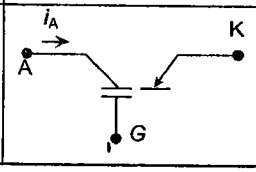
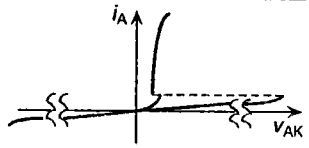
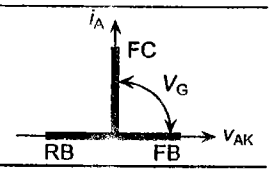
In the preceding sections, static i-v characteristics of different power semiconductor devices are discussed in detail. These characteristics vary greatly. However, the performance of devices, when used in a converter, is quite similar. Therefore, in general, the performance of a converter is understood and it is analyzed with respect to the ideal characteristics of the devices. For example, the process of commutation (turn off) of an SCR completes when its anode current (i_A) reduces to holding current level. The holding current of SCR is of the order of tens of milliampere. However, in the ideal characteristics, commutation of SCR completes when $i_A = 0$. Similarly, in the forward-blocking condition, $i_A \neq 0$. Whereas, in the ideal characteristics, it is considered to be zero. Therefore, the ideal characteristics slightly modify the actual characteristics, to simplify the analysis of converters/controllers. Table 2.2 gives a list of ideal and actual characteristics of the devices.

Table 2.2 Characteristics and Symbols of Power Semiconductor Devices

Devices	*Symbols*	*Actual characteristics*	*Ideal characteristics*
Diode			
SCR			
Triac			
GTO			

(Cont.)

Table 2.2 Characteristics and Symbols of Power Semiconductor Devices (*Cont.*)

Devices	*Symbols*	*Actual characteristics*	*Ideal characteristics*
SITH			
MCT			

2.7.3 Relative Performance of MOSFET/BJT/SCR

Table 2.3 is given here to understand the capability of these devices and to do comparison between thyristor (SCR), BJT and MOSFET.

Table 2.3 Relative Performance of SCR, BJT and MOSFET

SCR	*BJT*	*MOSFET*
Minority carrier device	Minority carrier device	Majority carrier device
Current driven device	Current driven device	Voltage driven device
High-voltage, high-current device Low-switching speed	High-current, low-voltage device Medium-switching speed	High-current, medium-voltage device High-switching speed
Low-resistive input (gate-cathode) impedance	Low input (base-emitter) impedance	Purely capacitive, high input (gate-source) impedance
Only single pulse is required for switching (turn-on)	Continuous dc (base) current is required to maintain conduction	No dc current is required to maintain conduction except during turn-on and turn-off conditions
Can be connected in series easily with voltage equalizing circuits	Series connection is difficult with voltage equalizing circuit (base/gate current requirement of each device)	Series connection is difficult with voltage equalizing circuit (base/gate current requirement of each device)
Thermal run away	Thermal run away	No thermal run away
Line commutation or separate switching arrangement is required for turn-off	No separate circuit is required	No separated circuit is required
Can be paralleled with forced current sharing circuits/ transformers	Cannot be easily paralleled because of V_{BE} matching problem	Easily paralleled due to positive temperature coefficient of resistance of the device
Most robust device	Less robust device	Less robust device
Low on-state voltage drop	Lower on-state voltage drop	High on-state voltage drop
Less temperature sensitive	Temperature sensitive	Temperature sensitive (less than BJT)
No second breakdown	Second breakdown	Less susceptible to second breakdown
Operating characteristics		
Maximum temperature: 125°C	150°C	200°C
Gain range: 10^5–10^7	10^1–10^2	10^5–10^6
Input (gate/base) impedance: 10^1 ohms	10^3–10^5 ohms	10^9–10^{11} ohms

2.8

MANUFACTURER'S DATA SHEET

A typical data sheet is given in Table 2.4 for SCR series (OE-1600) from Orbitron Electronics.

Table 2.4 S.C.R. Quick Typical Reference Data (OE-1600 series)

Type number	$I_{T(RMS)}$ (amp)	V_{DRM} (volt)	V_{RRM} (volt)	V_{RSM} (volt)	V_F (volt)	V_{GT} (volt)	I_{GT} (Ma)	T_{IM} (°C)
OE-1600	16	50	50	65	1.7	3	50	100
OE-1601	16	100	100	150	1.7	3	50	100
OE-1602	16	200	200	300	1.7	3	50	100
OE-1604	16	400	400	500	1.7	3	50	100
OE-1606	16	600	600	700	1.7	3	50	100
OE-1608	16	800	800	900	1.7	3	50	100
OE-1610	16	1000	1000	1100	1.7	3	50	100
OE-1612	16	1200	1200	1300	1.7	3	50	100

RATING

The limiting values of the above series (OE-1600) are given are as follows:

Conducting state

Maximum forward voltage drop at T_j = 25°C	V_{Fmax} = 3.0 volt
Average on-state current	$I_{T(AV)}$ = 10 amp
Holding current (dc voltage)	I_H = 40 mA
Average on-state power dissipation	P_D = 25 watts
RMS surge (non-repetitive) on-state current	I^2t = 60 A-sec (where $t \leq 10$ ms)
Peak reverse blocking current	I_{ROM} = 7 mA
Peak forward blocking current	I_{FOM} = 7 mA
Full cycle average reverse blocking current	I_{RX} (AV) = 2.5 mA
Full cycle average forward blocking current	I_{FX} (AV) = 2.5 mA

Gate parameters

Maximum gate triggering current	I_{GTM} = 70 mA
Maximum gate triggering voltage	V_{GTM} = 3.5 volts
Average gate power	$P_{G(AV)}$ = 0.5 watts

Thermal characteristics

Operating junction temperature range	T_j = −40° to +100°C
Storage temperature range	T_{STG} = −40° to +120°C
Case temperature	T_C = 60°C
Effective thermal resistance (DC)	ϕ_{jc} = 1.2°C/Watt max

Switching parameters

Rate of applied voltage	dv/dt = 20 V/μs (typical value)
Rate of change of on-state current	di/dt = 25 A/μs (typical value)

Mechanical parameters

Stud-torque = 30 lbs-inch (35 kg-cm)

Manufacturers used to specify device characteristics by suitable data. The device can be used properly within the safe-operating area (SOA), when the limiting values (ratings) of different parameters are known. Data sheets of different devices are given in the appendix.

2.9 GENERAL CONSIDERATIONS

Power dissipation, heat sinking and device mounting are important considerations for proper use of devices. They are now discussed:

Power Dissipation

The power semiconductor devices are not ideal switches. Therefore, power loss takes place during on-state, off-state as well as at the switching transitions. During off-state negligibly small current passes through the device at a rated voltage. While the rated current passes through the device with very low-voltage drop at turn-off condition. Thus the power loss in both the conditions are negligibly small. However, during the switching transition period, the device power loss (P_d) becomes significant. This loss depends upon transition period (T_t) and frequency of device switching (f_s). Thus P_d gives an idea about upper limit of f_s. The maximum value of P_d for an inductive load circuit is given by

$$P_D = V_d I_d \frac{T_t f_s}{6} \tag{2.40}$$

It may be lower for purely resistive load. At power frequency (below 100 Hz), P_D is not significant. For a fast recovery diode, the same is true even up to 1 kHz. The reliability and life expectancy of a power semiconductor is directly linked to the maximum junction temperature (T_j), current and power ratings of the device. Therefore, a heat exchanger is required to limit it. It was found that the failure rate decreases to half (50%) of silicon semiconductors for a decrease in T_j from 160°C to 135°C. Many failures are found due to faulty mounting causing unnecessarily high T_j.

Heat Sinking

Except for low-rating devices (lead mounted with a few watt power loss only), aluminium heat-sinks of various shapes are used to prevent the T_j from exceeding the rated limit. For the heat-sinks cooled by natural convection, the distance between two cooling fins is maintained at least 10 to 15 mm. Since a black body dissipates maximum heat, a black coating may improve cooling by decreasing the thermal-resistance by 25%. Fans are also used to cool the heatsinks called *forced air-cooled heat-sinks*. In case of natural cooling or convection, the time-constant of the cooling varies between 4 to 15 minutes while forced cooling reduces it to less than 1 minute. The forced air even at 2 m/s speed reduces the thermal resistance to a half. This type of arrangement is used in UPS and in the DC power supply of personal computer (MOSFET or IGBT based SMPS). In higher power applications, e.g. in HVDC systems, water or oil cooling is used to further improve thermal conduction.

Mounting Techniques

Proper mounting or fixing the device with heatsink avoids unnecessary heating of the semiconductor, which results in device failure. For this purpose proper attention has to be paid to the following areas:

1. Mounting surface preparation
2. Application of thermal compounds
3. Insulation of insulator
4. Fastening of assembly
5. Lead bending and soldering.

In general, the heat-sink mounting surface should be flat and finished, comparable to that of the device. Uneven surfaces or improper contact between a device and a heat-sink surface causes a poor conduction of heat. Moreover, thin air film or layer of oxides of metal (e.g. aluminium), is a poor conductor of heat. It increases the thermal resistance between device-casing and heat-sink ($R_{\theta c\text{-}s}$). To improve contacts, thermal compounds (like silicone grease) are put in between contact surfaces. If the voids, scratches and imperfection filled with thermal compound (which is thermally conducting), $R_{\theta c\text{-}s}$ is found to reduce to (1/20)th of its original value.

Wiring inductance depends upon the nature (or type) and length of the leads of current carrying wire of the device. Cancelling the magnetic fields in a number of ways can reduce it. First, the length of wire should be minimum, i.e. devices should be very close to each other. Second, the go-and-return paths should be parallel and physically close to each other. The per-unit inductance value of a conical cable is about 60 mH/metre. For parallel conductors (5 cm apart), it is almost 6 times more than that of a coaxial cable or parallel plates separated by a thin insulation layer (like bundle conductors).

The inductance of go-and-return path of parallel wiring conductors of radius r and separation D is given by

$$L = \frac{\mu_0}{\pi} \ln \frac{D}{r} \text{ (H/m)} \tag{2.41}$$

Litz wires are also used to reduce the inductance for very-high-frequency applications (instead of single strand wire/cable, a group of copper strands, separated by insulation, is called Litz wire). Moreover, wiring should cross together at perpendicular instead of moving in parallel. Care should be taken to avoid dry soldering at terminals of the device, which may introduce contact resistance of a significant magnitude. Similarly, during soldering, the temperature of the device terminals should not exceed the temperature limit of the device.

2.10 POWER MODULES

Often several power semiconductor devices are required in a single converter, e.g. six SCR in a three-phase ac-to-dc converter/inverter. Similarly, six MOSFET/IGBT are used in a dc-to-ac inverter. In a single-phase ac-to-dc converter, four devices are used. However, only two devices

are required in a half-bridge inverter/converter. Therefore, several power semiconductor devices are available in a group of 2, 4 or 6, as a single unit or module. It has several merits, e.g. high-speed and better switching characteristics due to compact circuitry (less inductance due to absence of connecting wires) and low losses (in connection wires). Sometimes, diodes and other protecting devices are also included in the same package or module.

Intelligent/Smart Modules

It is a power module integrated with protection and control peripheral circuits, designed and fabricated on a single chip. Normally, it has input/output isolation from an interface gate driver circuit, over-current and over-voltage protection circuits, diagnostic circuit, over-heating sensor, microcomputer control, etc. Sometimes an additional external dc-power supply is required.

In addition to the power modules and smart power modules, now complete dc-to-dc converter and motor drive modules are also available on the market of medium power rating (e.g. drive modules for vector control of induction motors). In addition to intelligent module, normally, it consists of the following parts:

1. *EMC unit:* It consists of line filter circuits (choke and capacitors), and transient clamp circuit.
2. *Rectifier unit:* Diode bridge rectifier with voltage clamp.
3. *Inrush control unit:* Semiconductor switch (IGBT/MOSFET) and current sensor, controller IC and transient clamp.
4. *PF correction unit:* Semiconductor switch (IGBT/MOSFET) and current sensor, controller IC and transient clamp.
5. *Power supply:* Regulated dc power supply for control/microprocessor control IC.
6. *Inverter:* IGBT/MOSFET based PWM inverter.

It is evident from the above that the motor drive modules consist of different types of power semiconductor devices, IC, microprocessor and protective units.

2.11 APPLICATION OF DEVICES

Invention of thyristor in 1956 introduced a new branch of electrical engineering—power electronics. Subsequently other power semiconductor devices are developed, e.g. TRIAC, GTO, bipolar power transistors, power MOSFET, IGBT, SIT, SITH and MCT, etc. Thus converter/controller circuits of wide applications become possible. Phase-controlled ac-to-dc converters, ac-phase controllers, dc-to-ac inverters, switched mode power supplies (SMPS) are commonly employed. They vary from a few-watt toys and domestic appliances to hundreds of MW HVDC system and steel rolling mills. These controllers are compact, highly efficient and offer flexibility of control. It is expected that within the quarter century 100% power will flow through these devices, at least, at any one stage of generation, transmission or distribution.

SUMMARY

In early 1950s, the semiconductor diode replaced the vacuum-tube rectifier and thus improved the efficiency by reducing on-state voltage drop from 30 V (vacuum tube) to 1–2 volts (semiconductor diode). The silicon controlled rectifier (SCR) was invented in 1956 and was commercially available in 1957. It was due to its invention, a new branch of engineering, i.e. power electronics has been created. Rating of both diode and SCR went to the highest level of all power semiconductor devices, viz., several kV, kA and MW. Both these devices (converter-grade) are most robust, reliable and have the highest transient withstand capability. Fast-recovery diodes and SCR (inverter-grade) are fast and their switching losses are small, but they are costly. TRIACs are bidirectional controllable device. It is more vulnerable to the transients and inductive loads. Mostly triacs are used in ac regulators (at power frequency 50 or 60 Hz). By mid-1960's, BJT based converters were used at high frequency (10–20 kHz). Thus a practical, efficient lightweight dc regulator became available. However, a power BJT requires substantial and sustained base-drive current (current gain, h_{fe} = 3–10). Both SCR and BJT are current controlled devices. In the late 1970s, the MOSFET was invented and high frequency (200 kHz–1 MHz), highly-efficient low-power converters were realized. It is a voltage-controlled device, which requires negligible power for the gate-drive circuit. It further reduced the size of the converter. Moreover, parallel operation of MOSFET for increasing the current rating, became extremely simple. Development of IGBT in 1980's further improved the converter efficiency (above 90%) by reducing on-state voltage drop and losses, which was present in MOSFET. The gate characteristics of IGBT are same as MOSFET (low power, low voltage) and on-state characteristics are like SCR. Although operating frequency range is less than MOSFET, but power-handling capability is more than MOSFET. A series of static induction devices were developed subsequently for very-high-frequency applications. However, their performance is inferior to IGBT due to high on-state losses. Ultimately, MOS-controlled thyristor (MCT) was developed. In 1992, it was commercially introduced by Harris semiconductors. It resembles an ideal switch and has features like IGBT (for gate characteristics) and SCR (for on-state characteristics). Both turn-on and turn-off are smooth and controlled by a positive and negative low-power gate signal, respectively. Moreover, paralleling of MCT is as simple as MOSFET (with slight derating). It is expected that on the availability of MCT at reasonable cost with more matured device technology, it will replace almost all other gate-commutation devices. At present, major research activity focus on obtaining new device structures based on MOS-BJT technology integration. Furthermore, power ratings of power modules (smart power) dc-dc converter modules and motor-drive modules will continuously increase due to continuous development of device technology and IC fabrication (high-density) technology.

REVIEW QUESTIONS AND PROBLEMS

1. In what respect a semiconductor switch is better than an electromagnetic-contactor switch?
2. Why commutation (turn-off) of a diode depends upon the circuit?
3. What are the conditions for successful switching (turn-on) of an SCR?

4. How doping level affects performance of a thyristor or SCR, explain?
5. What are the conditions for successful commutation of an SCR?
6. In what respect a triac is better than an SCR?
7. Why, in general, a triac is not used for inductive loads?
8. Why snubber circuits are used?
9. Why *di/dt* protection is necessary?
10. What are the requirements of series connection of thyristors.
11. Why paralleling of MOSFET is easy than any other devices?
12. Why power BJT are becoming obsolete now?
13. In what respect an IGBT is better than a MOSFET?
14. Mention merits and demerits of static induction devices.
15. Mention superiority of MCT over all other devices.
16. Find the absolute maximum switching frequency of an inverter-grade SCR (BTW-32-1200RM) whose rating and various parameters are given below:
    I_T (av) = 37 A, I_T (rms) = 55 A, I_{TSM} = 600 A; V_{RRM} = V_{RSM} = 1200 V, V_{RWM} = 1000 V; V_T = 3.5 V at I_T = 100 A; I_H < 200 mA; t_{on} < 2 μs; t_q < 11 μs (at 25°C) and < 25 μs (at 125°C); $R_{\theta j\text{-}mb}$ = 0.6°C/W; T_{jmax} = 125°C; *dv/dt* = 200 V/μs and *di/dt* = 20 A/μs.

3

Triggering Circuits for Thyristors*

3.1

INTRODUCTION

All power semiconductor-controlled devices require a drive signal. However, the gate (or base) drive requirement of each device varies. It depends upon the voltage and current rating and also on the type of the device (i.e. thyristors or gate-commutation devices). The gate-drive requirements of thyristors (SCR, RCT, ASCR, LASCR, triac, etc.) are completely different from the gate-drive requirements of gate-commutation devices, viz., GTO, power BJT, MOSFET, IGBT, SIT, MCT, etc. Here gate drive or triggering circuits of thyristors are discussed in detail.

3.2

THYRISTOR GATE REQUIREMENTS

A thyristor can be triggered by the application of a positive gate voltage (v_G) or a gate current (I_G), supplied from a gate-drive circuit, as shown in Fig. 3.1. However, the choice of v_G and I_G is not restricted to a particular value rather it varies over a wide range and depends upon gate characteristics of the device, as shown in Fig. 3.2. Any operating point (v_G, I_G) may be selected within the permissible or preferred gate-drive area bounded by curves 1, 2, 3, 4, 5 and the rectangle mnop. Curve 3 represents a constant value of maximum permissible gate power dissipation (P_{GM}). Moreover, there is a non-trigger gate voltage (V_{GD}), which is a minimum gate-voltage, below which a thyristor cannot be triggered at any temperature (normally up to 100°C). This gives a permissible noise level of the gate-drive circuit that will not trigger the thyristor in worst cases. The manufacturers prescribe the rectangle mnop to avoid both unsuccessful and undesirable triggering. It corresponds to the threshold-condition of triggering (V_{GT}, I_{GT}). It is related with forward-anode voltage (v_{AK}) and junction temperature (T_j). For lower temperature, V_{GT}

*Contributed by the author and published earlier: 'Gate drive circuits', in *Power Electronics Handbook*, Rashid, M.H. (Chief Editor), Ch. 18, Academic Press, California. Received permission from Elsevier/Academic Press, California, to republish it.

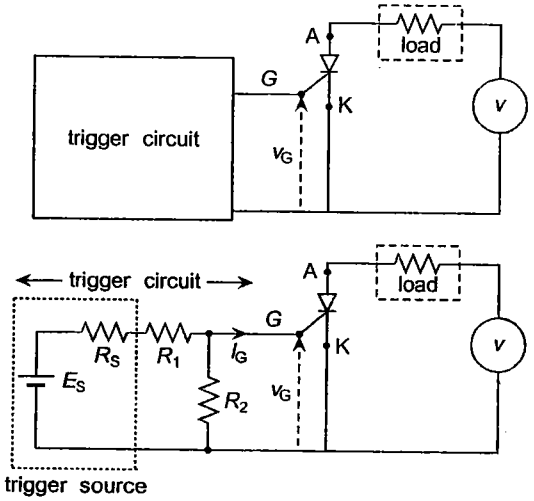


Figure 3.1 A typical switching arrangement for an SCR.

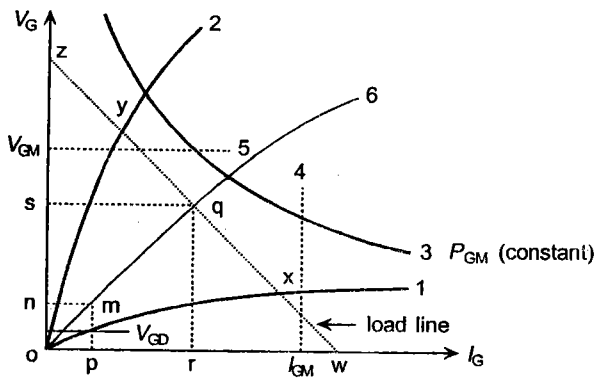


Figure 3.2 A typical gate characteristics of an SCR.

and I_{GT} increase and therefore the size of the rectangle 'mnop' increases. Similarly, it should be ensured that the gate-circuit load-line (wxyz) should pass above this area. However, the most preferred zone for the operating point is close to the curve 3. This, in turn, increases *di/dt* capability, minimizes the switching-on time and hence reduces switching loss of the thyristor.

Gate trigger circuits can be designed with the help of both Figs. 3.1 and 3.2. Curve 6 shows the gate-to-cathode forward *v-i* characteristics of the device at given v_{AK} and T_j. This is same as forward-conducting characteristics of a silicon diode. The load-line wxyz of the gate trigger circuit intersects the device characteristics at q. Thus operating gate voltage (v_G) and gate current (I_G) are given by or and os, respectively. The permissible range of the operating point is between x and y. The maximum or short-circuit current of trigger source is $E_S/(R_S + R_1)$, which is shown by ow. R_1 should be selected such that this current is not harmful to the source as well as to the gate-to-cathode junction (J_3). Similarly oz shows maximum trigger source voltage E_S. The presence of R_2 is optional. However, if E_S is greater than V_{GM}, it helps to clip V_G not to exceed V_{GM} level.

Otherwise, J_3 may be damaged. Moreover, R_2 provides a low gate-to-cathode impedance during the off-state of the device. It improves the thyristor noise immunity. When R_2 is connected across G and K terminals, the maximum V_G should be less than V_{GM}. Thus

$$\frac{R_2}{R_S + R_1 + R_2} E_S \leq V_{GM} \tag{3.1}$$

Also,

$$E_S = V_G + (R_S + R_1)\left(I_G + \frac{v_G}{R_2}\right) \tag{3.2}$$

The above design considerations are in terms of continuous or dc values of gate voltage and gate current. However, a single pulse or a train of pulses are also used to trigger a thyristor. The above design considerations (with dc values of V_G and I_G) are also valid for a pulse width up to 100 μs. For a short pulse-width, V_G (peak) and I_G (peak) should be increased. In case of a single pulse, the width of the gate pulse should be wide enough such that anode current would reach the latching current level of the thyristor. This is an important consideration for a highly inductive load, where the rise-time of anode current is significantly high. For a train of pulses, it is practically found that a 50-μs pulse-width at 10 kHz (50% duty-cycle), is sufficient for switching a highly inductive load. However, the average value of the peak gate drive power, P_G (peak), should be less than P_{GM} (dc value), such that

$$P_{GM} \geq P_G \text{ (peak)} \times \text{Duty ratio} = P_G \text{ (peak)} \times \text{Pulse width} \times \text{Frequency of pulses} \tag{3.3}$$

Similarly, there is a permissible limit of the maximum negative gate voltage that may appear across gate-to-cathode junction. This is just like peak inverse voltage (PIV) rating of an ordinary pn-junction diode. For this purpose, either a diode is connected in series with a gate (between R_1 and G), or a diode (or a Zener diode) is connected across the R_2, where cathode of diode is connected to G. The Zener diode clips the positive overshoot of the gate voltage above V_{GM} level.

Example 3.1 Design a suitable gate trigger circuit for an 800-V, 110-A SCR (OE-C50N) connected with a 6-V dc power supply. The maximum permissible current and the short circuit current of the dc source are 200 mA and 500 mA, respectively. The SCR has the following gate parameters: $v_G = 2.5$ V, $I_G = 50$ mA, $V_{GM} = 3$ V, $I_{GM} = 100$ mA, $P_{GM} = 0.5$ W.

Solution (i) For a gate drive circuit shown in Fig. 3.1 (without R_2), short circuit current, $I_{Sh} = 500$ mA. Therefore,

$$R_S = \frac{E_S}{I_{Sh}} = \frac{6}{0.5} = 12\ \Omega$$

To protect the source from the excessive current, the minimum value of resistor R_1 is given by

$$R_S + R_1 \geq \frac{E_S}{0.2} = \frac{6}{0.2} = 30\ \Omega$$

or

$$R_1 \geq 30 - 12 = 18\ \Omega$$

Also, to protect the gate-to-cathode junction of the SCR, the minimum value of resistor is given by

$$R_S + R_1 \geq \frac{E_S}{I_{GM}} = \frac{6}{0.1} = 60\ \Omega$$

or

$$R_1 \geq 60 - 12 = 48\ \Omega$$

Therefore, R_1 should be greater than 48 Ω.

Now corresponding to the typical gate characteristics, i.e. $V_G = 2.5$ V and $I_G = 50$ mA, the maximum value of resistor R_1 is given by

$$R_S + R_1 \leq \frac{E_S - v_G}{I_G}$$

or

$$R_1 \leq \frac{E_S - v_G}{I_G} - R_S = \frac{6 - 2.5}{0.05} - 12 = 58\ \Omega$$

Thus R_1 should be selected within 58 Ω and 48 Ω. Depending upon the availability of resistors of different values in the market, we may choose, $R_1 = 56\ \Omega$.

(ii) Resistor R_2 is also incorporated (Fig. 3.1): since V_G should not exceed V_{GM} level,

$$\frac{R_2}{R_S + R_1 + R_2} E_S \leq V_{GM}$$

or

$$R_2 \leq \frac{V_{GM}}{E_S}(R_S + R_1 + R_2) = \frac{3}{6}(12 + 56 + R_2)$$

Therefore, we choose $R_2 = 68\ \Omega$.

3.3 TRIGGER CIRCUITS FOR THYRISTORS

Normally, thyristors are switched on by a voltage signal at the gate terminal of the device (Fig. 3.1). The gate voltage (v_G) is generated with the help of a gate-drive circuit, which is called *firing* or *triggering* circuit. Thus thyristors can be switched on by a slow-rising rectified ac signal, a sharp single pulse, a constant magnitude dc signal, or a train of high-frequency pulses, as shown in Fig. 3.3. The thyristor switches on as soon as v_G exceeds the critical gate trigger voltage (V_{GT}) level, at the switching angle, α. This depends upon gate-to-cathode junction temperature (T_j), anode current (i_A) and the supply voltage. The ideal switching signal for a thyristor should have an adequate amplitude of current for sufficient duration with a short rise time as shown in Fig. 3.4. The initial high magnitude and rapid rise in gate current quickly turns on the device completely. Thus, carriers spread rapidly throughout the layer of blocking junction (J_2). This decreases switching losses and increases initial *di/dt* capability of the device. After a few microseconds, a small gate current (slightly higher than the minimum value required for triggering, I_{GT}) can be maintained. Generally, a gate signal is not required continuously but inductive circuits necessitate sustained gate signal, till a successful triggering takes place. For reliable operation of controllers,

gate trigger signals are normally supplied during whole one period (e.g. converters of a dc drive). However for a resistive load, a single sharp rising pulse is enough for triggering. For high-power applications, it is a common practice to isolate the control and triggering circuits from the power circuit (consisting of thyristors). Otherwise, effects of high voltage and high-current transients may cause mal-operation, or damage the low-power control and trigger circuits. For this purpose, pulse transformers or opto-couplers are used for low- and medium-power semiconductor devices. For higher-power applications, e.g. HVDC transmission systems, fibre-optical cables are used to isolate control circuit from the power circuit. A 5-milli-watt light trigger power source was found sufficient for switching a LASCR of 4-kV, 3-kA rating.

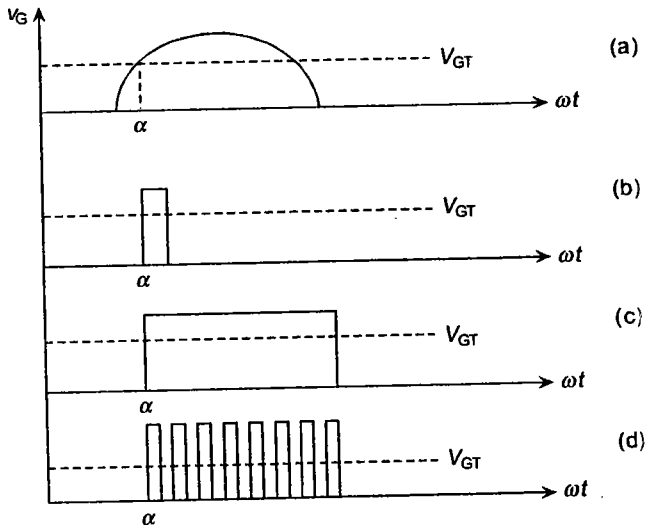


Figure 3.3 Different types of trigger signals for switching a thyristor.

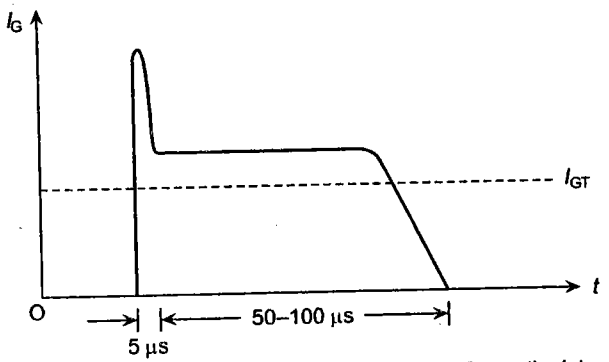


Figure 3.4 An ideal gate current required for a thyristor.

In general, a thyristor conducts when it is properly biased and the trigger source of a trigger circuit supplies the required minimum gate voltage (V_{GT}) and gate current (I_{GT}).

3.4

SIMPLE GATE TRIGGER CIRCUITS FOR THYRISTORS

Simple trigger circuits can be realized using an R or RC network. They are cheap and low power-consuming. However, the control hence the load output voltage (v_0) are susceptible to the device temperature variations. Moreover, feedback control cannot be easily incorporated.

3.4.1 Resistance Trigger Circuits

A step-dc voltage, a slow-rising dc signal, or a rectified positive-half-wave signal can be used to trigger thyristors. When the voltage applied to the gate terminal exceeds V_{GT} level, triggering takes place. Figure 3.5 shows trigger circuit and waveforms for an ac circuit. Before conduction of the SCR, the input supply voltage (v) appears across the SCR.

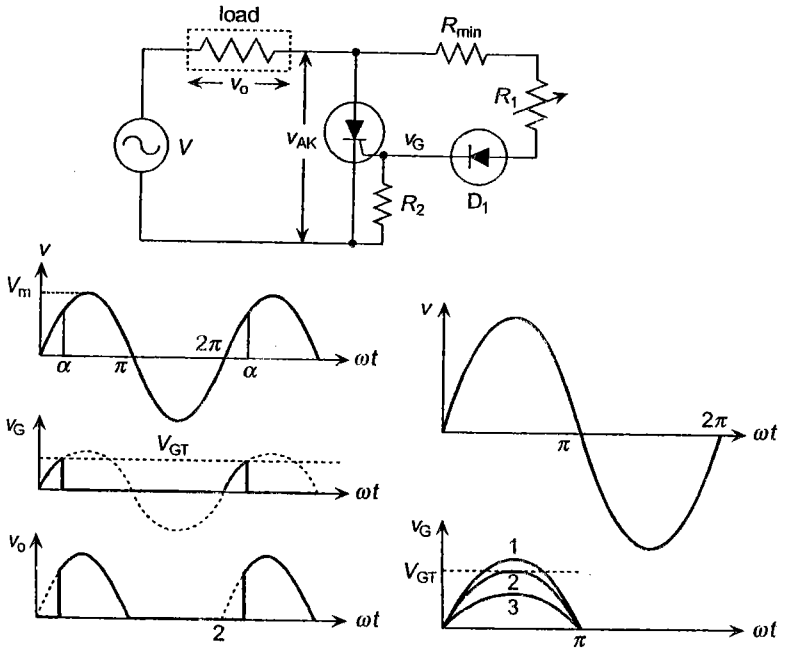


Figure 3.5 Resistance trigger circuit for an SCR.

Neglecting R_2 (being large in comparison to R_{GK}) and the voltage drop across D_1, the gate voltage is given by

$$v_G = \frac{R_{GK}}{R_1 + R_{GK} + R_{min}} v \tag{3.4}$$

where $v = V_m \sin \omega t$, the supply voltage, and R_{GK} is forward gate-to-cathode resistance.

As soon as v_G reaches V_{GT} level and supplies the required gate current, conduction of SCR takes place. The voltage v_{AK} collapses. Therefore v_G also reduces to almost zero level and v

appears across the load. Now, R_1 can be increased to reduce v_{R2} and thus to increase α. But with a larger R_1, eventually, the circuit fails to trigger the device, as shown by the curve 3. Here the control of α is restricted to 90° only (curve 2 of v_G in Fig. 3.5). Similarly, I_G should not exceed I_{GM} level. Therefore, the minimum value of the resistor R_{min} is given by

$$\frac{V_m}{R_{min}} \leq I_{GM} \tag{3.5}$$

This circuit is further improved by adding a resistor R_2 across G and K terminals of the SCR. Then the worst-case voltage across R_2 should not exceed V_{GM} level. Therefore, the maximum value of the resistor, R_2 is given by

$$\frac{R_2}{R_{min} + R_2} V_m \leq V_{GM} \tag{3.6}$$

Same circuit is also applicable for triac. However diode D_1 has to be removed such that trigger signal will be available at the gate terminal during both the half-cycles. Since the gate of a triac is not equally sensitive in all its four modes of switching, α and hence v_o are usually different in the positive and negative half-cycles of the supply voltage.

3.4.2 *RC* Trigger Circuits

A phase-shifted signal in an ac circuit and a slow-rising signal in a dc circuit generated by an RC network, are used to trigger the thyristors. In these cases, the range of α is extendable beyond 90°.

AC-type

Figure 3.6 shows a trigger circuit and related vector diagram. The supply voltage appears across the RC branch. Neglecting the discharge of the capacitor during the conduction period of the thyristor, the circuit can be analyzed by the sinusoidal steady-state response of a linear RC circuit. Thus, the phase angle of the capacitor voltage (θ), can be controlled from 0° to almost 90°

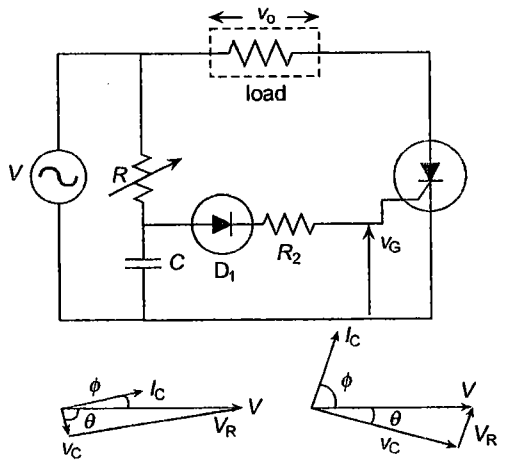


Figure 3.6 A typical RC trigger circuit.

(Fig. 3.6). However, the rms value of the capacitor voltage (V_C), which is equal to $V\cos\theta$, decreases drastically for higher value of θ. By variation of R, phase angle (θ) as well as magnitude of V_C change. The power-factor angle (ϕ) of the RC circuit is given by

$$\phi = \tan^{-1}\frac{XC}{R} = \tan^{-1}\frac{1}{\omega CR} \tag{3.7}$$

Also, from trigonometry, when $\theta = (\pi/2) - \phi$, we have

$$\tan\theta = \frac{1}{\tan\phi} \quad \text{and} \quad \theta = \tan^{-1}(\omega CR) \tag{3.8}$$

The instantaneous value of the voltage across capacitor (v_C), is given by

$$v_C = \sqrt{2}\,V_C \sin(\omega t - \theta) = (\sqrt{2}\,V\cos\theta)\sin(\omega t - \theta) \tag{3.9}$$

During the positive half-cycle when v_C hence v_G exceeds V_{GT} level, conduction of thyristor takes place (Fig. 3.6). In fact v_G is the rectified capacitor voltage. Thus α can be controlled over wide range (beyond 90°). By variation of R, phase angle (θ) as well as magnitude of v_C change, as shown in Fig. 3.6. Furthermore, the magnitude of v_G can also be controlled using the gate-current limiting resistor, R_2 (like resistance-trigger circuits). An improvement in the circuit configuration is possible when the RC branch is connected across the SCR. When the SCR conducts, the voltage across RC branch also reduces to a very low level (ideally zero). The power dissipation in the gate circuit therefore reduces significantly.

Example 3.2 A 240-V, 50-Hz supply is connected to an RC trigger circuit (Fig. 3.6). If R is variable from 1 kΩ to 22 kΩ, $V_{GT} = 2$ V and $C = 0.47$ μF, what are the minimum and maximum switching angle (α)?

Solution The phase angle of V_C is given by,

$$\theta = \tan^{-1}(\omega CR) = \tan^{-1}(2\pi fCR) = \tan^{-1}(2\pi \times 50 \times 0.47 \times 10^{-6} \times R)$$

Also,

$$v_C = V\cos\theta \quad \text{and} \quad v_C(\omega t) = \sqrt{2}\,v_C \sin(\omega t - \theta)$$

(i) When $R = 1$ kΩ, it gives $\theta = 8.4°$, $\cos\theta = 0.989$ and $v_C = 240 \times 0.989 = 237.4$ V. Therefore,

$$v_C(\omega t) = \sqrt{2}\,V_C \sin(\omega t - 8.4°) = 335.77 \sin(\omega t - 8.4°)$$

The conduction of SCR takes place at $\omega t = \alpha$, where $v_C = V_{GT} = 2$ V. Then

$$v_C(\alpha) = 2 = 335.77 \sin(\omega t - 8.4°) = 335.77 \sin(\alpha - 8.4°)$$

The minimum value of α is given by

$$\alpha_{min} = 8.4° + \sin^{-1}\frac{2}{335.77} = 8.7°$$

(ii) When $R = 22$ kΩ, it gives $\theta = 72.9°$, $\cos\theta = 0.294$ and $v_C = 240 \times 0.294 = 70.57$ V. Since,

$$v_C(\alpha) = 2 = \sqrt{2} \times 70.57 \sin(\omega t - 72.9°) = 99.8 \sin(\omega t - 72.9°)$$

The maximum value of α is given by

$$\alpha_{max} = 72.9° + \sin^{-1}\frac{2}{99.8} = 74°$$

HALF-WAVE TYPE

This circuit has been realized by incorporating an additional diode (D_2) in the circuit shown in Fig. 3.6. As illustrated in Fig. 3.7, the capacitor gets charged (upper plate negative) by v through D_2. The charging starts from negative-zero-crossover instant and continues up to the negative peak of v, i.e. $-\sqrt{2}$ V. Then the voltage at the anode of D_2 (i.e. v_C) becomes equal to the voltage at cathode (v). Therefore, the current through D_2 ceases and D_2 becomes reverse biased. Now the charging of capacitor takes place though R and the charging rate depends upon the time-period RC. When v_G (rectified v_C) becomes slightly higher than V_{GT}, conduction of the SCR takes place. Simply by controlling R, charging *rate of the capacitor* (*hence* α) *varies*. D_1 prevents large negative supply voltage to appear at the gate terminal of the thyristor. For wide range of α, charging of capacitor is required for almost (3/4)th time-period (T) of the supply voltage. However, for 50-Hz or 60-Hz mains-supply applications, an empirical equation had been reported as

$$RC \geq 0.65T = \frac{4}{\omega} \tag{3.10}$$

where the angular frequency of ac mains, $\omega = 2\pi/T$.

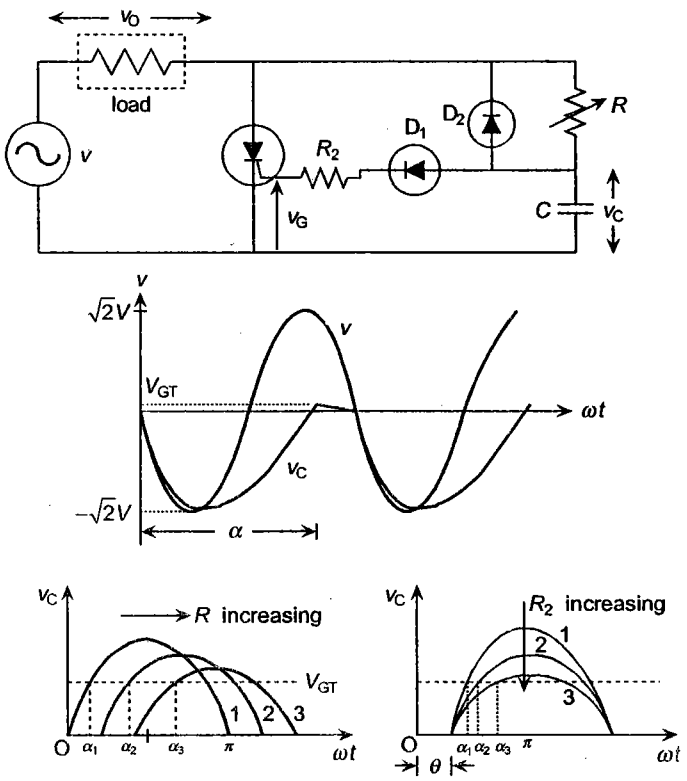


Figure 3.7 Another RC trigger circuit.

The value of R_2 is chosen such that the required I_{GT} and V_{GT} are supplied to the gate terminal and it is given by

$$R_2 \leq \frac{v - V_{GT} - V_D}{I_{GT}} \tag{3.11}$$

where v is the voltage at the switching instant of thyristor and v_D is forward voltage drop of diode, D_1.

Also, the maximum value of R_2 is given by

$$R_{2(max)} \leq \frac{\sqrt{2}V - V_{GT} - V_{D1}}{I_{GT}} \cong \frac{\sqrt{2}V}{I_{GT}} \tag{3.12}$$

With an approximation, the previous analysis of the trigger circuit holds good even for this case.

Full-wave Type

This circuit has been realized by incorporating a diode bridge in the previous circuit (Fig. 3.6). As illustrated in Fig. 3.8, charging of capacitor takes place through R and charging rate depends upon RC (time period). When v_G (rectified v_C) becomes slightly higher than V_{GT}, conduction of SCR takes place. Simply by controlling R, charging rate of capacitor hence α varies.

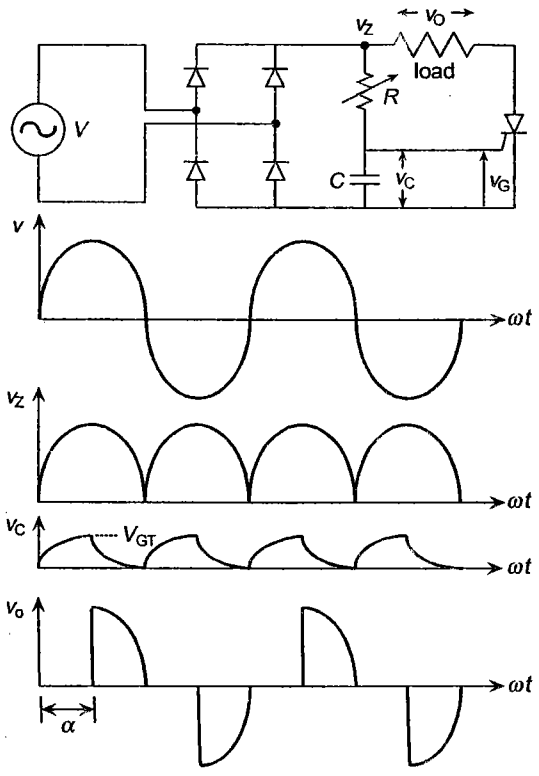


Figure 3.8 A full-wave RC trigger circuit.

Here in this circuit, charging of the capacitor starts from each zero-crossover instant and the capacitor experiences only a half-wave rectified voltage till the thyristor is triggered. The circuit can be analyzed by the complete response of an RC circuit with a sinusoidal (half-wave) excitation. The voltage expression is given by

$$v(t) = V_m \sin \omega t = Ri(t) + \frac{1}{C}\int i(t)\,dt \qquad \text{where } 0 \le t \ge \frac{T}{2} = \frac{\pi}{\omega} \tag{3.13}$$

Differentiating, we get

$$\omega V_m \cos \omega t = R\frac{di(t)}{dt} + \frac{i(t)}{C} \tag{3.14}$$

With zero initial condition, the total current response is given by

$$i(t) = \frac{V_m}{Z}[\sin(\omega t + \phi) - \sin\phi\, e^{-\omega t/\tan\phi}] \tag{3.15}$$

and

$$v_R(t) = i(t)R = \frac{V_m R}{Z}[\sin(\omega t + \phi) - \sin\phi\, e^{-\omega t/\tan\phi}] \tag{3.16}$$

$$= V_m \cos\phi\, [\sin(\omega t + \phi) - \sin\phi\, e^{-\omega t/\tan\phi}] \tag{3.17}$$

Also,

$$v_C(t) = v(t) - v_R(t) \quad \text{or} \quad v_C(\omega t) = v(\omega t) - v_R(\omega t) \tag{3.18}$$

As soon as v_C reaches V_{GT} level, the triggering of thyristor takes place.

Example 3.3 If the RC branch of Example 3.2 (and, as shown in Fig. 3.6), is used in a full-wave trigger circuit, what are the minimum and maximum switching angle, α?

Solution (i) When $R = 1$ kΩ, it gives $\phi = 90° - \theta = 81.6°$. Since,

$$v_C(t) = v(t) - v_R(t) = V_m \sin \omega t - V_m \cos\phi\, [\sin(\omega t + \phi) - \sin\phi\, e^{-\omega t/\tan\phi}]$$

We get

$$v_C(\omega t) = V_m \{\sin \omega t - \cos\phi\, [\sin(\omega t + \phi) - \sin\phi\, e^{-\omega t/\tan\phi}]\}$$

$$= \sqrt{2} \times 240 \{\sin \omega t - \cos(81.6°)\, [\sin(\omega t + 81.6°) - \sin(81.6°)\, e^{-\omega t/\tan 81.6°}]\}$$

Now, value of $v_C(\omega t)$ can be computed for $\omega t = 0$ to 180° by the direct substitution method. The required value of α corresponds to the condition when v_C becomes equal to $V_{GT} = 2$ V. It gives, $\omega t = \alpha_{min} = 2.5°$.

(ii) When $R = 22$ kΩ, it gives $\phi = 17.1°$. Therefore,

$$v_C(\omega t) = \sqrt{2} \times 240 \{\sin \omega t - \cos 17.1° [\sin(\omega t + 17.1°) - \sin 17.1°\, e^{-\omega t/\tan 17.1°}]\}$$

It gives $\omega t = \alpha_{max} = 11.35°$.

3.4.3 Diac Trigger Circuits

This circuit is commonly used for triac, where a trigger signal is required in both the half-cycles of the supply voltage (Fig. 3.9). Basically, it is similar to an RC trigger circuit (Fig. 3.6). Here

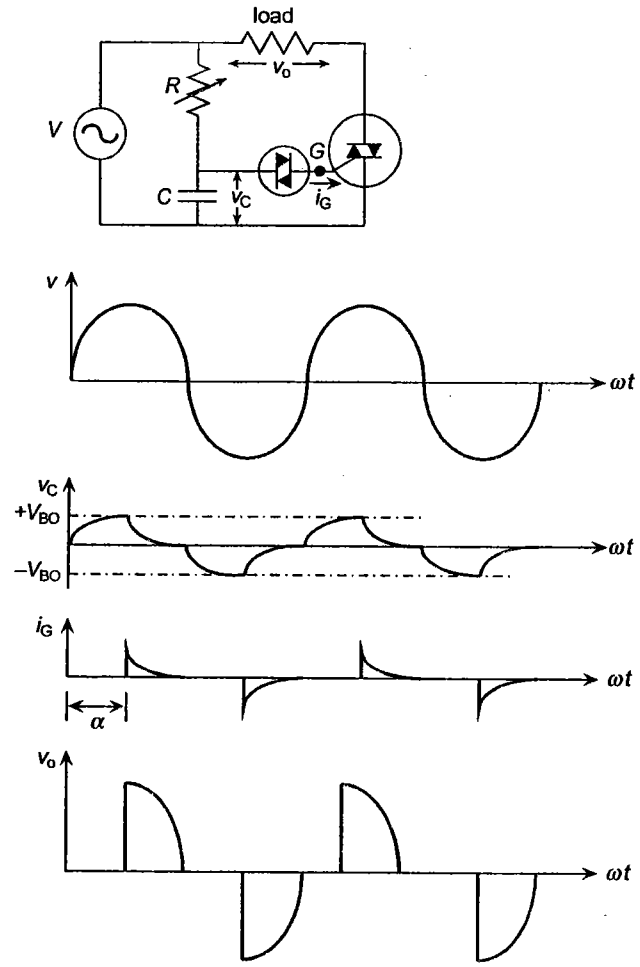


Figure 3.9 A diac RC trigger circuit used in ac regulators.

both SCR and diode D_1 are replaced by a triac and a diac, respectively. The capacitor gets charged through the resistance R during each half-cycle. When v_C reaches the break-over voltage of diac ($V_{BO} \cong 30$ V), conduction of the diac takes place and the required gate current is supplied. The triac conducts and the voltage across capacitor (hence v_G) collapses for the rest portion of the half-cycle. In the next half-cycle, same phenomenon repeats. Here, the triac conducts in the positive half-cycle by positive gate-current and in the negative half-cycle by the negative gate-current. Thus, triac operates in the first and third modes of its switching characteristics. However, gate sensitivity of triac is not same in both these modes. Therefore, for commercial circuits, an additional RC branch is added between the capacitor and diac, to make α same in both the half-cycles. In this circuit, the charging of the capacitor starts from each zero-crossover instant of the supply voltage. The RC circuit experiences only a half-wave voltage (before triggering of thyristor). As discussed in the previous section, this circuit can be analyzed by the total current response of an RC circuit with a sinusoidal (half-wave) excitation voltage.

Example 3.4 If the RC branch of Example 3.3 (Fig. 3.6) is used in a diac trigger circuit (with V_{BO} = 30 V), what are the minimum and maximum firing or switching angle, α?

Solution Equation (3.18) for v_C holds good even for this case. However, in this case, triggering takes place at $v_C(\omega t) = v_C(\alpha) = V_{BO}$ = 30 V, instead of V_{GT} = 2 V. Now, the value of $v_C(\omega t)$ can be computed for $\omega t = 0°$ to 180° by the direct substitution method, as was done for the previous case. A simple computer program in QBASIC is given below for diac trigger circuits to find the required value of α. It corresponds to the condition when v_C becomes equal to V_{BO}.

```
CLS
REM Program for switching angle, Alpha in diac trigger circuit
PRINT "Program developed by Jamil Asghar, EED, AMU, Aligarh, India"
PRINT "Give:  R in K-Ohm, C in uF, VBO of diac, Supply Voltage"
INPUT R, C, VBO, V
pi = 4 * ATN(1)
phi = ATN(1000 / (2 * pi * 50 * R * C))
Vm = SQR(2) * V
phid = phi * 180 / pi
FOR wtd = 0 TO 180 STEP 0.1
phi = pi * phid / 180
wt = pi * wtd / 180
vR1 = SIN(wt + phi) - SIN(phi) * EXP(-wt * TAN(phi))
vR = Vm * vR1 * COS(phi)
vC = Vm * SIN(wt) - vR
IF vC >= VBO GOTO 33
NEXT wtd
IF wtd >= 180 THEN PRINT  "NO TRIGGERING ---- VALUE OF RC TOO HIGH"
GOTO 44
33 PRINT "For diac: R in kOhms=", R, "C -in uF=", C, "VBO =", VBO
PRINT "Alpha in deg.=", wtd, "Phi -in deg=", phid, "vC=", vC
44 STOP
END
```

Result: (i) R = 1 kΩ, value of alpha = 11.33°, (ii) R = 22 kΩ, value of alpha = 46.5°.

3.4.4 AC-THYRATRON TYPE TRIGGER CIRCUITS

This trigger circuit is similar to the circuit shown in Fig. 3.6, except that the phase-shifting RC network is energized from a separate centre-tapped transformer. A simple RC trigger circuit suffers from the disadvantage that v_C does not remain constant for all values of θ (Fig. 3.6). Therefore, for higher values of θ (near 90°), v_C becomes very small, eventually it fails to trigger the thyristor. Thus the control range of α becomes small. While in this case, the rms value of the voltage v_B remains constant and its angle β varies from 0° to almost 30° (lagging), as shown in Fig. 3.10. From the phasor diagram of secondary of the transformer and the RC circuit,

$$\angle ADB = \frac{\pi}{2} - \phi = \theta \tag{3.19}$$

and since $V_{OA} = V_{OB}$, we have

$$\phi = \angle BAO = \frac{\pi}{2} - \angle ADB = \angle ABO \tag{3.20}$$

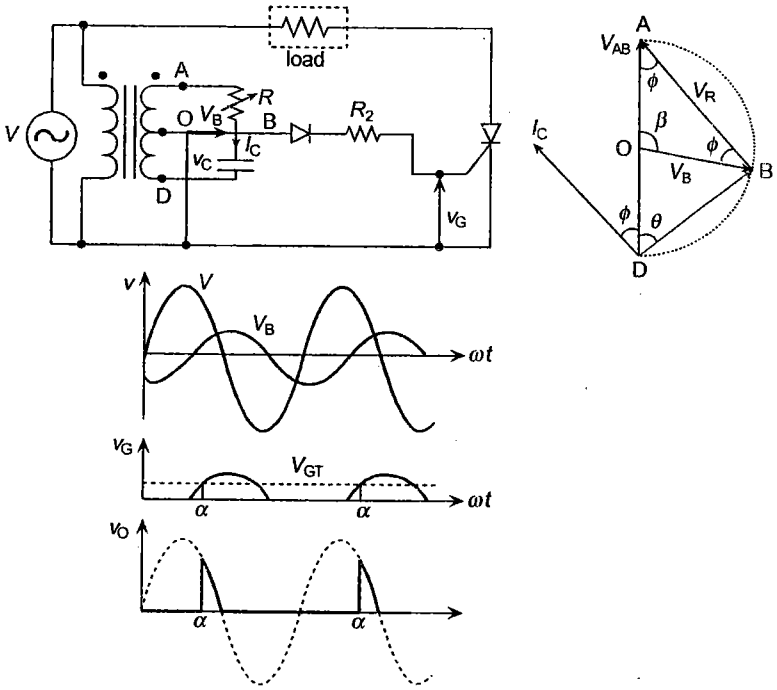


Figure 3.10 An ac-thyratron type trigger circuit.

Also, from triangle OAB,

$$\beta = \pi - 2\phi = 2\left(\frac{\pi}{2} - \phi\right) = 2\theta = 2\tan^{-1}(\omega CR) \tag{3.21}$$

The same circuit can also be used to trigger two thyristors in a bridge. In this case, gate current flows during the whole conduction period of the thyristor. It unnecessarily increases the temperature of gate-to-cathode junction (T_j), which may reduce voltage withstand (blocking) capability of the thyristor.

3.4.5 UJT-BASED TRIGGER CIRCUITS

An uni-junction transistor (UJT) based oscillator provides constant-frequency, sharp pulses with small rise-time. An UJT is a three-terminal, two-layer pn-device (Fig. 3.11). It has n-type semiconductor (between two base terminals B_1 and B_2) with a small p-type doping (at emitter terminal, E). The emitter terminal divides the inter-base resistance (V_{BB}) into two parts (say R_{B1} and R_{B2}). If a dc biasing voltage (V_{BB}) is applied across the base terminals, the voltage in n-type material, near emitter terminal (K), is given by

$$V_\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \eta V_{BB} \tag{3.22}$$

where η is called *intrinsic-standoff* ratio of UJT and its value is less than one (typical value varies between 0.5 and 0.8).

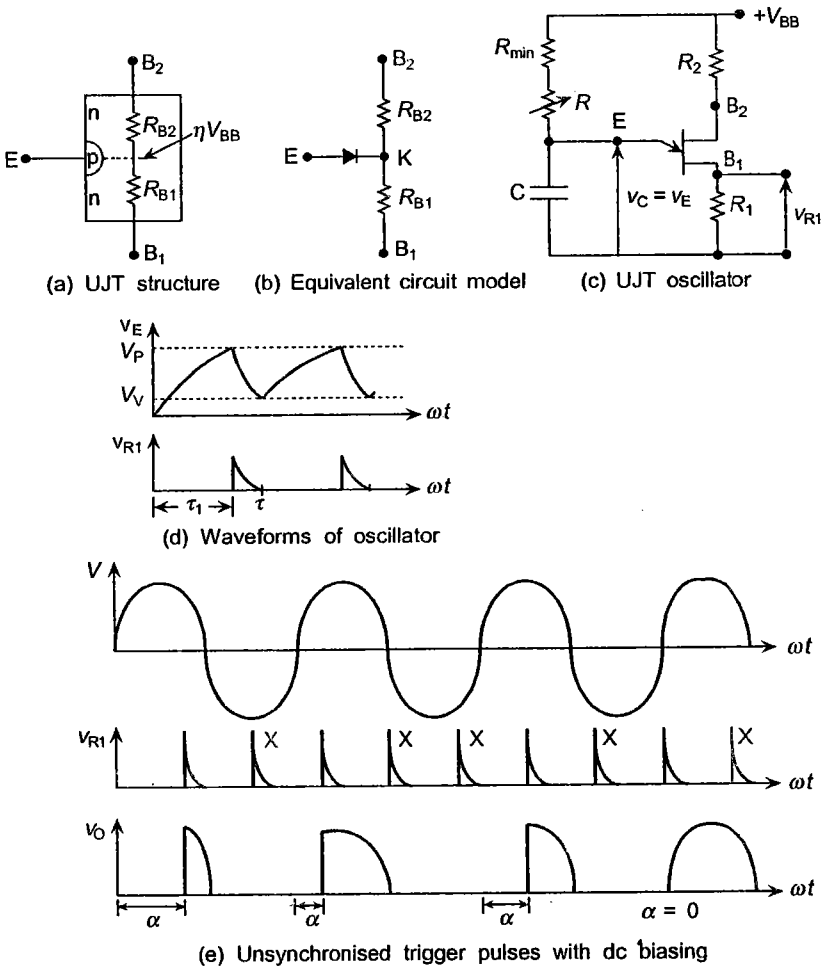


Figure 3.11 An UJT based oscillator circuit and waveforms.

When the emitter voltage (v_E) is less than v_k (or ηV_{BB}), E-B_1 junction behaves as a diode in reverse biased condition. Thus it offers a very high impedance. A small reverse leakage current (few micro-ampere) flows through the emitter terminal. An UJT based oscillator circuit is shown in Fig. 3.11c. When a dc supply voltage (V_{BB}) is connected, the charging of capacitor starts through resistance R_{min} and R. The voltage across capacitor, v_C (or v_E) increases. As soon as v_E slightly exceeds v_k or ($\eta V_{BB} + v_D$) level, the pn-junction behaves as a diode in forward-biased condition. Then emitter to Base1 impedance collapses and flow of a large current (i_E) through R_1 takes place. The capacitor gets discharged through R_1 and therefore a voltage pulse appears across R_1 (Fig. 3.11d). At the trailing edge of the pulse, v_E becomes very small (valley voltage, v_V), depletion layer forms again and pn-junction (between E-B_1) becomes reverse biased. Ideally, no current flows between E and B_1 terminals (except the reverse leakage current) and they behave like open circuited. Now charging of the capacitor starts and v_E again increases. The charging rate depends upon ($R_{min} + R$)C and discharge rate of capacitor depends upon R_1C. The delay period (τ_1) and the time period (τ) of the first pulse are related as

$$\tau = \tau_1 + R_1 C \tag{3.23}$$

and

$$\tau_1 = (R_{min} + R)\, C \ln \frac{1}{1 - \eta} \tag{3.24}$$

Also, the switching angle depends upon the delay period (τ_1) of the oscillator, which is given by

$$\alpha = \omega \tau_1 \tag{3.25}$$

However, in a trigger circuit, α may not be equal in each cycle of the supply voltage (v), as shown in Fig. 3.11e. Some pulses arrive when the thyristor is already conducting while some pulses arrive when the thyristor is in reverse biased condition. These pulses are marked 'X'. They do not have any contribution towards triggering of thyristor. Thus, α does not remain same, rather varies randomly in each cycle. To get a constant value of α, synchronization of the trigger pulse with supply voltage, is necessary. Figure 3.12 shows an UJT based trigger circuit synchronized with the supply voltage through a diode bridge. The charging of the capacitor starts from each zero-crossover instant only. The first pulse in each half-cycle that triggers the thyristor is synchronized with V, and therefore α becomes equal in each cycle. By controlling R, the time-period of oscillator (τ), or the delay period of the first pulse (τ_1), hence α can be adjusted. The UJT trigger circuit may also be energized from a separate transformer (for biasing and synchronization) and the same performance can be achieved.

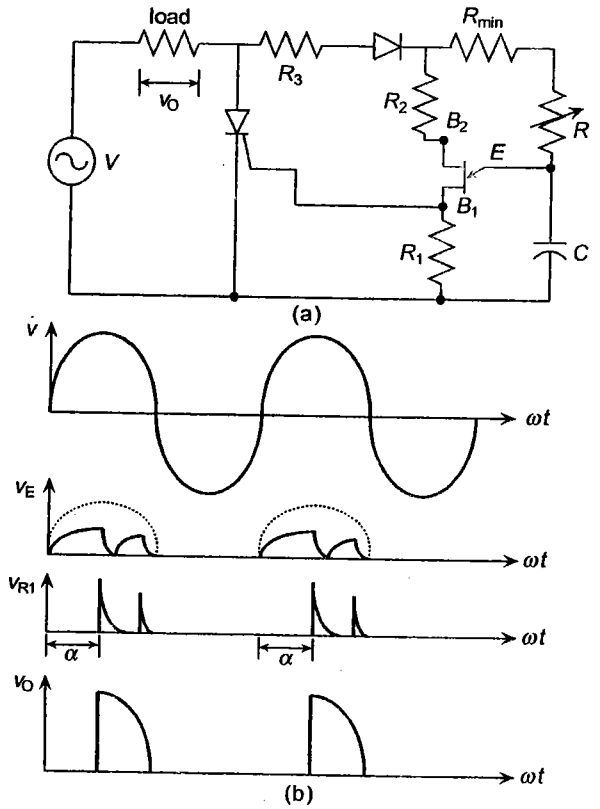


Figure 3.12 An UJT trigger circuit with waveforms.

DESIGN CONSIDERATIONS

Following are important design considerations:

1. Selection of R_1: It should be low enough to prevent undesirable triggering of the thyristor. Therefore, R_1 is related with the maximum gate-voltage (V_{GD}) that will not trigger the thyristor at any temperature,

$$V_{GD} \geq \frac{R_1}{R_1 + R_2 + R_{BB(min)}} V_{BB} \tag{3.26}$$

2. Selection of R_2: It is selected from the stability consideration of the circuit because the peak voltage (V_P) decreases with increase in temperature. The following equation gives the approximate value of R_2 for compensation over a temperature range of 40°C to 100°C:

$$R_2 = \frac{10^4}{\eta V_{BB}} \tag{3.27}$$

3. Selection of capacitor, C: It should store sufficient charge to trigger the thyristor. The typical values are between 0.01 and 0.7 μF. It can be calculated with the help of equations (3.23) and (3.24). The time period (τ) of the output pulse is $\tau_1 + R_1C$, while the delay period which corresponds to the switching angle (α) is τ_1, as given in (3.24).
4. Selection of R_{min}: It should be large enough so that the load line formed by R and V_{BB}, intersect the emitter characteristics of UJT to the left of the valley point. Therefore,

$$R_{min} \geq \frac{V_{BB} - V_V}{I_V} \tag{3.28}$$

5. Selection of R: The total charging resistance ($R + R_{min}$) must be sufficiently small to allow peak point current drawn from the supply. Therefore,

$$R_{max} = R + R_{min} \leq \frac{V_{BB} - V_P}{I_P} \tag{3.29}$$

Example 3.5 Following are the parameters and ratings of UJT (2N2646) at T_j = 25°C:

Maximum inter-base voltage (V_{BB})	= 35 V
Maximum average power dissipation	= 300 mW
Range of inter-base resistance (R_{BB})	= 4.7–9.1 kΩ (typical 5.6 kΩ at V_{BB} = 12 V)
Valley-point current, I_V	= 4 mA at V_{BB} = 20 V
Intrinsic stand-off ratio, η	= 0.56 to 0.75 (0.63 typical)
Valley-point voltage, V_V	= 2 V at V_{BB} = 20 V
Peak-point current, I_P	= 5 μA (maximum) at V_{BB} = 25 V
The maximum gate voltage (V_{GD}) that will not trigger-on the SCR	= 0.18 V

Design a suitable UJT based trigger circuit for a single-phase converter (rectifier) operating with a 50-Hz ac mains supply.

Solution The switching angle α varies from 0° to 180°, i.e. a half time-period of the ac mains supply. Therefore, the required maximum delay of the switching pulse is

$$\frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 50} = 10 \text{ ms}$$

Let $V_{BB} = 12$ V, then

(i) The minimum value of resistance

$$R_{min} > \frac{V_{BB} - V_V}{I_V} = \frac{12 - 2}{4 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

Take $R_{min} = 2.7$ kΩ (the nearest value of commercially available carbon resistor).

(ii) The peak-point voltage

$$V_P \cong \eta V_{BB} = 0.63 \times 12 \text{ V} = 7.56 \text{ V}$$

Then

$$R_{max} < \frac{V_{BB} - V_P}{I_P} = \frac{12 - 7.56}{5 \times 10^{-6}} = 888 \text{ k}\Omega$$

Then value of R is given by

$$R = R_{max} - R_{min} = 888 - 2.7 = 885.3 \text{ k}\Omega$$

Take $R = 1$ MΩ, then the new value of $R_{max} = 1002.7$ KΩ.

(iii) Selection of base-resistances: The empirical formula for R_2 is given by

$$R_2 = \frac{10000}{\eta V_{BB}} = \frac{10000}{0.63 \times 12} = 1.32 \text{ k}\Omega$$

The nearest value of commercially avalable resistor is selected, i.e. $R_2 = 1.2$ kΩ. Then R_1 can be found as

$$\frac{V_{BB}}{R_1 + R_2 + R_{BB(min)}} R_1 < V_{GD}$$

or

$$\frac{12}{R_1 + 1200 + 5600} R_1 < 0.18$$

It gives, R_1 is less than 103 Ω. Therefore, take $R_1 = 100$ Ω.

(iv) Selection of capacitor: Let the triggering circuit is designed for a maximum delay period, i.e. 10 msec. The maximum delay period corresponds to the minimum frequency of oscillator, which is given by

$$\tau = 10 \text{ ms} = R_{max} C \ln \frac{1}{1 - \eta}$$

Therefore,

$$C = \frac{10^{-2}}{R_{max} \times \ln[1/(1 - \eta)]} = \frac{10^{-2}}{1002.7 \times 10^3 \ln[1/(1 - 0.63)]} = 0.01 \text{ μF}$$

Although a capacitor of 0.01 μF can be selected but the pulse-width of the triggering pulse will be small ($R_1C = 100 \times 0.01 = 1$ μs). Sometimes, this may not be sufficient to trigger a thyristor successfully. Then it should be increased (about 5 μs). Moreover, sometimes, the voltage

(peak) across R_1 may not be sufficient to drive the thyristor, then the value of R_1 has to be increased.

The minimum delay period (ideal) is given by

$$\tau_{min} = R_{min}C \ln \frac{1}{1-\eta} = 2.7 \times 10^3 \times 0.01 \times 10^{-6} \times 0.99425 = 0.0268 \text{ ms}$$

where

$$\text{Minimum value of } \alpha = \text{Minimum delay period (in ms)} \times \frac{360°}{20 \text{ ms}} = \frac{0.0268 \times 360}{20} = 0.483°$$

Similarly, the maximum delay period (ideal) is given by

$$\tau_{max} = R_{max}C \ln \frac{1}{1-\eta} = 1002.7 \times 10^3 \times 0.01 \times 10^{-6} \times 0.994 = 9.967 \text{ ms}$$

The maximum value (ideal) of α is given by

$$\alpha_{max} = \text{Maximum delay period (in ms)} \times \frac{360°}{20 \text{ ms}} = \frac{9.967 \times 360°}{20} = 179.4°$$

3.4.6 Advanced Triggering Circuits for Thyristors

Although RC trigger circuits are very simple and economical, but they depend upon gate trigger characteristics of the thyristor used. They cannot be easily used in self-programmed, automatic or feedback controlled systems. Since the use of power-electronic controllers are increasing steadily in industry as well as in power systems, different types of controllers are required for specific applications. In a controller, a group of thyristors or power-semiconductor devices are required to be switched at different switching instants for different durations and with a particular sequence. Different three-phase converters—dual converters, cyclo-converters and regenerative reversible drive—may require twelve to thirty-six number of such devices. Thus switching a large number of these power devices with different control strategies by a simple trigger circuit becomes almost impossible. Moreover, incorporation of feedback and/or different control approaches for same load/drive system requires an intelligent controller. The advanced triggering circuits therefore become necessary.

Some modules of power semiconductor devices include gate drive as well as transient protection circuitry. Commercially available such modules are called *intelligent module* or *smart power*. They include input–output isolation and gate drive circuits, microcomputer control, a protection and diagnostic circuit (for over-current, short circuit, open load, overloading and excess voltage) and a controlled power supply. Similarly custom-built driver ICs are also available for thyristors as well as MOSFET and IGBT.

3.4.7 Driver and Buffer Circuits for Thyristors

In most of the power electronic circuits, difference of potential exists between the gates of the various thyristors, as well as between the control circuit and thyristors. The control electronics normally consist linear ICs (e.g. operational amplifiers, timers) and digital ICs (e.g. TTL, CMOS), discrete passive elements and active devices. Basically, they are low-voltage (few volts) and low-power (few watts) circuits. The power circuit, which consists thyristors, is a high-voltage circuit

(normally of the order of several hundreds of volts) circuit. Therefore, it becomes necessary for the output channels of the gate-pulse generating circuit to be isolated from one another as well as from thyristors. The isolation can be provided either by a small high-frequency pulse transformer or by an opto-coupler IC. Then it becomes possible to switch on several thyristors together (e.g. in a series connection or switching an ac load by two anti-parallel thyristors). Similarly control electronics, which controls the conduction period of each thyristor, gives an output of very low power (few milli-watt, e.g. the output of a CMOS logic gate). In general, in most of the cases, output power is not sufficient to drive the gate directly. Therefore, an amplifier circuit is required which amplifies the weak gate drive control signal. For this purpose, a transistor amplifier is used.

For isolation between control and power circuit, use of a pulse-transformer is common. Normally, it has two or three windings. It is a small low power and high-frequency transformer. The turns-ratio are normally 1:1 or 2:1. When the high frequency pulse is applied to the primary winding, then output pulse appears at one or more output secondary windings. An opto-coupler IC circuit is also used for this purpose. In this arrangement, infra-red light-emitting diode (I-LED) turns on a photo-sensitive device (photo-SCR, photo triac, photo logic gate, or photo transistor), which ultimately turns on the thyristor. However, a separate dc power supply is normally required for each thyristor. For high-voltage applications, an optical-fibre technique is applicable. In this case, output of control electronic circuit is supplied in the form of light signal through optical-fibre cable to the thyristor. Optical-fibre offers very high level of insulation between control circuit and power circuit consisting of thyristors.

Figure 3.13 shows different driver and buffer circuits (DBC). In Fig. 3.13a, pulses are generated by a differentiator circuit (R_1C), which converts a step input signal into sharp positive and negative pulses. Then a transistor-amplifier circuit amplifies the positive pulse. A pulse-transformer provides the isolation. Diode D_3 allows only positive portion of the amplified signal to be applied between gate and cathode terminals of a thyristor. D_2 provides a freewheeling path for the inductive current of the primary winding of the pulse transformer. Thus protects the transistor from high voltage spikes that could be generated due to snap of inductive current (Ldi/dt) by turn-off of the transistor.

The anode current of a thyristor reaches the latching current level after certain delay period. Therefore, for an inductive load, a long pulse is required for a successful triggering. For this purpose, a capacitor is connected in parallel with R_2. However, to avoid saturation of core of the pulse transformer due to stretched unidirectional current, the pulse duration is restricted to 50 μs to 100 μs.

Often in converter circuits with inductive loads, the load current is discontinuous within the assigned conduction period and therefore it is required to trigger the thyristor more than once. Similarly, conduction period (or commutation instant) of each thyristor depends upon the load current flowing through it, which varies with respect to load power factor. Therefore, for a reliable triggering, a continuous gate signal is required but it increases thyristor losses and decreases voltage withstand or blocking capability. Alternatively, a train of trigger pulses of high frequency (e.g. 10 kHz) is supplied during whole conduction period. In this case, the switching may be delayed by one time period (0.1 ms for 10 kHz signal) of the pulse train. However, this delay is negligible for power frequency (e.g. 1.8° for 50 Hz or 2.0° for 60 Hz).

Figure 3.13b shows a commonly used driver and a buffer circuit (DBC). A high-frequency (5–20 kHz) positive pulse (or square wave signal) from an oscillator is applied to an AND gate continuously. These pulses are enabled to reach the base of transistor only when the input drive control signal is high. The transistor basically acts as a switch to energize the primary winding of the pulse transformer corresponding to each pulse. Moreover, these pulses are amplified, too. Their

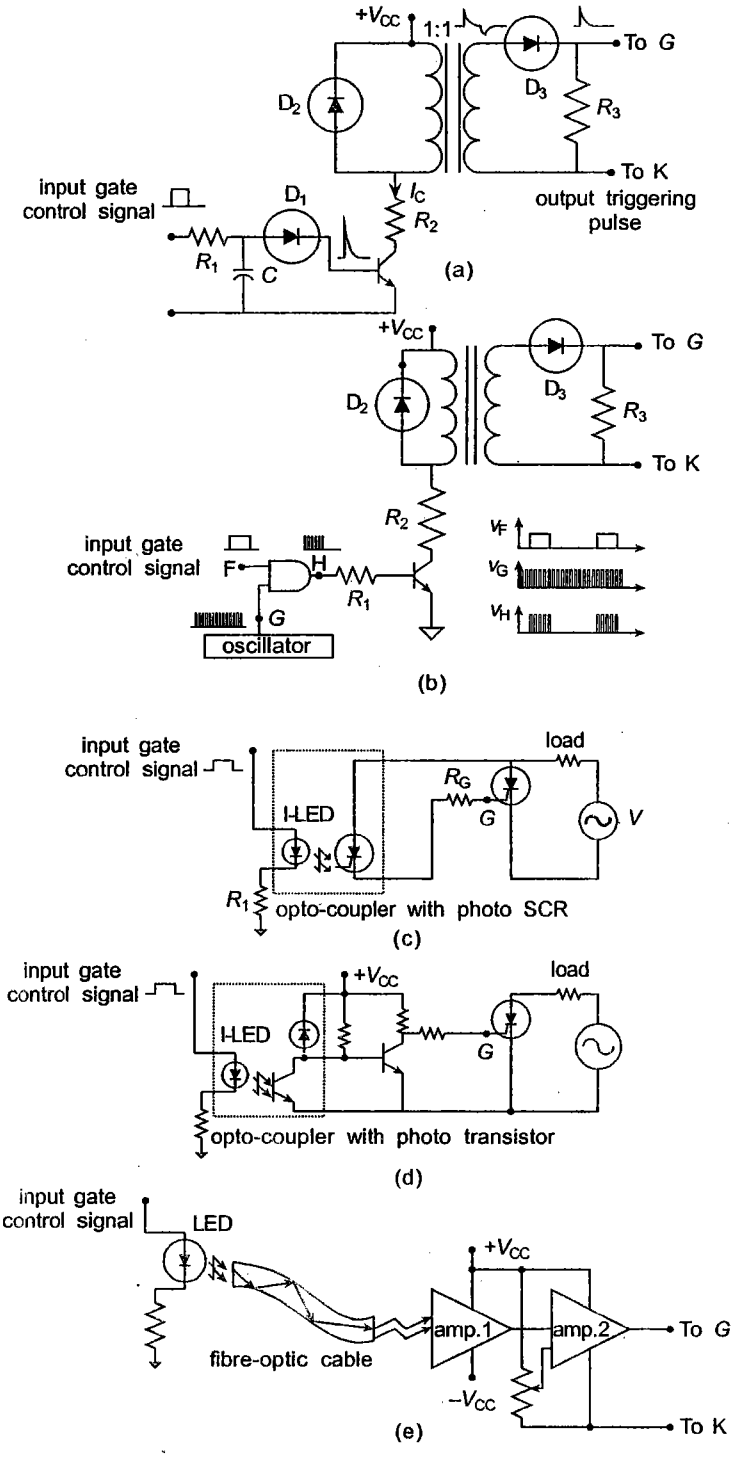


Figure 3.13 Driver and buffer circuits for thyristors.

magnitudes are restricted by the current-limiting resistor (R_2), which is connected in series with the dc source. In the secondary windings, pulses of almost same strength are produced due to the transformer action. The snap of inductive current in primary winding (when the transistor is switched off) generates a negative pulse in the secondary winding. This pulse is blocked by the diode D_2. Thus amplified positive pulses become available between G and K terminals of the thyristor.

Figure 3.13c shows an opto-coupler IC chip based isolation circuit. An infrared light-emitting diode (I-LED) and a photo-SCR are fabricated in a single IC chip. On arrival of the gate control signal, I-LED conducts and emits light to bring photo-SCR into conduction mode. Thus switching of the main SCR takes place.

Figure 3.13d shows another opto-coupler based circuit where photo-transistor is used. Since the output current of the photo-transistor is not sufficient to drive a thyristor, an additional transistor (BJT) is used for amplification. This type of circuit requires an additional electrically isolated dc power supply for each thyristor.

Figure 3.13e shows a fibre optic cable based driver circuit. It provides very high electrical isolation and a large creepage-distance, which is required in between low power control circuit and high-voltage power circuit. In case of an opto-coupler, I-LED and the receiving photo-transistor both are fabricated on the same IC chip. Therefore, the capacitance between them should be as small as possible to avoid re-triggering at both turn-on and turn-off of the power devices (e.g. power transistors, power MOSFET and IGBT), due to jump of potential across the devices (*dv/dt*). To avoid this problem, the fibre optic technique is used. The amplifier-1 is a receiver (fibre optics integrated detector/pre-amplifier). The second amplifier amplifies the control signal to the required level for triggering of the thyristor. Here the driver circuit is linked to the control circuit only through the fibre optic cable, thus galvanic isolation is provided between them.

Example 3.6 Design a suitable pulse transformer based driver circuit for a given SCR. The worst-case requirements of the SCR are given as: I_{Gmin} = 100 mA, V_{Gmin} = 2.5 V, @ –65°C.

The input drive control signal is an output of AND gate (IC7408). The specification of a TTL gate (general type) is given by

Output current and voltage at logic '1' level: I_{OH} = 0.4 mA, @ V_{OH} = 2.4 V

Output current and voltage at logic '0' level: I_{OL} = 16 mA, @ V_{OL} = 0.4 V

Solution The gate current requirements of thyristor are important for the design considerations. Then the desired gate current, hence secondary current of the pulse transformer (I_2), should be 100 mA. Let the turns-ratio of the pulse transformer is 2:1 (Fig. 3.13b). Therefore, the primary current (I_1) of the pulse transformer can be taken as

$$\frac{I_2}{I_1} = \frac{2}{1} \quad \text{or} \quad I_1 = \frac{100}{2} = 50 \text{ mA}$$

Here the maximum output current of TTL IC is limited to 0.4 mA for logic '1' level. Neglecting the small V_{BE} voltage drop during the switching of the transistor, we have

$$R_B \geq \frac{V_{OH}}{I_{OH}} = \frac{2.4}{0.4 \times 10^{-3}} = 6 \text{ k}\Omega$$

We thus choose, R_B = 6.8 kΩ.

For this purpose, a switching transistor (BC 107, BC 148, BEL100N, 2N2222 or similar) may be selected according to voltage and current ratings (V_{CC} and I_C). Let BEL100N (or SL 100) transistor is taken, whose specifications are: $V_{CBO(max)}$ = 60 *V*, $I_{C(max)}$ = 500 mA, h_{fe} (at I_C = 150 mA, V_{CE} = 1 V, T_j = 25°C) = 50 to 280.

Since the required primary winding current of the pulse transformer, $I_1 = I_C$ = 50 mA, the value of resistor R_1 (which is used to limit the collector current within allowable range), is given by

$$R_1 = \frac{V_{CC}}{I_C} = \frac{12}{50 \times 10^{-3}} = 240\ \Omega$$

We choose, R_1 = 220 Ω. Then

$$\text{Power rating of the resistor} = I_C^2 R_1 = (50 \times 10^{-3})^2 \times 220 = 0.55\ \text{W}$$

Therefore, a 220-Ω, 1-W resistor will be a good choice.

3.5

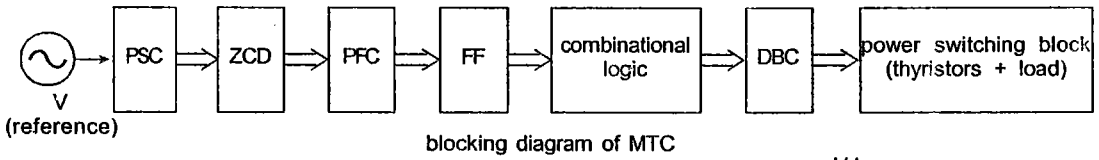
A MASTER TRIGGERING CONTROL (MTC) CIRCUIT

The block diagram of a master triggering control (MTC) circuit is shown in Fig. 3.14. It has blocks of phase-shifting circuits (PSC), pulse-forming circuits (PFC), *SR* flip-flops (FF), digital combinational logic circuits and driver and buffer circuits (DBC). Several phase-shifted signals (leading or lagging) are generated by adding more RC series branches at the secondary of a centre-tapped auxiliary transformer (audio inter-stage coupling transformer, Delta 13A74A), as shown in Fig. 3.14a. With respect to *V*, these voltage signals, V_1, V_2 and V_3 are phase shifted by the required angle θ_1, θ_2 and θ_3 respectively. A pulse-forming circuit (PFC) gives a sharp positive pulse at each positive zero-crossing instant (ZCI) of the input ac voltage (V_1, V_2 or V_3). The pulse generated at ZCI sets or resets a FF. The outputs of different FF are connected to different logic gates. The output of these logic gates reaches different DBC according to the required logic combinations. Thus amplified trigger pulses reach the gate of a particular thyristor through the pulse transformer.

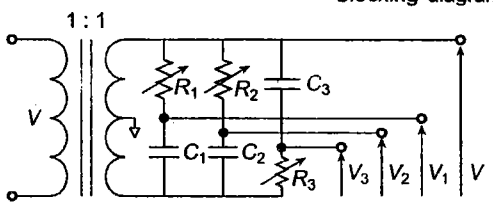
Chopper control For time-ratio control (TRC) of a dc-to-dc chopper, two ac signals V_2 and V_3 are generated by two PSC of MTC (Fig. 3.14b). The frequency control is achieved by varying the frequency of the reference voltage (*V*) supplied from the sine-wave oscillator. The duty-cycle control is achieved by the phase-difference. The phasor positions of V_2 and V_3 are controlled by varying R_2 and R_3 respectively. It varies from 0 to almost equal to π (lagging and leading). The control pulse at the positive ZCI of V_2 (i.e. at θ_2), sets the FF, and the other pulse at θ_3 resets it. Q_1 and Q'_1, the outputs of FF, reach the main SCR and the auxiliary SCR through two DBC. The phase-difference, $\theta_3 - \theta_2$, corresponds to the desired duty-cycle of the chopper. Thus, the phase-difference of 90°, 180° and 270° correspond to 25%, 50% and 75% of duty-cycle, respectively. The duty cycle of the chopper is given by

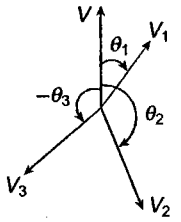
$$\text{Duty-cycle} = \frac{\theta_3 - \theta_2}{2\pi}$$

Therefore, the duty-cycle can be continuously controlled from 0 to 100%.

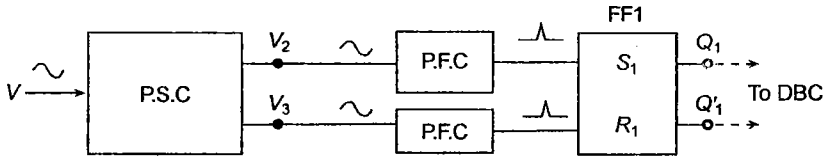


blocking diagram of MTC

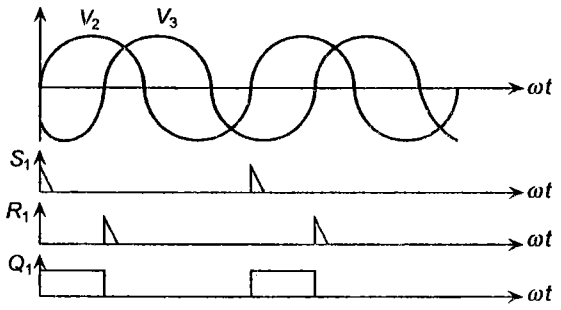




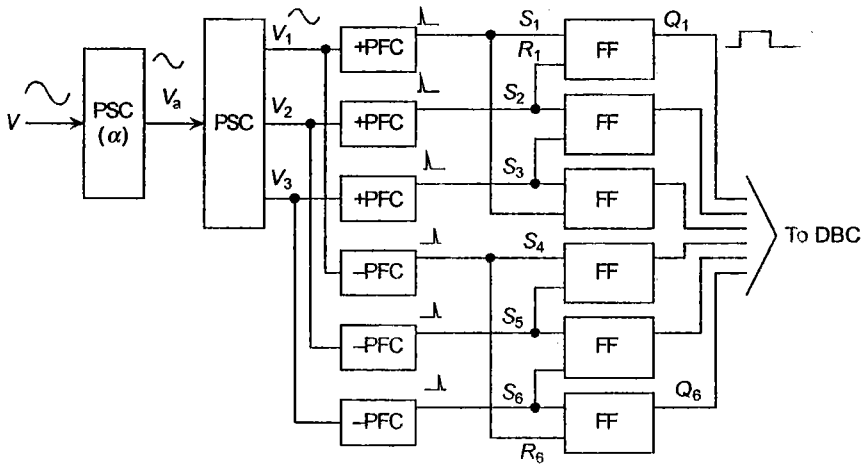
PSC with phasor diagram



(a) MTC connection for chopper



(b) MTC connections and waveforms for chopper



(c) An MTC in converter/inverter mode

Figure 3.14 A master triggering control circuit.

Bridge converters/inverters For single-phase and 3-phase converters/inverters, four and six thyristors are used, respectively. Thus four and six switching signals are required. Figure 3.14c shows connections of MTC for 3-phase applications (120° conduction mode). Here V_1, V_2 and V_3 are adjusted at 0°, 120° and 240°. Each of them is applied to two PFC. A positive group PFC generates a positive pulse at the positive ZCI. While a negative group PFC generates a positive pulse at the negative ZCI. Thus control pulses are available at 0°, 120°, 240°, 180°, 300° and 60°, which are used to set or reset a FF for the desired duration. During this period, the triggering pulses reach the gate of a thyristor through DBC. The output voltage, hence the switching-angle control, is accomplished by the variation of the phase-angle (α) of V_a with respect to the reference voltage (V). Here V_a is generated with the help of an additional PSC. In this way, pulses at positive ZCI of all voltage signals (reaching PFC) shift by α. This MTC can also be used for a 3-phase ac voltage controller by rearranging output signals from each FF and connecting SCR in anti-parallel mode.

3.6 SOME PRACTICAL TRIGGERING CIRCUITS

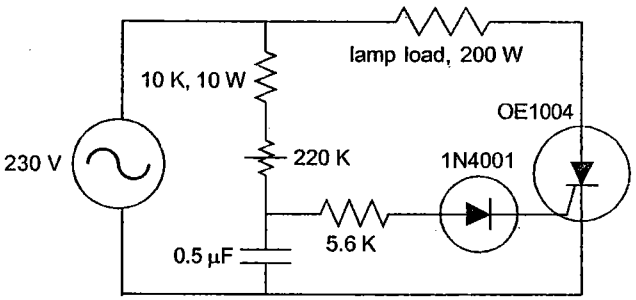
Actual triggering circuits highly depend upon the type as well as rating (power handling capability) of the thyristors. However, the basic circuit configuration does not change significantly. Figures 3.15–3.17 show different types of triggering circuits for thyristors.

3.6.1 Simple Triggering Circuits

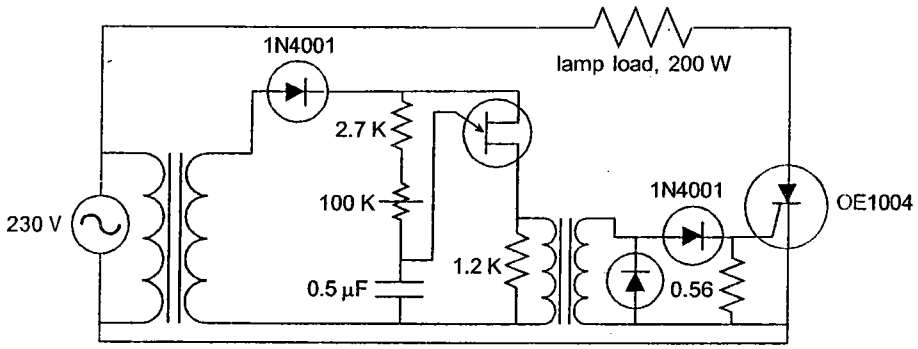
Figure 3.15a shows a simple R and RC trigger circuit for an SCR. The beginning of conduction (switching) of SCR depends upon the magnitude of the gate current as well as the magnitude of the anode-to-cathode voltage (v_{AK}). The magnitude of gate-current can be controlled using a variable resistance only (without capacitor). It controls the switching-angle up to 90°. Similarly, the switching-angle can also be controlled using a simple RC phase-shifter circuit. Thus the positive half-cycle of the capacitor voltage (rectified voltage), controls the switching-angle even beyond 90° and up to about 150°.

Uni-junction transistor (UJT) based oscillator is shown in Fig. 3.15b for triggering of an SCR. The transformer (230/12 V) supplies dc power as well as synchronizes the oscillator circuit with the ac mains. Therefore, the charging of capacitor starts only after the positive zero-crossing instant (ZCI) of the voltage signal. Hence, the first sharp pulse (that triggers the thyristor) is generated with reference to ZCI of the voltage, and not arbitrarily. For the higher frequency settings of the oscillator (using 100-kΩ pot.), the switching-angle (α) is small. While for the lower-frequency settings, α is high. Thus very wide range of control of α (nearly zero to almost 180°), is possible. For the negative group of SCR, a centre-tapped transformer and another pulse transformer may be used.

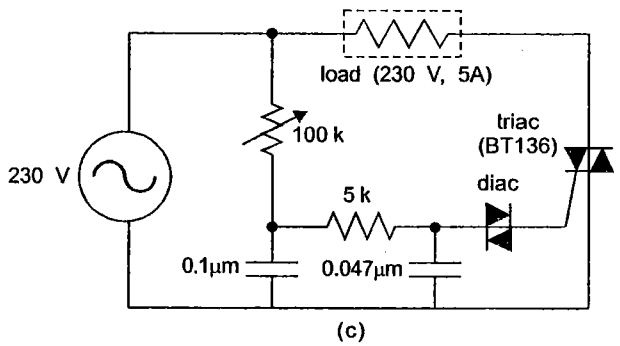
Figure 3.15c shows a diac based trigger circuit. Its performance is better than the previous circuit shown in Fig. 3.9. In this case, an RC branch is added to make the switching-angle same in both the half cycles.



(a) A simple R and RC trigger circuit



(b) UJT oscillator based trigger circuit



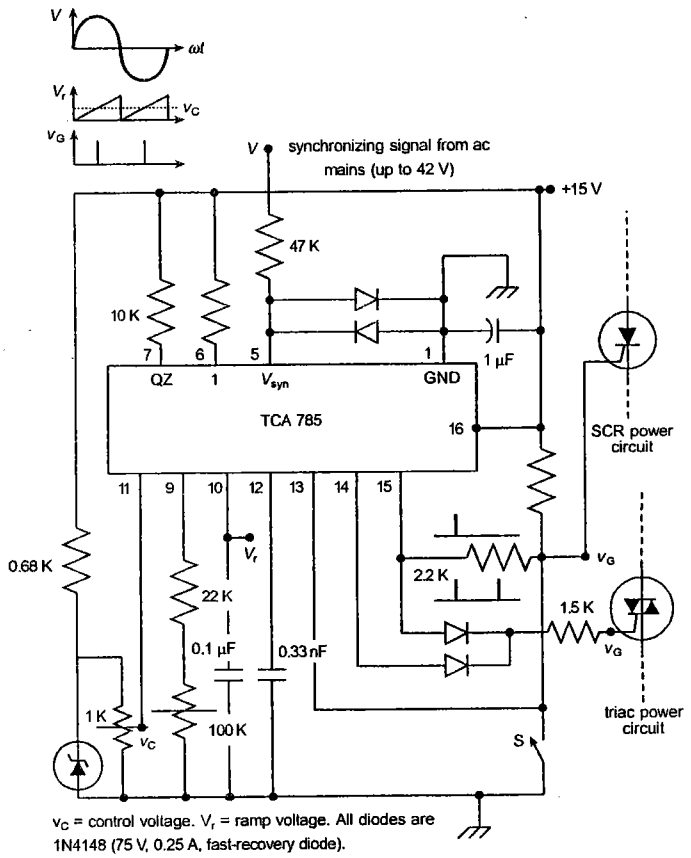
(c)

Figure 3.15 Simple triggering circuits.

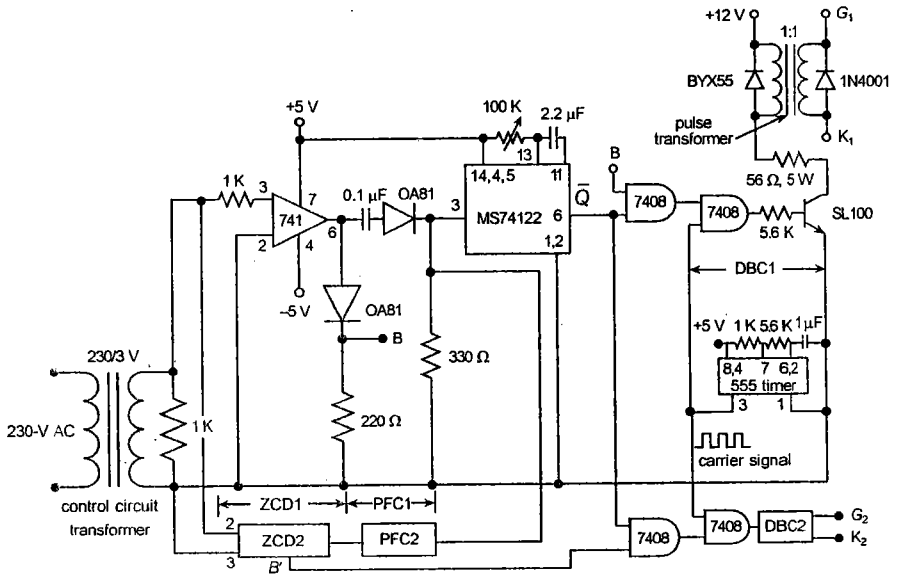
3.6.2 IC-BASED ADVANCE TRIGGERING CIRCUITS

For accurate switching angle control and to incorporate feedback control signals, advance triggering circuits are used. For a single-phase ac regulator, semi or full converter/inverter, the triggering pulses are required for two or four thyristors (SCR). They form two groups, i.e. positive group and negative group. The on-period or duration for which the triggering pulses are available to the gate of thyristors depends upon the delay or the switching angle (α) of each group.

Figure 3.16a shows a custom-built integrated circuit TCA785 used for triggering of thyristors (SCR, triac and thyristor bridges). It can also be used for driving MOSFET/IGBT. A



(a) TCA785 based trigger circuit for SCR and triac



(b) A monostable based trigger circuit

Figure 3.16 IC-based advance triggering circuits.

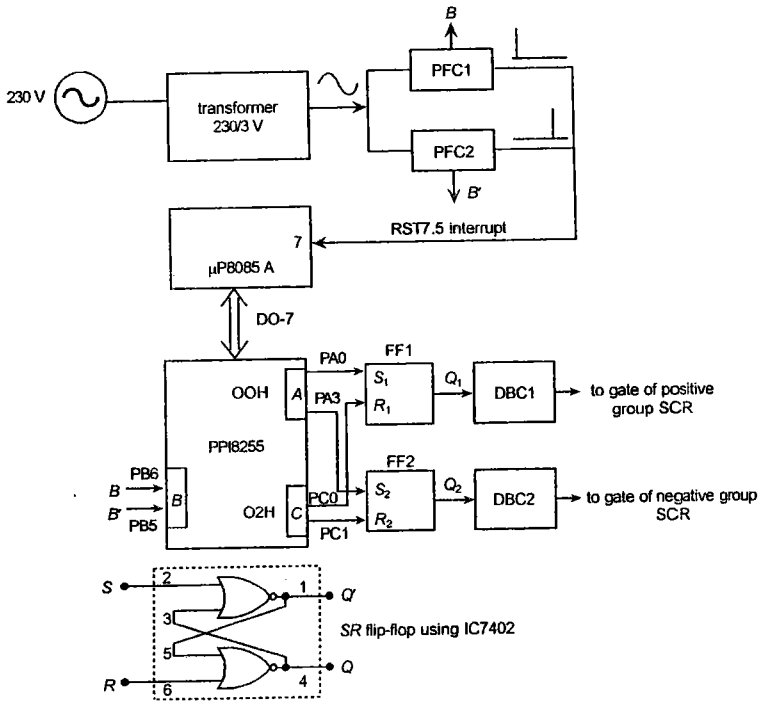
transformer (230/24 V) supplies dc power to the IC and synchronizes it with the ac mains. This IC can also incorporate feedback signals for an automatic control application. A ramp signal is generated inside the chip. When the control signal becomes equal to the ramp signal, the IC generates a trigger pulse. The trigger pulses become available in the positive half-cycle (pin 15) as well as in the negative half-cycle (pin 14).

A retriggerable monostable (IC74122) based triggering circuit is shown in Fig. 3.16b. It contains, zero-crossing detector (ZCD) based pulse-forming circuits (PFC), a monostable, digital-logic gates and DBC. A pulse generated at both positive and negative ZCI (using ZCD1, PFC1 and ZCD2, PFC2 respectively), sets the monostable at the positive edge of each pulse. An RC delay network controls the output (Q) of the mono stable for which it remains 'high'. The high level of Q' corresponds to the required duration of the triggering signal (α to π and $\pi + \alpha$ to 2π). It is used to control α, and hence the output voltage. During the positive half-cycle, both B and Q' are high and they (AND output) are used for triggering the positive group thyristors (using DBC1). Similarly, AND output of B' and Q' is used for the negative group of thyristors (using DBC2). A 555 timer based astable multivibrator, generates carrier signals (about 7 kHz) for DBC1 and DBC2. The amplified pulses ultimately reaches the gate of a thyristor through the pulse transformer.

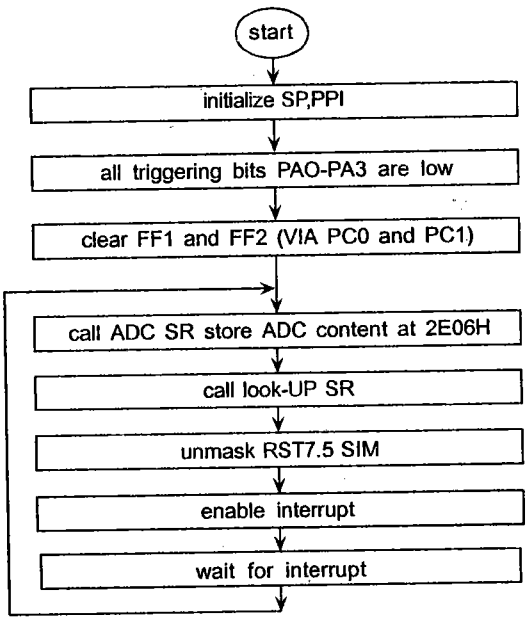
3.6.3 Microprocessor-based Trigger Circuits

The block diagram and flowchart of operation of a microprocessor (μP)/microcomputer based triggering circuit is shown in Fig. 3.17. This scheme is based on a synchronization circuit, a programmable peripheral interface PPI8255, an 8085 μP based microcomputer system, SR flip-flops (FF) and driver and buffer circuits (DBC). The delay-period is controlled by a software (delay subroutine). By look-up table approach for a given voltage, the value of α can be obtained. The duration of the trigger pulses varies from supply voltage to zero, for $\alpha = 0°$ to $180°$. The maximum duration is one-half of time-period of ac mains, i.e. 10 ms for 50 Hz or 9 ms for 60 Hz. Two pulse-forming circuits (PFC) are used for synchronization of the triggering pulses with the voltage wave. PFC1 and PFC2 generate a sharp positive pulse, at the positive ZCI and negative ZCI, respectively. These pulses are supplied to RST7.5 interrupt of μP (at pin 7). Since RST7.5 responds to a positive edge of the control signal, RST7.5 interrupt is obtained at both positive ZCI and negative ZCI. The flowchart of the main program and the interrupt service subroutine (ISS 7.5 of RST) are also given.

Initially μP and PPI are initialized along with variables used. Then, the value of the desired output voltage is fed through an 8-bit ADC. The switching angles, α and $(\pi + \alpha)$, are calculated, through look-up table approach. In the main program, RST7.5 interrupt is unmasked and on acknowledgment, the interrupt service subroutine (ISS) is serviced. The subroutine includes a reset command for each FF connected to DBC, through the control ports (PC0 and PC1 of PPI8255). The register pair DE is loaded with a delay count. When the delay or down-counting completes, μP issues a control signal to set FF1 and FF2 for each positive and negative group of thyristors, respectively. Ultimately, Q_1 and Q_2 enable the amplified triggering pulses to reach the gate of SCR through DBC1 and DBC2, respectively.

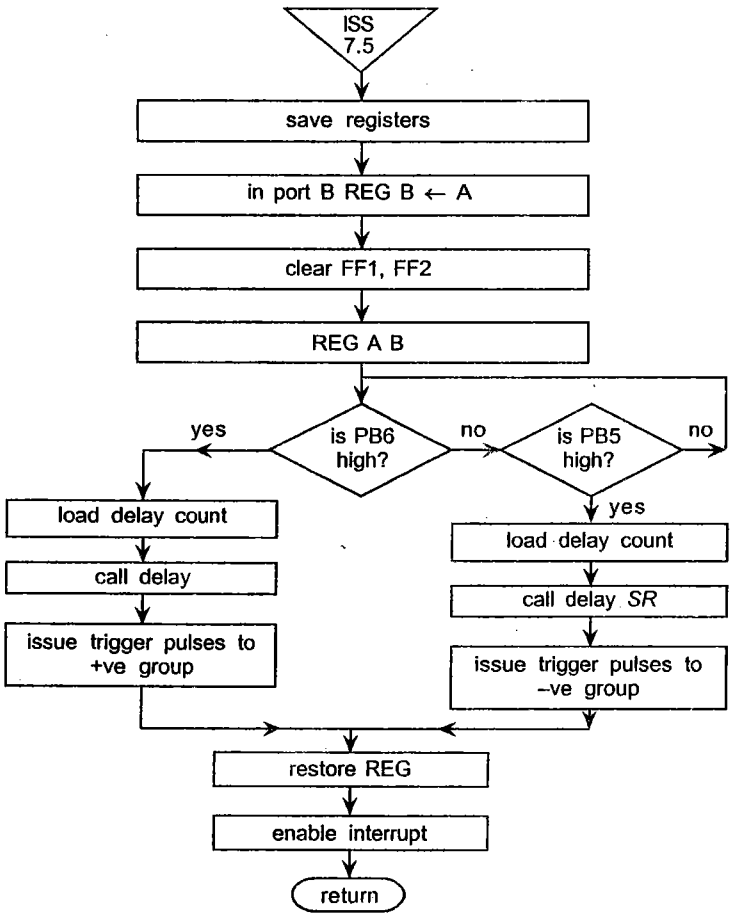


(a) Block diagram of circuit



(b) Flow chart: main program

Figure 3.17 (*Cont.*)



(c) Interrupt service subroutine (ISS) 7.5.

Figure 3.17 A microprocessor based trigger circuit.

SUMMARY

A triggering signal is required for every thyristor to turn it on. A wide range of gate-drive or triggering circuits are available from simple and cheap R and RC circuits to digital/ microprocessor based circuits. A thyristor can be triggered by a single, very low-power, sharp pulse. However, in general, for reliable operation of the converter/controller, they are triggered by a train of pulses for the whole on-period. Advance trigger circuits are used for an accurate control of switching angle and to incorporate a feedback control signal. Normally, analog and digital IC are used to realize such circuits. However, the power-output of such IC is not sufficient to drive a thyristor. Therefore, driver and buffer circuits are used to amplify the weak control signals (from IC) and to isolate low-voltage control circuit from high-voltage power circuit.

REVIEW QUESTIONS AND PROBLEMS

1. What are the conditions for successful switching (turn-on) of an SCR?
2. How do the gate requirements of a triac vary from an SCR?
3. What are the advantages of a sharp gate signal for an SCR?
4. What are drawbacks of a resistance-triggering circuit?
5. Why an *RC* triggering circuit cannot be used for α close to 180°?
6. Find suitable values of *R* and *C* for an UJT based trigger circuit for $\alpha = 0°$ to 120°.
7. How feedback signal can be used to control α in a TTL-based triggering control circuit?
8. Show connections of PFC, FF and logic circuits in MTC for a 3-phase ac voltage controller using MTC.
9. For a 1-phase ac voltage regulator (using phase-controlled switching), suggest suitable changes in the hardware and software of μP-based triggering system, when FF connected to DBC is removed and a delay FF is used instead of generation of *B* or *B'* signal.
10. For three-phase applications, suggest suitable changes in the hardware and software in the given microprocessor based trigger circuit.

4

Driver Circuits for Gate-commutation Devices*

4.1 INTRODUCTION

The devices from the transistor family differ from the devices of the thyristor family with respect to their input or drive characteristics. In case of a thyristor, once it is triggered, it continues to remain in the conduction mode unless a current passing through it reduces to zero (actually, below its holding current level). However, in case of transistors, to keep them in conduction state, a continuous base or gate signal is required. Basically, the transistors or other gate-commutation devices are either current controlled device (e.g. BJT) or voltage-controlled device (e.g. MOSFET, IGBT). Similarly for turn-on operation, GTO behaves as an SCR, while turn-off operation (or gate-current requirements for turn-off) is totally different from the SCR. A GTO requires a large negative-gate current and a high-power sink for successful commutation (similar to the driving requirements of a power BJT). As discussed earlier, normally the driver circuit has to provide electrically isolated gate/base signal. In case of a power BJT, current gain (h_{fe} or β) of the transistor is low (β = 5 to 10). Therefore, the power capability of the driver circuit should be as high as 20% of the power circuit. However, driving a power MOSFET is similar to driving a very high impedance capacitive network. Thus, a carefully designed very low-power driver circuit is required. Most of the gate-voltage controlled (or gate-commutation controlled) power semiconductor devices require very low power driver circuit. In general, unipolar drive signals (positive voltage) are sufficient for normal turn-on and turn-off of the devices. However, for rapid turn-on and turn-off, bipolar signals (both positive and negative voltage pulses), are required. Moreover, for high switching performance, similar circuits with high source and sink capabilities, are required for MOSFET, IGBT and BJT alike. In case of MOSFET/IGBT, the transition current

*Contributed by the author and published earlier: 'Gate drive circuits', in *Power Electronics Handbook*, Rashid, M.H. (Chief Editor), Ch. 18, Academic Press, California. Received permission from Elsevier/Academic Press, California, to republish it.

capability should be high (with low-output power). While in case of a BJT, sustained high base current is required. In case of a GTO, a very low power circuit is required for switching it on (turn-on). However, power of the turn-off circuit should be very high (compatible to power BJT drive circuit). Although it is required for a very short period but the gate power requirement of the negative pulse is about $\frac{1}{3}$rd of the power circuit. Contrary to all these devices, an MCT requires a very low-power driver circuit (±10 V, 200 nA).

4.2

GATE DRIVE CIRCUITS FOR POWER MOSFET

The input gate characteristics of a MOSFET differ from its bipolar counterparts. The gate is isolated electrically from the source by a layer of silicon dioxide. Ideally, no current flows into the gate when a dc voltage is applied. However, a small leakage current (of the order of 10^{-10}A), flows to maintain the gate voltage. During the transition periods (off-to-on and on-to-off), therefore, a small current is enough to charge and discharge the device capacitances. However, the device capacitances and the source impedance of gate-drive, limit the device switching speed.

4.2.1 Gate and Device Capacitances

There are three parasitic device capacitances (Fig. 4.1). They are non-linear and voltage dependent. Their values are high for very low magnitude of V_{DS} and become almost constant for higher or the rated values of V_{DS}.

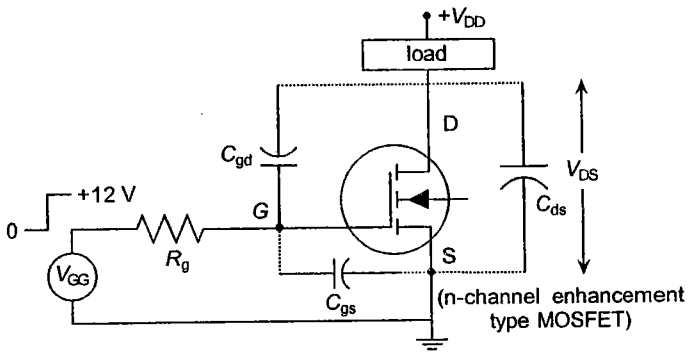


Figure 4.1 An n-channel enhancement type MOSFET with voltage dependent device capacitances.

To turn-off the device, let the gate voltage is reduced to zero, then V_{DS} attains the supply voltage magnitude (V_{DD}). Thus the potential at D swings from 0 to V_{DD} and C_{gd} gets charged (through a low gate-source impedance, R_g) up to V_{DD} (say 100 V), as shown in Fig. 4.2a. Now, if a gate-drive signal is applied (higher than the threshold value, V_T) the device will be turned on. Ideally, the voltage across D and S reduces to zero (neglecting small V_{DS}) and terminal D will swing to ground potential (which was earlier at V_{DD} = 100 V). The decreasing V_{DS} produces a feedback current ($i = C_{gd}\, dV_{DS}/dt$) to the gate circuit, through C_{gd}, as shown in Fig. 4.2b. This feedback mechanism is called

Miller effect. Due to the charging and discharging of C_{gs} and due to the large swing in gate-to-drain voltage, a gate-drive circuit is required with high source and sink capabilities. Although, C_{gs} is an important parameter but C_{gd} is more significant due to Miller effect.

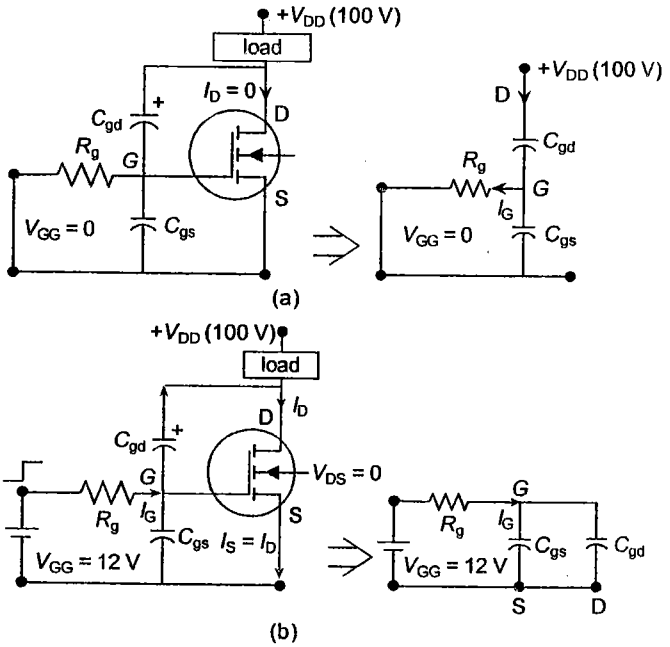


Figure 4.2 Large voltage swing of C_{gs} at D: (a) during turn-off and (b) during turn-on.

Both turn-on time and turn-off time are affected by R_g because R_g is in series with C_{gs} and C_{gd}. These periods can be independently controlled (Fig. 4.3). The turn-on time and turn-off time are reduced by the diode which allows the quick charge and discharge of the parasitic capacitors, by shorting R_g (as shown in Figs. 4.3a and 4.3b, respectively). However, a bipolar gate-drive signal enables rapid turn-on and turn-off.

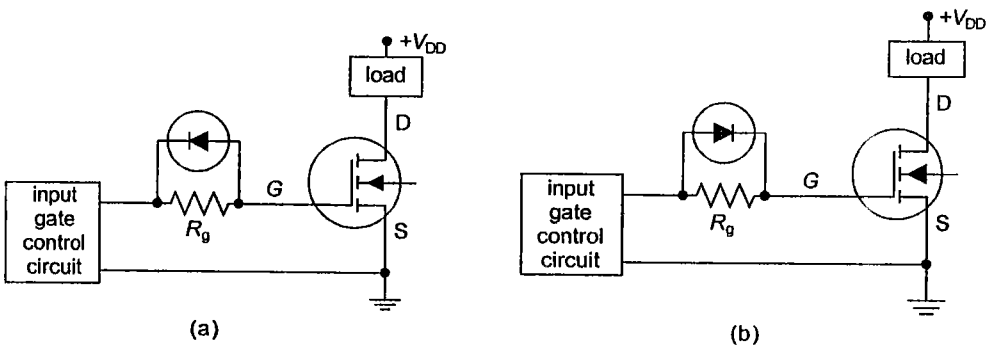


Figure 4.3 Driver circuits for (a) delayed turn-on and (b) delayed turn-off.

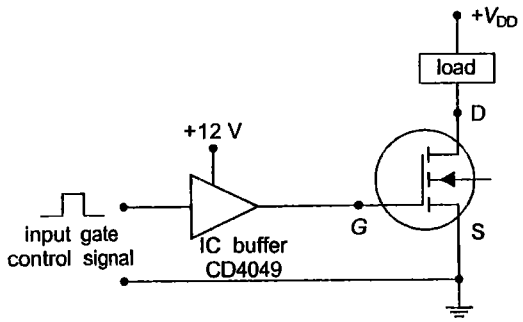
4.2.2 Different Driver Circuits

Low-power digital logic circuits (TTL or CMOS) can be easily used to directly drive the gate of a power MOSFET (Fig. 4.4). Since CMOS has limited source current and sink current capabilities (2 mA and 4 mA, @ V_{DD} = 12 V, respectively), a modest delay in the rise time and fall time is expected due to Miller effect (charging and discharging current requirements). However, CMOS IC can directly drive the gate with the required magnitude of the drive voltage. In case of a TTL device with a totem-pole output, the output voltage (high level) available is approximately 3.5 V (when V_{CC} = 5 V). This voltage (3.5 V) may be insufficient to drive the MOSFET into conduction mode. However the TTL IC has better source and sink capabilities than its counterpart CMOS. This speeds up the switching transition and reduces turn-on and turn-off time. The output voltage magnitude can be raised using an open-collector TTL with a pull-up resistor connected to a separate dc power supply (+10 to +15 V). It can guarantee rapid gate-turn-off due to large sink capability when output transistor of TTL (inside the TTL IC) is conducting at logic '0' level (Fig. 4.4). Moreover, this arrangement insures a sufficient gate voltage (+10 to +15 V) to turn the MOSFET fully on. However the turn-on is not as rapid as the turn-off because the pull-up resistor delays charging of the device capacitor, C_{gs}. Figure 4.4a shows a CMOS-based-driver circuit. Although the output voltage (+10 to +15 V) of CMOS logic is large enough to drive the MOSFET but to increase source and sink capabilities CMOS buffers (CD4049 or CD1450) are used. Thus, high performance is achieved with respect to switching speeds and low output impedance. To increase the switching speed further, more buffers can be connected in parallel to increase sink–current capability, for fast turn-off.

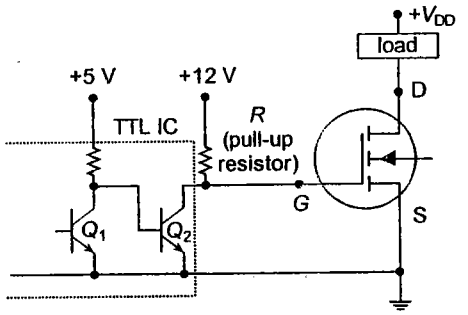
Figure 4.4b shows the connection of an open-collector TTL-based driver-circuit. The drawback of the TTL output voltage due to its lower magnitude (which is input gate control signal) has been removed. An additional dc power supply (+10 to +15 V) will be required, but this provides a rapid turn-off and ensures a sufficient gate voltage to turn the MOSFET fully on.

Figure 4.4c shows a configuration for fast turn-on with reduced power dissipation in TTL. When the TTL output is at logic '0' level, transistor Q_2 conducts. The output point (cathode of diode and base of Q_2) comes to about the ground potential, and Q_3 remains in off state. A very small power loss (few mW) takes place in R whose value is large and it behaves as the base resistance of Q_3. Similarly when the TTL output is at logic '0' level, Q_3 conducts due to high voltage at its base and diode becomes reverse biased. Thus a high voltage (approximately 12 V) reaches the gate of MOSFET. The conducting Q_3 provides low source impedance than R (as in previous case, Fig. 4.4b). Thus source capability increases, which enables a fast turn-on. The turn-off period depends upon the conduction of TTL output or pull-down transistor, Q_2 (by shunting the input gate capacitance of MOSFET to ground). Although sink and source capability of different types of TTL families varies, 74AC00 series (logic type) offers better performance for driving the MOSFET. The typical source current and sink current are 24 mA with a 7-ns propagation delay. Only Schottky (74S00 series) and low-Schottky (74LS00 series) offers less propagation delay (4 ns) but their source and sink current magnitudes are significantly low.

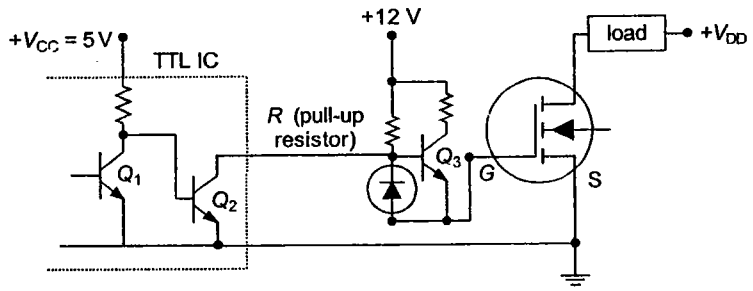
Figure 4.4d shows an open-collector TTL driving complementary emitter-follower (push–pull configuration). This circuit removes the drawback of the lower sink capability of the previous circuit (Fig. 4.4c). Thus very fast turn-off (hence high switching-speed) is attained using an outboard transistor (Q_4) to clamp the gate-to-ground. Both Q_3 and Q_4 are operating as emitter followers. As they are never driven into saturation and therefore their associated storage times do not significantly affect the switching frequency limit of the gate drive circuit.



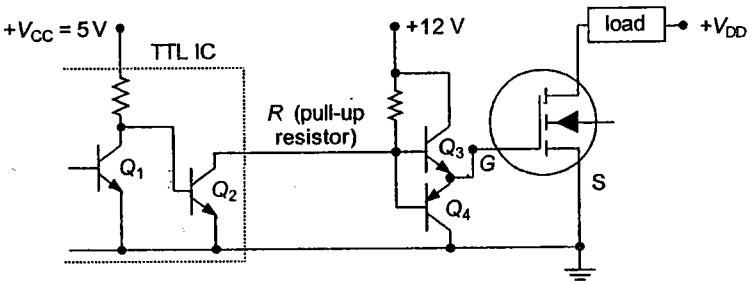
(a) A CMOS-based-driver circuit



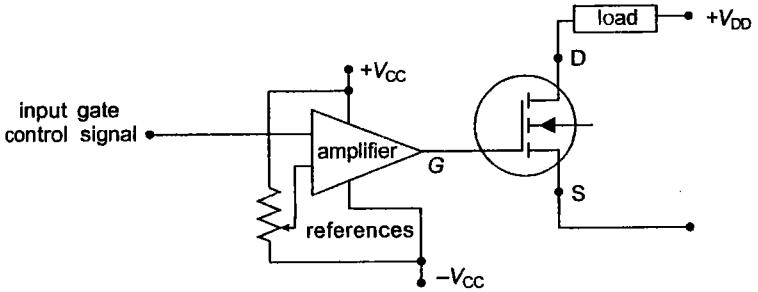
(b) Connection of an open-collector TTL-based-driver circuit



(c) A configuration for fast turn-on with reduced power dissipation in TTL

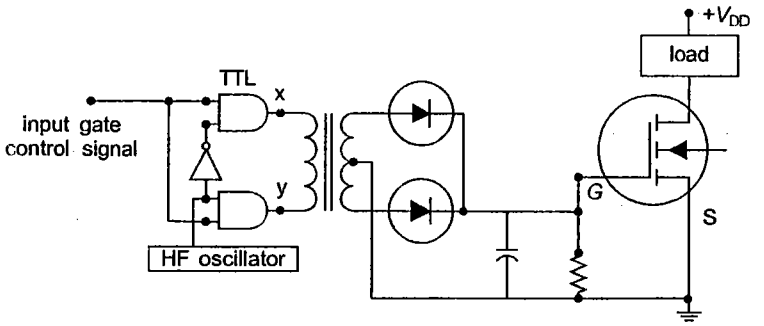


(d) An open-collector TTL driving complementary emitter-follower

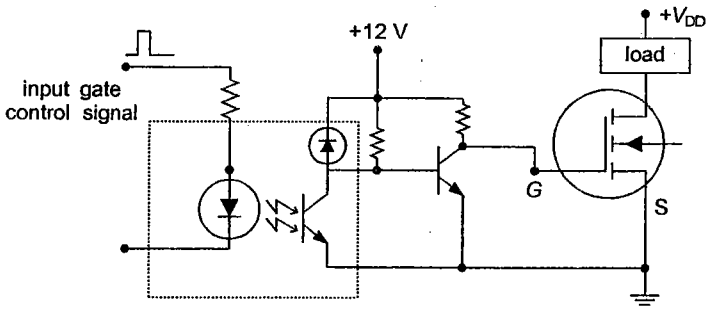


(e) A bipolar driver-circuit

Figure 4.4 (*Cont.*)



(f) An isolated gate driver circuit



(g) An opto-coupler based gate driver circuit

Figure 4.4 CMOS and TTL IC based driver circuits for MOSFET.

Figure 4.4e shows a bipolar-driver circuit, where during on and off periods, input drive signal varies between $+V_{CC}$ and $-V_{CC}$. This type of driver circuit is required for fast switching applications. In this case, the turn-on and turn-off times are small and the configuration is similar to a complementary emitter-follower circuit. Here source and sink capabilities are increased by providing low output impedance of the operational amplifier. Due to the negative voltage rail ($-V_{CC}$), the input gate capacitor of MOSFET quickly discharges hence turn-off time decreases.

Figure 4.4f shows a pulse transformer based driver circuit. The pulse transformer provides the isolation needed to drive different MOSFETs at different voltage levels (e.g. in a bridge configuration) or to control an n-channel MOSFET driving a grounded or source-follower load. The size of the transformer reduces significantly when the operating frequency becomes very high (100 kHz or more). Since current (hence power) requirement for the gate driver-circuit is very small at a steady-state condition (a few micro-Watts only), a separate driver circuit and additional (independent) dc power supply are not required. However, at the dynamic condition, i.e. during turn-on or turn-off transitions, a large current (high source and sink capability) is required for fast switching. Another limiting factor is the switching capability of the diode. Thus Schottky diode can be used whose turn-off time is very small (about 0.23 μ-sec). Here high-frequency carrier signal reaches the logic gates when the input drive control signal is high. The output voltage of logic gates become alternately high and low. Therefore, current flows in the primary winding of transformer from *x* to *y* and vice-versa. The voltage, generated in the secondary winding of transformer, is rectified and filtered. This dc voltage is ultimately used for driving a MOSFET. Recently, instead of the conventional pulse transformer, a miniaturized coreless (planar) transformer of about 1 cm^2 size,

fabricated on the surface of a printed circuit board (PCB), is used at 1 MHz for the same application. It is just like two-spiral winding arrangement (primary and secondary) on the plane of PCB. This arrangement is not very attractive due to the limitations of high-frequency switching and difficulty in fabrication of a dedicated PCB. Moreover, the size of conventional pulse-transformers is now significantly reduced which is compatible to the size of an IC chip. A surface-mount pulse-transformer with 5 mm height is available in the market (Picco Electronics, U.S.A.).

Figure 4.4g shows an opto-coupler based electrical isolation circuit. This circuit is similar to opto-coupler based driver circuit discussed for thyristors (Fig. 3.13d).

Figure 4.5 shows the connections of a clock driver (National DS0026, Motorola MMH0026 or Silicon General SG1626) based circuit. It is designed for high capacitive loads (high-sink and source capability). It has capability of ±1.5A output peak current (source and sink) with a typical 15-ns propagation delay. These drivers are compatible with series 54/74 TTL devices.

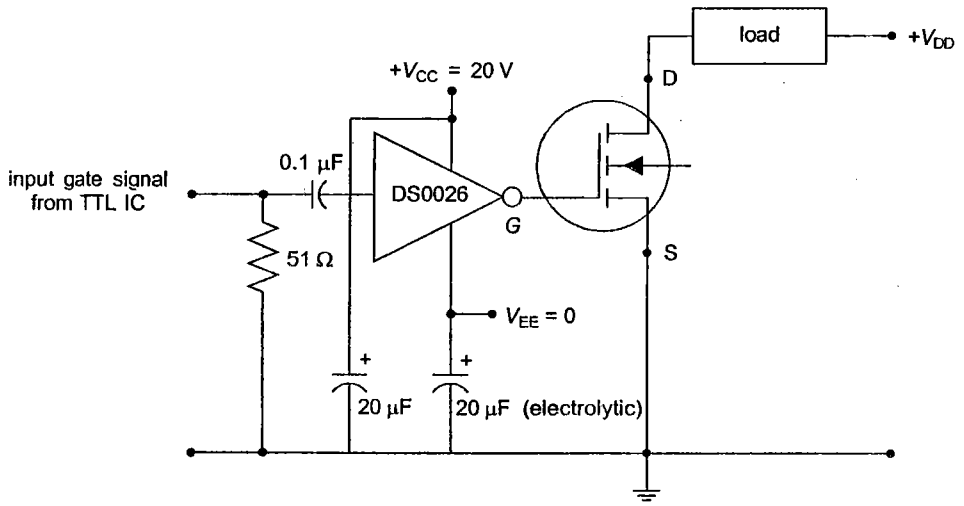


Figure 4.5 A clock driver based driver circuit for a MOSFET.

Moreover, custom-built integrated-driver circuits are also available for such applications (e.g. IRXX series). IC IR2110 and IR2111 are recommended for general applications. Similarly, for specific applications, IR2112, IR2130 and IR2132 are recommended for resonant-mode, six-step and PWM control, respectively.

4.2.3 Design Considerations of MOSFET-driver Circuits

Normally, manufacturers do not specify the device capacitances, rather they quote input, output and reverse common-source capacitances (C_{iss}, C_{oss} and C_{rss} respectively). All these capacitances are related according to the following relations:

$$C_{iss} = C_{gs} + C_{gd} \quad \text{(where } C_{ds} \text{ shorted)} \tag{4.1}$$

$$C_{oss} = C_{ds} + C_{gd} \quad \text{(where } C_{gs} \text{ shorted)} \tag{4.2}$$

$$C_{rss} = C_{gd} \tag{4.3}$$

The device switching speed largely depends upon C_{rss} (or C_{gd}) and the gate-drive source impedance. However, due to two considerations, the accurate estimation of the switching time (turn-on and turn-off) becomes difficult. First, the magnitude of C_{iss} varies with V_{DS}, particularly large variations are at low drain-voltage levels. The switching time-constant (RC) determined by C_{iss} and gate-drive impedance changes even during the switching cycle. The second consideration is due to the Miller effect. The switching transition can be divided into three distinct periods, as shown in Fig. 4.6.

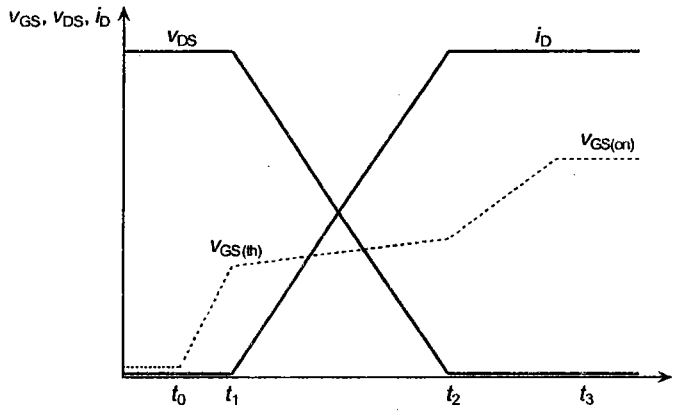


Figure 4.6 Ideal switching characteristics of MOSFET with resistive load.

The gate-drive requirements for these three periods may be expressed as follows:

$$\left.\begin{aligned} i_G &= \frac{C_{iss} v_{GS(Th)}}{t_1 - t_0} && \text{for } t_0 \le t \le t_1 \\ &= \frac{C_{rss}(v_{DD} - v_{DS(on)})}{t_2 - t_1} && \text{for } t_1 \le t \le t_2 \\ &= \frac{C_{iss}(v_{GS(on)} - v_{GS(Th)})}{t_3 - t_2} && \text{for } t_2 \le t \le t_3 \end{aligned}\right\} \quad (4.4)$$

The value of capacitances may be found from the manufacturers data book. For the first-two periods, C_{iss} and C_{rss} values may be assumed corresponding to $v_{DS} = \frac{1}{2} v_{DD}$. While for the third one, assume C_{iss} corresponding to $v_{DS} = v_{DS(on)}$. A small valued gate resistor of considerable power rating (5–20 W) is used in high-speed switching circuits. Because the stray inductance of the device assembly, connecting wire from driver circuit/chip (on printed circuit board to the gate of MOSFET) and the gate capacitances cause oscillation of input-gate current. It behaves as an under-damped series *RLC* circuit. If there is no gate resistance on the gate-driving circuit (ideally), then un-damped oscillation will cause a gate-voltage (v_{GS}) twice of v_{GG}. When the driver-chip or circuit operates at v_{GG} = 12 V, then v_{GS} would be 24 V. It could be destructive as maximum v_{GS} is normally 20 V.

The inter-connection from the gate driver to the MOSFET can be modelled with a lumped inductance of value,

$$L_p = \mu_0 \frac{ld}{w} \tag{4.5}$$

where $\mu_0 = 4\pi \times 10^{-7}$ H/metre $= 4\pi \times 10^{-9}$ H/cm, l is the trace length in (cm), w is the trace width (in cm) and d is distance from the trace to the ground plane (that should be under the trace).

Example 4.1 For a suitable value of gate resistor of a MOSFET, let l = 2 cm, w = 0.1 cm and d = 0.16 cm, then L_p = 40 ηH. The damping ratio is given by

$$\zeta = \frac{R}{2\sqrt{L_p/C_g}} \tag{4.6}$$

Let the total gate-input capacitance, C_g = 1nF. Then the resonance frequency of this circuit ($2\sqrt{L_p/C_g}$) is about 25 MHz. The fastest response of the circuit without overshoot will be for critical damping (ζ = 1.0), then

$$R = 2\sqrt{\frac{L_p}{C_g}} = 2\sqrt{\frac{40 \times 10^{-9}}{1 \times 10^{-9}}} = 12.6\ \Omega \tag{4.7}$$

A higher value gate-resistor may efficiently damp out the oscillations but at the same time, it slows down the switching-speed of the MOSFET. Because most of the driver chips run from a 12 V source and they supply or absorb about 1 A or more during the switching transitions. Therefore, 12 Ω is a suitable upper value for the gate resistance to damp out oscillation.

However, the response of the gate-drive circuit will be faster, when the circuit is an under-damped circuit. Therefore, if a small overshoot is allowed, say 10%, the corresponding value of ζ = 0.6 (which is found from the universal response curve of a second-order under-damped circuit). Therefore,

$$\zeta = 0.6 = \frac{R}{2\sqrt{L_p/C_g}} \tag{4.8}$$

or

$$R = 7.56\ \Omega$$

Therefore normally, a 10-Ω resistor is a suitable choice.

4.3 DRIVER CIRCUITS FOR IGBT

Basically, an IGBT is a MOSFET-driven power BJT. Thus, the driver circuits used for MOSFET are applicable for IGBT, too. It includes fabricated-driver circuits as well as custom-built-drive circuits, as discussed in the previous sections.

4.4

BASE-DRIVE CIRCUITS FOR POWER BJT

A properly designed base-drive circuit improves reliability by minimizing the switching time and hence switching losses and allows the device to operate in its most robust modes. Ideal base current and voltage waveforms are shown in Fig. 4.7. Initially a high current pulse should superimpose over the normal turn-on base current supplied from a current source. It brings the BJT rapidly into conduction. Thus reduces turn-on switching (transition) time and switching losses. Instead of simply ceasing the input drive base current, the turn-off switching (transition) time can be reduced by applying a negative (or reverse) base current. Normally, the base drive circuits are placed as near as possible to the device. For this purpose, additional base and emitter terminals are provided for the base-drive circuits. It reduces the length and inductance of the connecting wires, minimizes the effect of the noise/stray signals and clamps the oscillation in the base-drive signal.

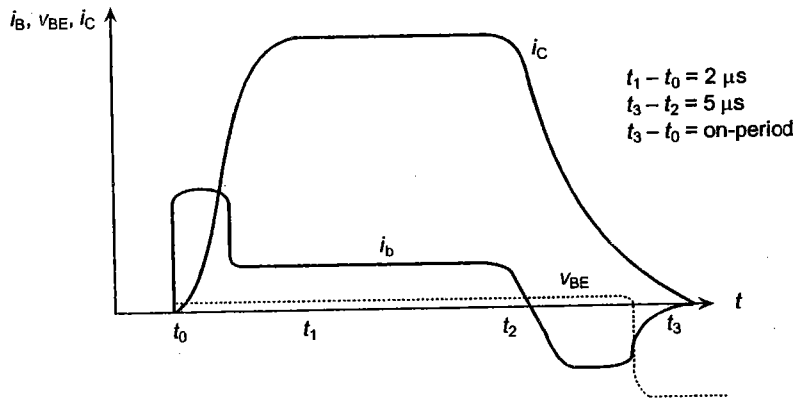


Figure 4.7 Ideal base current and voltage requirements of a power BJT.

Since a high current (and high-power) source is required for driving the base of a power BJT, difficulty arises when the emitter is not at ground potential (or at a fixed voltage level). When BJTs are connected in bridge configuration, or load is connected between emitter and ground, then the emitter terminal has a floating potential. Its potential changes from zero to supply voltage and from supply voltage to zero, when the BJT is switched off and switched on, respectively. Figure 4.8 shows a simple base drive circuits for a power BJT. Here a pnp transistor amplifies input-drive signal (Fig. 4.8a), and I_C ultimately drives the main power BJT. Basically, it is similar to a Darlington transistor circuit. Figure 4.8b shows a transistor totem-pole arrangement, which reduces power dissipation in the base drive circuit. Although this circuit operates even with unipolar dc power supply (with 0-volt rail instead of $-V_{CC}$), negative-voltage rail speeds up the turn-off transition (turn-off time reduces). Figure 4.8c shows a p-channel MOSFET-based-driver circuit. BJTs are drived by both unipolar as well as bipolar dc supply voltage. The emitter-to-base breakdown voltage rating (V_{EBO}) specifies the maximum negative-rail voltage. Normally, –8 to –6 V is used. Therefore, either a ±6 V, or +12 V and –6 V rails may be selected.

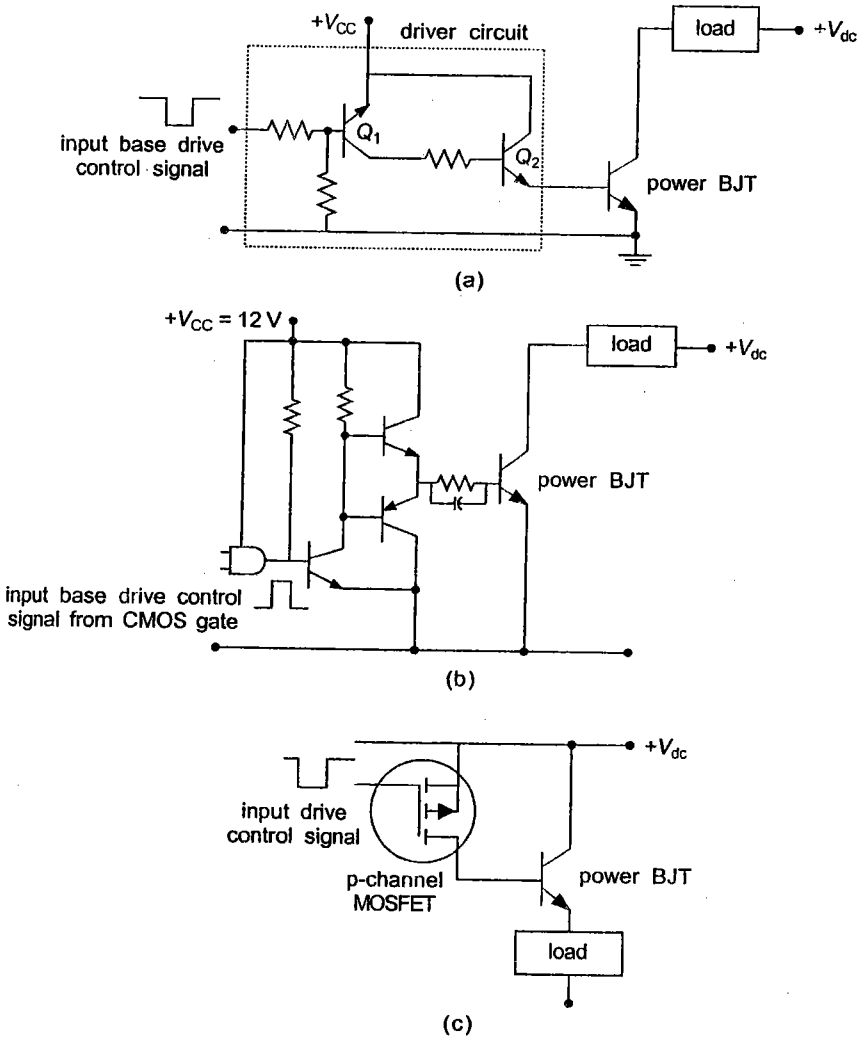


Figure 4.8 Base-drive circuits for power BJT.

4.5 GATE-DRIVE CIRCUITS FOR GTO

The gate-drive circuit for commutation of a GTO, as shown in Fig. 4.9, is similar to the transistor-drive circuits discussed in the previous section. The design procedure is same except that the anti-saturation circuit (e.g. BJT in push–pull mode) and base-to-emitter low impedance circuit are not necessary. The gate turn-off loop (circuit) should have minimum inductance (including L), to increase reverse gate di/dt and the shorter turn-off time. Therefore, the commutation circuit should be fabricated as close as possible to the gate terminal of GTO.

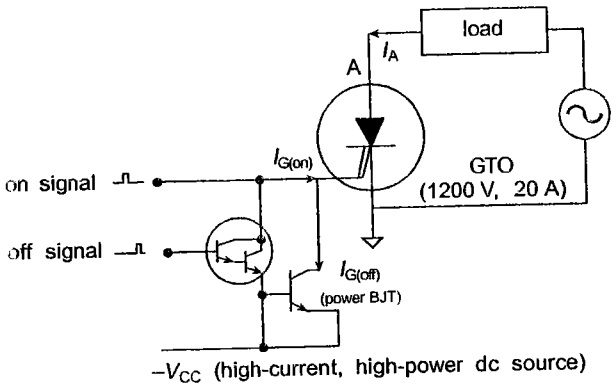


Figure 4.9 A gate-drive (commutation) circuit for GTO.

However, with a shorter turn-off time, the turn-off gain reduces (up to unity). Therefore, the reverse commutating gate-current must be almost of the same magnitude as the anode current. A high turn-off gain (over 20) can be achieved at the cost of turn-off switching losses with a slow reverse commutating gate-current (slow *di/dt*).

4.6 SOME PRACTICAL DRIVER CIRCUITS

The actual drive circuit highly depends upon the type as well as rating (power handling capability) of the power semiconductor devices. However, the basic circuit configuration does not change significantly.

Figure 4.10 shows a simple driver circuit for a power BJT. Figure 4.11 shows simple driver circuits for both MOSFET and IGBT. It works satisfactorily up to several kHz of switching

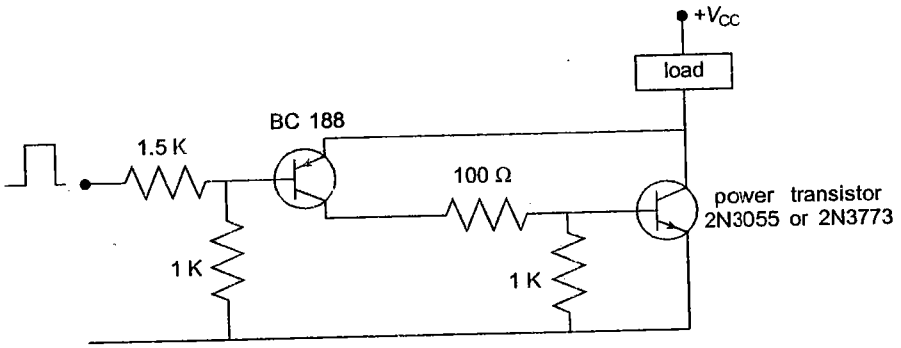


Figure 4.10 A simple driver circuit for a power BJT.

frequency. In this circuit, turn-off is faster than the turn-on, as the npn transistor (SL100) offers very-low-impedance path to discharge the gate capacitances quickly. Figure 4.12 shows another improved driver circuits for fast switching of MOSFET and IGBT. The complementary transistor pair (or similar e.g. BC 187 and BC 188) acts as source and sink for the gate of the device. Thus, both turn-on and turn-off are fast.

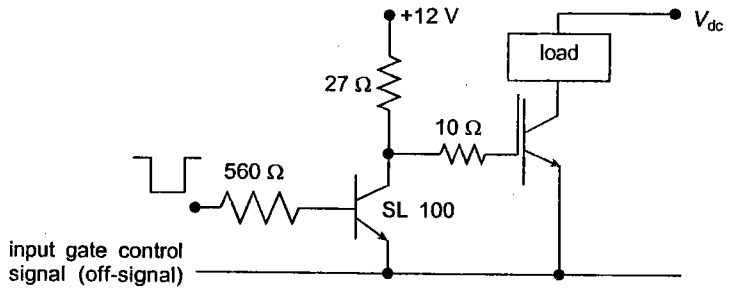


Figure 4.11 A simple driver circuits.

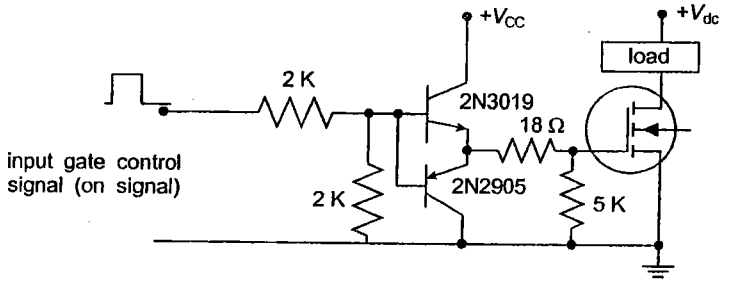


Figure 4.12 Some improved driver circuits.

Figure 4.13 shows an opto-coupler based driver circuit for GTO. Here a power BJT is used for high-current requirement during the commutation of the device.

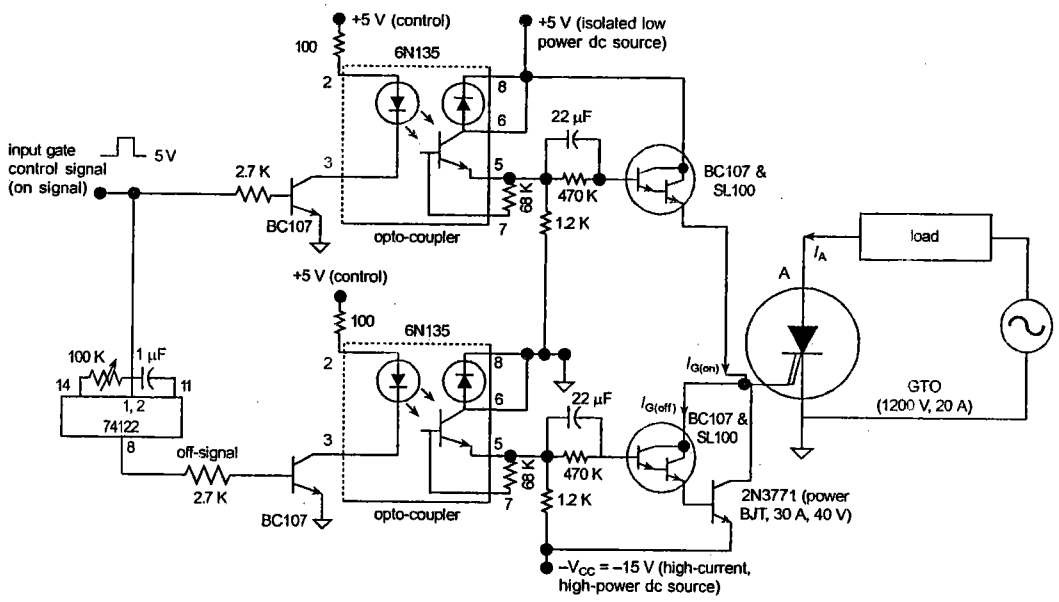
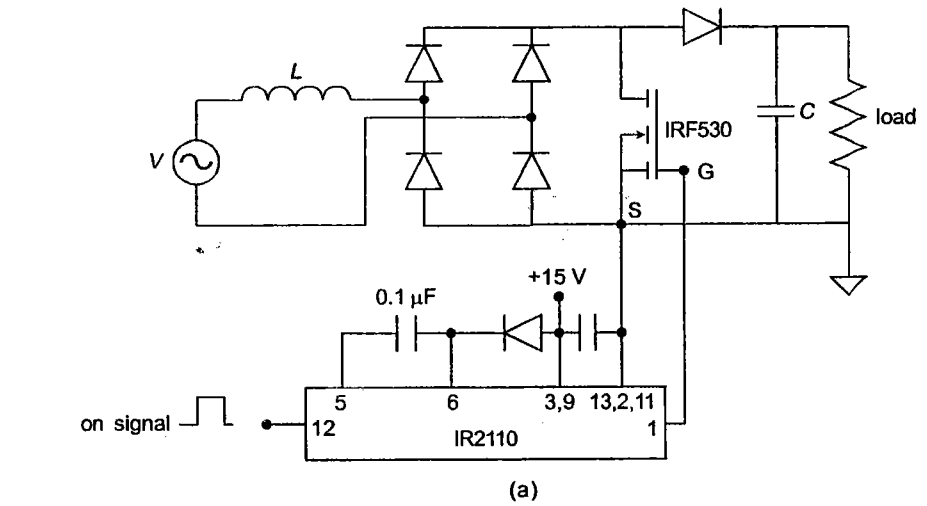


Figure 4.13 An opto-coupler based driver circuit for a GTO.

Figure 4.14a shows a custom-built driver circuit using IC chip IR2110 for driving a MOSFET in boost type switched-mode rectifier (SMR) circuit. In addition to the gate-resistance control circuit and ultra-violet ray sensor based short-circuit protection circuit (inside the chip), such custom-built driver circuits have high source and sink capability (2 A for IR2110). However, these driver circuits are not cheap and sometimes costlier than the power semiconductor device itself. Figure 4.14b shows another driver circuit for driving IGBT power module of a half-bridge inverter circuit. It has one floating (independent) gate drive signal output, which is used in a half-bridge configuration. For full-bridge applications, two or three IR2110, or one IR2130 (which has six gate-drive outputs) may be used.



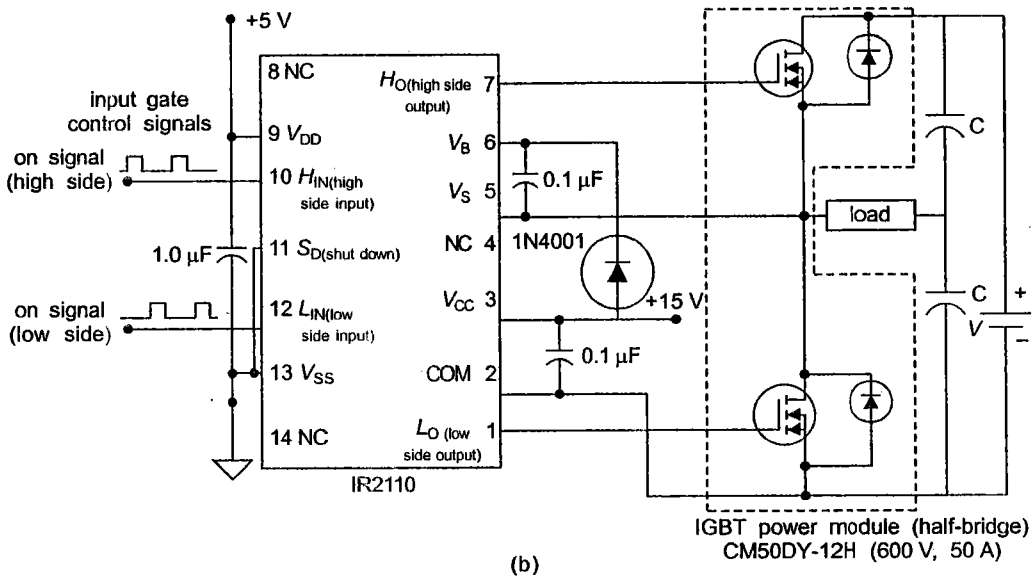


Figure 4.14 A driver IC for (a) MOSFET and (b) IGBT power module (half-bridge circuit).

SUMMARY

Gate-commutation devices require gate signals continuously to retain its conduction state. Unlike thyristors, during on-state of device, the power required is negligibly small, except in case of a power BJT. While, in case of MOSFET or IGBT, during the switching transition, the requirement of this current is high. Custom-built driver circuits are also available for such applications.

REVIEW QUESTIONS

1. In what respect gate driver circuits are different from thyristor trigger circuits?
2. What is Miller effect?
3. What are demerits of GTO driver circuits?
4. Why high source and sink capability is necessary for MOSFET/IGBT gate drive?
5. What are merits and demerits of a custom-built driver circuits?
6. Which parasitic device capacitance of MOSFET is important? Explain its role during turn-on and turn-off operation of the MOSFET.
7. Why cannot a normal digital IC (TTT or CMOS) drive MOSFET and IGBT?
8. What are main demerits of BJT with respect of its base drive circuits?
9. What are merits and demerits of opto-coupler based driver circuits?
10. What are demerits of GTO with respects to its gate driver circuits.

5

AC Voltage Regulators

5.1 INTRODUCTION

In general, ac voltage is controlled to obtain the desired performance of electrical systems. For this purpose, an ac voltage controller or regulator is used. The output voltage is either maintained constant, reduced or boosted. There are conventional as well as power electronic controllers for the same applications. These controllers have numerous applications, such as electrical heating, electrical welding, speed control of induction motors, output voltage stabilizers, etc. There are several conventional methods by which the output voltage can be controlled, such as variable resistors, variable inductors and autotransformers, as shown in Fig. 5.1. The variable resistor method, although simple, but in this case the efficiency is very poor. The variable inductor method requires a bulky and costly full-load current compatible variable inductor. Apart from the losses in these components, the rms value of output voltage (V_o) is highly load dependent. Therefore, in case of a fluctuating load, it is difficult to maintain the output voltage constant. Although the autotransformer method is one of the best methods, but it too suffers from the demerits due to its size, weight and cost. Earlier, this type of control scheme (autotransformer with tap changing arrangement) was used to control the dc voltage (hence speed) of series motors for electric traction of Indian Railways.

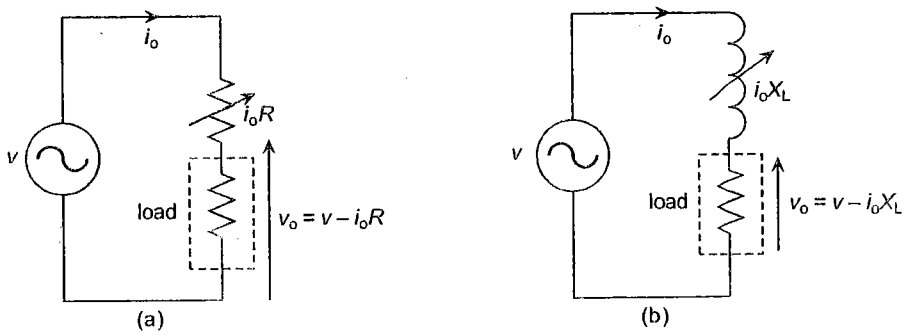


Figure 5.1 (*Cont.*)

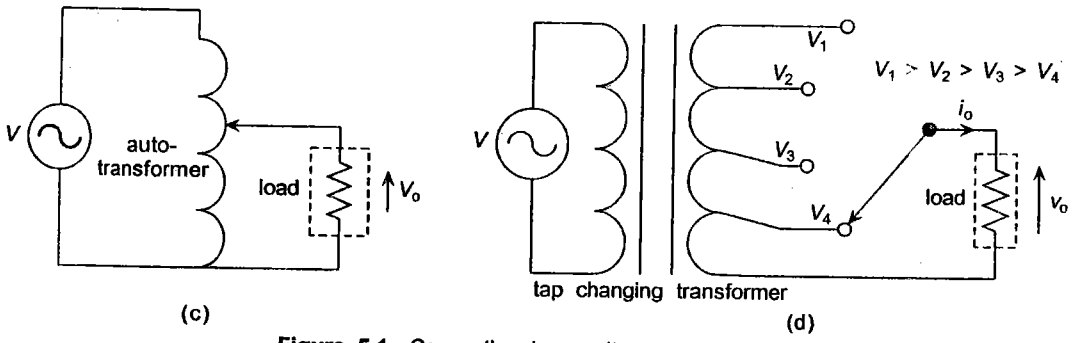


Figure 5.1 Conventional ac voltage controllers.

5.2 ON-OFF OR INTEGRAL-CYCLE CONTROL (ICC)

In this case, by closing and opening of a switch (S), the input voltage, v reaches the load for certain period of time (on-period). Similarly, for a certain period (off-period), the switch remains open. In general, for integral number of half-cycles (n), the switch S is closed and therefore the output (load) voltage is equal to the supply voltage ($V_o = V$). Similarly, for integral number of half-cycles (m), the switch (S) remains open and therefore the output voltage becomes zero ($V_o = 0$). That is why this method of voltage control is called *integral-cycle control* (ICC). To avoid fluctuations in the output voltage (V_o), the closing and opening operation should be fast. Since a mechanical switch cannot serve the purpose, power-semiconductor or thyristor based switches are used (Fig. 5.2). This type of control is used for temperature or other high time-constant type systems where on/off control does not cause fluctuations in performance of the system. The main demerits of ICC are that it introduces sub-harmonics in the line current, which are normally avoided. That is why this type of control is not very popular. For heating applications, zero-voltage switching (ZVS) is used, in addition to this technique. It is ensured that each thyristor is switched (gate current is supplied) at the zero-crossing instant (ZCI) of the input voltage wave only. Therefore, only sinusoidal current flows and that starts from ZCI only (for a resistive load). In this case large *di/dt* is avoided, which otherwise induces emf (*Ldi/dt*) in the neighbouring circuits (specially low-voltage circuits) and causes electro-magnetic interference (EMI) to the neighbouring communication lines.

Voltage waveforms of ICC circuits are shown in Fig. 5.2. The output voltage is, basically, an integral number of half-cycles. If the switch S is closed and opened for n and m number of cycles, respectively, the rms value of the output voltage is given by

$$V_o = \left[\frac{n}{\pi(n+m)} \int_0^{\pi} (\sqrt{2}V \sin \omega t)^2 \, d(\omega t)\right]^{1/2} \tag{5.1}$$

or

$$V_o = \left[\frac{n}{\pi(n+m)} \int_0^{\pi} (\sqrt{2}V \sin \omega t)^2 \, d(\omega t)\right]^{1/2} = V\sqrt{\frac{n}{n+m}} = V\sqrt{k} \tag{5.2}$$

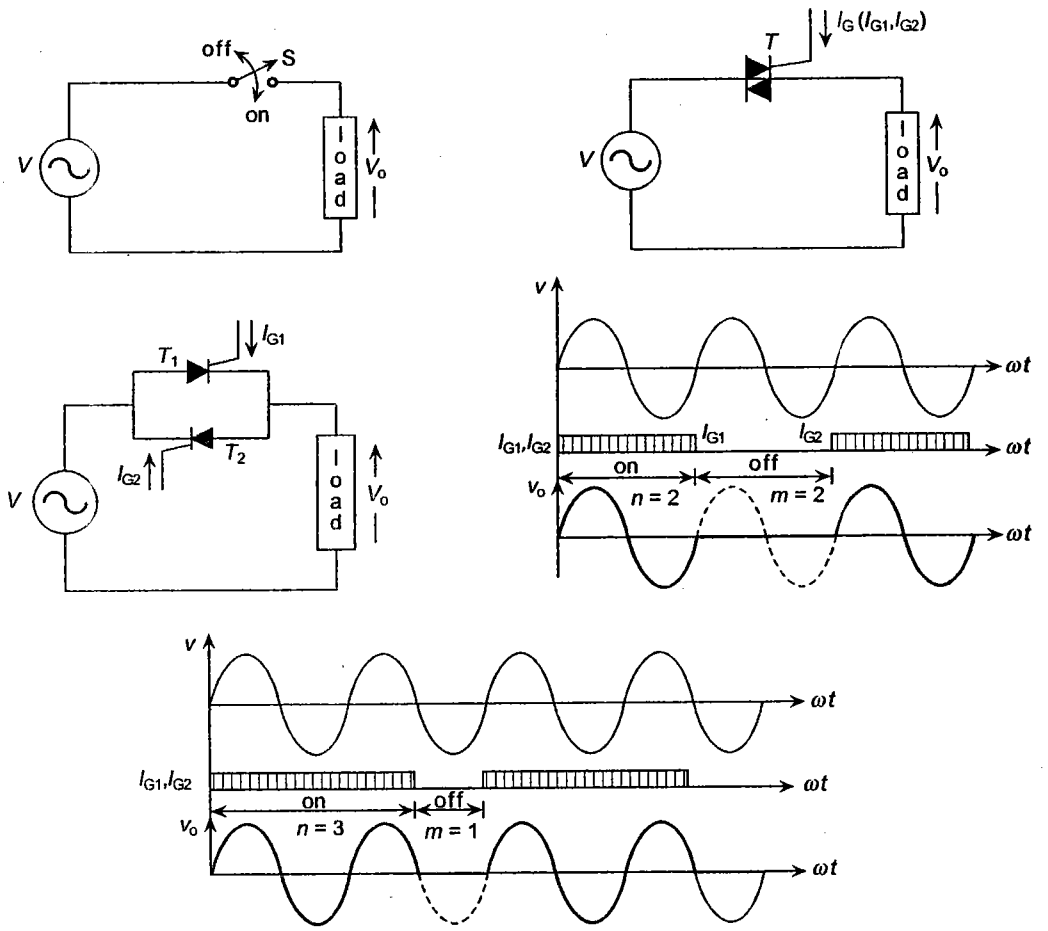


Figure 5.2 Output voltage control by ICC.

The output power for a resistive load,

$$P_o = \frac{V_o^2}{R} = \frac{n}{n+m}\frac{V^2}{R} \tag{5.3}$$

Therefore, the power factor,

$$\text{PF} = \frac{\text{Output power}}{\text{Input power}} = \frac{V_o(V_o/R)}{V(V_o/R)} = \frac{V_o}{V} = \sqrt{\frac{n}{n+m}} = \sqrt{k} \tag{5.4}$$

It is evident from equation (5.2) that the voltage can be controlled in steps only. Therefore, a smooth and fine voltage variation is not possible. For increasing resolution of steps, the total number of control-cycles ($n + m$) are to be increased. This causes large fluctuations in the output voltage, especially, in lower range due to longer off period (m). It is the main hurdle in adoption of on/off or ICC technique. If on and off periods (m and n) are reduced to overcome this demerit, it limits the controllability. For example, if m is fixed to a minimum, i.e. $m = 1$, the controlled

output voltage (V_o) will be 70.71, 81.65, 86.6, 89.44 and 91.29 per cent of V for $n = 1, 2, \ldots, 5$. In this case, there is no control between 0 and 70.71 per cent of V. Moreover, the input power for a resistive load varies between 50 and 100% (in steps only). Similarly, if n (on-period) is fixed to a minimum ($n = 1$), the value of V_o will be 70.71, 57.73, 50, 44.72 and 40.82 for $m = 1, 2, \ldots, 5$, respectively. When the off period becomes longer, it causes a large fluctuation in the output voltage. Moreover, ICC technique generates sub-synchronous harmonic current in the line. It may ultimately cause pulsation of the alternator shaft at that frequency (lower than 50 Hz or 60 Hz). Therefore, for large power applications, ICC is not acceptable.

Example 5.1 The resistance of a heating element of a 230-V, 5.3-kW resistance furnace is 10 Ω. Find:

(a) the duty ratio, for 50% input power using ICC
(b) the duty ratio, for 50% of the rated voltage using ICC, and
(c) the power factor at above condition.

Solution (a) We have

$$\text{Power input, } P = \frac{V_o^2}{R}$$

For ICC,

$$V_o = K^{1/2}V \quad \text{or} \quad P = \frac{KV^2}{R}$$

and

$$\text{Duty ratio, } K = \frac{PR}{V^2} = \frac{5.3 \times 10^3}{2} \frac{10}{(230)^2} = 0.5$$

If $(m + n)$ is selected as 2, then $n = 1$.

(b) For ICC, the output voltage,

$$V_o = K^{1/2}V \quad \text{or} \quad K = \left(\frac{V_o}{V}\right)^2 = (0.5)^2 = \frac{1}{4}$$

If $(m + n)$ is selected as 4, then $n = 1$.

(c) In case of ICC,

$$\text{PF} = \frac{V_o}{V} = K^{1/2} = \left(\frac{1}{4}\right)^{1/2} = 0.5$$

5.3 PRINCIPLE OF PHASE CONTROLLED SWITCHING

In case of ICC method, the output voltage is controllable by opening and closing the switch for one or several half-cycles of the ac input voltage. While in case of phase controlled switching, the output voltage is controllable by opening and closing the switch within a cycle (Fig. 5.3). The controller keeps the switch open (off) for a certain period within a supply voltage cycle (in general, less than half-cycle), and closes the switch (on) for the remaining period of the cycle. Thus the input supply

voltage (V) reaches the load within a fraction of each cycle and V_o becomes equal to V. When the switch is open, the input voltage does not reach the load and it becomes zero ($V_o = 0$). Thus instead of complete input voltage (whole ac cycle) reaching the load, the switch slices the input ac voltage and only its part (or parts) reaches the load. Thus in this case, as shown in Fig. 5.3, the switch is closed between α and β only. Therefore, instead of a sinusoidal voltage, a discontinuous sinusoidal voltage reaches the load. The magnitude of the output voltage depends upon the discontinuity of the supply voltage reaching the load. In the previous case (ICC), this discontinuity was in steps of the half-cycle and the fine output voltage control was not possible. In case of a phase control, the discontinuity of the supply voltage reaching the load is maintained within each cycle. Therefore, a fine output voltage control becomes possible. The rms value of the output voltage, V_o may vary from 0 to V—the rms value of the input or supply voltage.

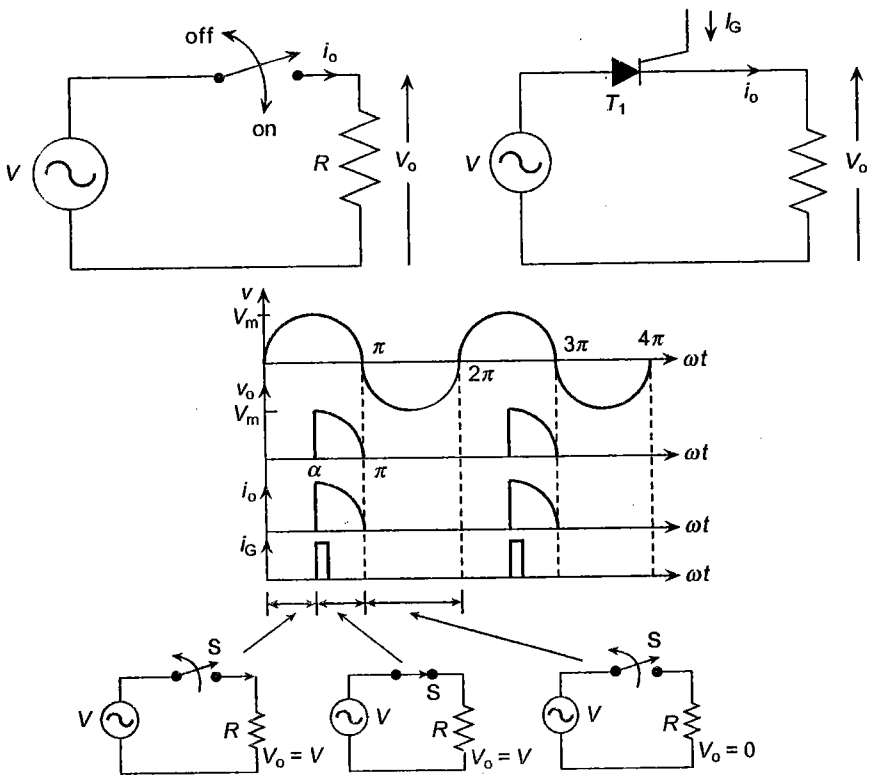


Figure 5.3 Output voltage control by phase-controlled switching.

In this arrangement, no transformer is necessary. The power semiconductor switching devices work as a switch. Thus, the size, weight and cost are small and the efficiency is very high. Sometimes, the efficiency of the controller is close to 99%.

Since fast switching and opening of the switch in each power cycle (50 or 60 Hz) is an essential requirement of such controllers, mechanical switches cannot serve the purpose. Thus power semiconductor based switches (SCR, triac, etc.) are used. Between $\omega t = 0$ and α, no gate current is supplied to the thyristor (T_1) or switching device. Therefore, SCR remain off and the

load voltage remains zero (as if a contactor switch is open). If a gate signal is applied at $\omega t = \alpha$, the SCR (T_1) conducts and the supply voltage, V reaches to the load (as if a contactor switch is closed). The load or the output voltage (V_o) becomes equal to the input or supply voltage. Since the output current varies according to the output voltage ($i_o = V_o/R$) and ideally at $\omega t = 180°$, the magnitude of the current reduces to zero. Then thyristor (SCR) ceases to conduct. This angle, where turn-off of the device takes place is called *commutation* angle, β (in this case, it is equal to 180°). In fact, commutation takes place slightly before $\omega t = 180°$, when the load current or current through the thyristor becomes equal to the holding current. Here, the turn-off of SCR is line commutation or natural commutation. Between α and β, the load voltage is same as the source voltage. Therefore, the rms value of output voltage is given by

$$V_o = \left[\frac{1}{2\pi}\int_0^{2\pi} (\sqrt{2}V \sin \omega t)^2 \, d(\omega t)\right]^{1/2}$$

$$= \left\{\frac{1}{2\pi}\left[\int_0^{\alpha} 0 + \int_{\alpha}^{\pi} (\sqrt{2}V \sin \omega t)^2 d(\omega t) + \int_{\pi}^{2\pi} 0\right]\right\}^{1/2}$$

$$= \left[\frac{V^2}{2\pi}\int_{\alpha}^{\pi} (1 - \cos 2\omega t)\, d(\omega t)\right]^{1/2}$$

$$= V\left\{\frac{1}{2\pi}\left[(\pi - a) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2} \qquad (5.5)$$

It is evident from equation (5.5), that the output voltage can be finely controlled by controlling α from 0° to 180°. In fact, α is controlled by delaying the gate signal. Therefore, α is called a *switching* or *delay* angle. Contrary to the conventional ac voltage controllers (Fig. 5.1), here V_o is no more sinusoidal rather it is a discontinuous voltage.

If a diode is also connected in reverse parallel with SCR, as shown in Fig. 5.4, the output voltage has unsymmetrical positive-half and negative-half cycles. It is a distorted sinusoidal wave and its magnitude is given by

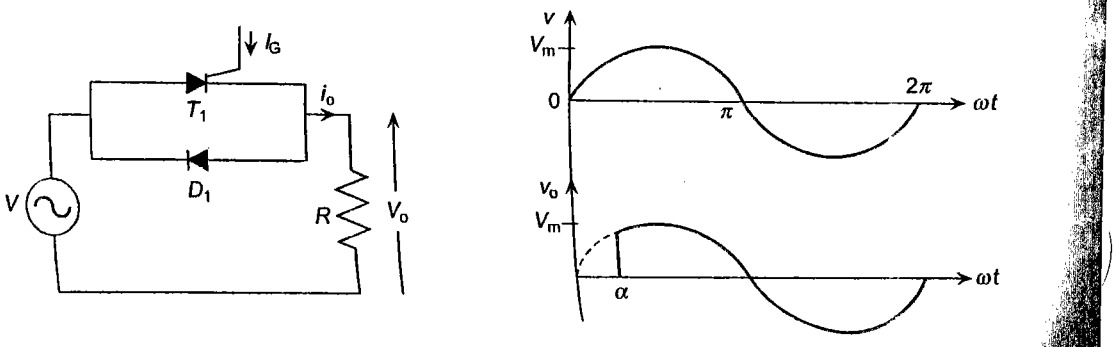


Figure 5.4 Asymmetric phase angle control.

$$V_o = \left[\frac{1}{2\pi}\int_{\alpha}^{2\pi}(\sqrt{2}V\sin\omega t)^2 d(\omega t)\right]^{1/2} = V\left\{\frac{1}{2\pi}\left[(2\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2} \quad (5.6)$$

From (5.4), the power factor of the resistive load is given by

$$\text{PF} = \frac{V_o}{V} = \left\{\frac{1}{2\pi}\left[(2\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2} \quad (5.7)$$

For a low-power load and for small voltage-variations, this circuit can be used. However, the presence of dc voltage (as the average value is not zero) introduces dc current in the line, which may cause saturation of the input or distribution transformer. Therefore, in general, this type of controller (with unidirectional control) is not used.

5.4

FULL WAVE WITH *R* LOAD

This is most common ac voltage regulator. Here either two thyristors (SCR), one triac, one SCR with a diode bridge or a bridge with two SCR and two diodes can be used as a switch. Different circuit configurations and the relevant waveforms are shown in Fig. 5.5. The principle of ac phase control is applied in both the half-cycles. The output voltage (hence the load and line current) become symmetric in both the half-cycles. The gate pulse (I_{G1}) turns on T_1 at α and its conduction continues till β, which is equal to π. Similarly, the gate signal (I_{G2}) turns on T_2 at $(\pi + \alpha)$, the conduction of T_2 continues up to 2π. Here natural or line commutation of T_1 and T_2 takes place at π and 2π, respectively. The rms value of the output voltage is given by

$$V_o = \left[\frac{1}{\pi}\int_{\alpha}^{\pi}(\sqrt{2}V\sin\omega t)^2 d(\omega t)\right]^{1/2}$$

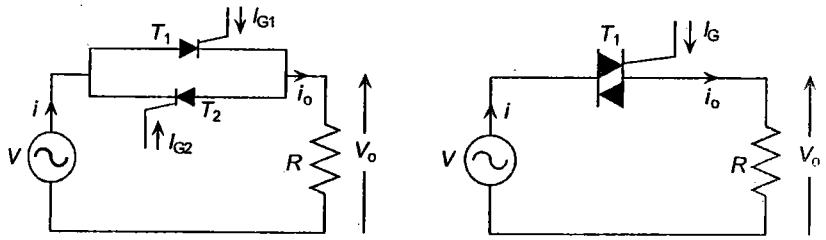
$$= \left[\frac{V^2}{\pi}\int_{\alpha}^{\pi}(1-\cos 2\omega t)\, d(\omega t)\right]^{1/2}$$

$$= V\left\{\frac{1}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2} \quad (5.8)$$

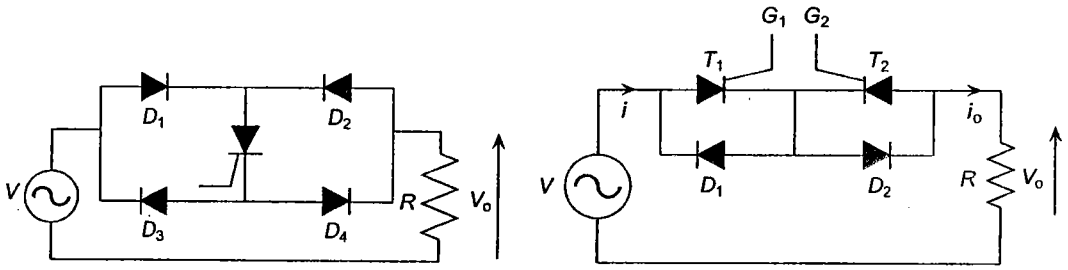
It is evident that the rms value of the output voltage can be finely controlled between 0 and V. From equation (5.4), the power factor of the ac voltage is given by

$$\text{PF} = \frac{V_o}{V} = \left\{\frac{1}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2} \quad (5.9)$$

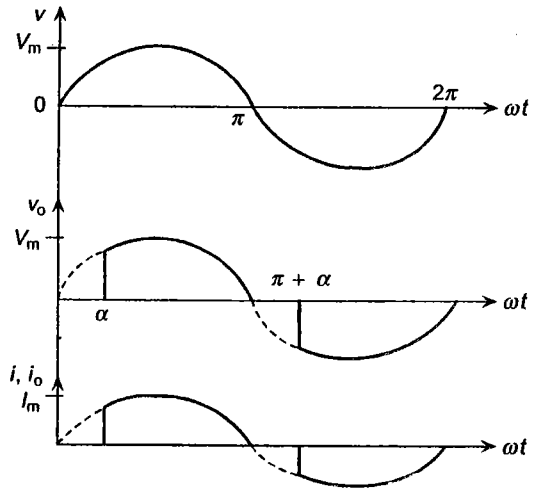
Example 5.2 Find the power factor of the resistance furnace of example 5.1 for the 50% input power, where the output voltage is controlled by the full-wave, phase-control switching technique.



(a) Symmetric, full-wave ac phase



(b) Full-wave, ac voltage regulator



(c) Waveform of full-wave, ac voltage regulator with R load

Figure 5.5 Different circuit configurations and the relevant waveforms.

Solution In case of ac phase control, for 50% input power, the output voltage is given by

$$P = \frac{V_o^2}{R} \quad \text{or} \quad V_o = (PR)^{1/2} = \left(\frac{5.3 \times 10^3}{2} \times 10\right)^{1/2} = 162.8 \text{ V}$$

Also,

$$\text{PF} = \frac{V_o}{V} = \frac{162.78}{230} = 0.707$$

In this case, PF is high, in comparison to ICC technique, for the same input power.

Example 5.3 A single-phase, 220-V, 1-kW electric room heater (radiator) is connected across 220-V supply through a triac. For a delay angle of 90°, calculate the power dissipated by the heater element.

Solution The output voltage of the ac regulator is given by

$$V_o = V\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)\right]^{1/2}$$

where the rms value of supply or input voltage, $V = 220$ V. For $\alpha = 90°$, V_o is given by

$$V_o = V\left[\frac{1}{\pi}\left(\pi - \frac{\pi}{2} + \frac{1}{2}\sin\frac{2\alpha}{2}\right)\right]^{1/2}$$

$$= V\left[\frac{1}{\pi}\left(\frac{\pi}{2} + 0\right)\right]^{1/2}$$

$$= 0.707V$$

If R is resistance of heater element (load) and the maximum power or rating of heater, $P = 1$ kW. Therefore,

$$R = \frac{V^2}{P} = \frac{(220)^2}{1 \times 10^3} = 48.4\ \Omega$$

The output power or power dissipated by the heater element at $\alpha = 90°$,

$$P_o = \frac{V_o^2}{R} = \frac{(0.707V)^2}{R} = \frac{(0.707 \times 220)^2}{48.4} = 499.85\ \text{W}$$

Example 5.4 For the above ac voltage controller, find the value of α, for the output voltage, 0.25 V.

Solution Since

$$V_o = V\left\{\frac{1}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2}$$

or

$$\frac{V}{4} = V\left\{\frac{1}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2}$$

or

$$\frac{\pi}{16} = (\pi - \alpha) + \frac{1}{2}\sin 2\alpha$$

or

$$\sin 2\alpha - 2\alpha + \frac{15\pi}{8} = 0$$

Let

$$f(\alpha) = \sin 2\alpha - 2\alpha + \frac{15\pi}{8}$$

Since α varies between 0 and 180°, by numerical technique using direct substitution method, the above equation can be solved. When $f(\alpha)$ becomes zero, it gives the value of α. From the voltage equation it is evident, at $\alpha = 90°$, $V_o = 0.707$ V. In this case as $V_o = 0.25$ V (which is less than 0.707 V), therefore α is higher than 90° and it lies between 90° and 180°. To find a suitable initial value for α, $f(\alpha)$ becomes zero or changes its sign, the true value of α lies there. It can be found manually as well as by using a dedicated computer program for a higher accuracy.

α	2α (rad)	sin 2α	$f(\alpha)$	Remarks
140°	4.8869	–0.984	0.0182	Positive
150°	5.235	–0.866	–0.2	Negative
145°	5.06	–0.9396	–0.111	Negative
142°	4.956	–0.970	–0.036	Negative
141°	4.921	–0.9783	–0.009	Negative (close to zero)

From the tabulated values, it is evident that sign changes between $\alpha = 140°$ and 141°. We can select $\alpha = 141°$, as in this case, $f(\alpha)$ is very small and almost zero. It can be verified by substituting the value of α in the voltage equation.

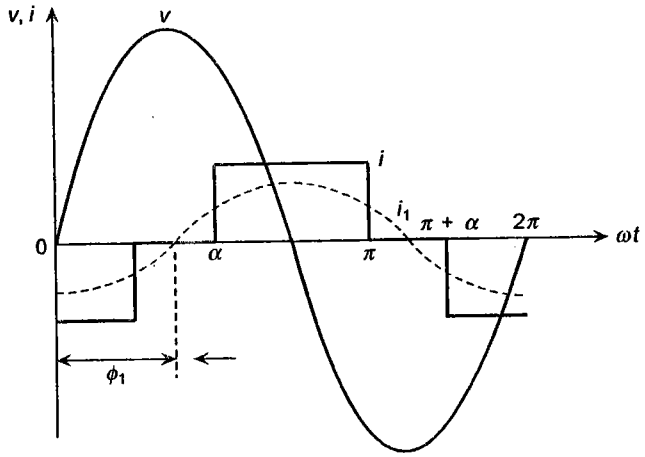
$$V_o = V\left\{\frac{1}{\pi}\left[\pi - \left(141° \times \frac{\pi}{180°}\right) + \frac{1}{2}\sin 282°\right]\right\}$$

$$= V\left[\frac{1}{\pi}(0.6806 - 0.485)\right]^{1/2}$$

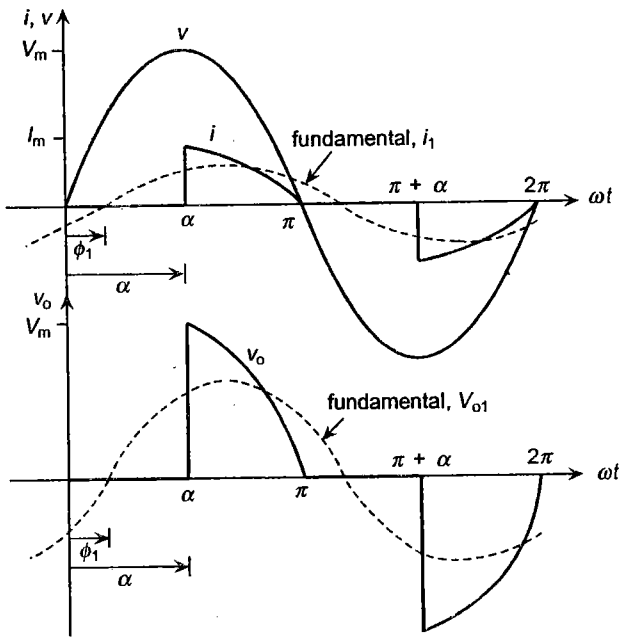
$$= 0.249V$$

5.5 HARMONIC ANALYSIS OF CONVERTERS

For sinusoidal voltage and current of same frequency, real power, apparent or reactive power and power factor can be easily found by using a standard relationship. However, in power electronic circuits, devices (diodes, thyristors, transistors, etc.) are on, in some portions of a cycle, and off, in other portions. Therefore, in general, the current and voltage waveform are periodic but non-sinusoidal, as shown in Fig. 5.6. Thus, the relationships for voltage, current, power and power factor for a purely sinusoidal waveform are no more valid. At steady-state, the waveform voltage and current may be continuous or discontinuous and it may contain high-frequency harmonics. Moreover, the power-factor angle is no more directly related simply with power input or with the phase angle between current and voltage waveforms, as shown in Fig. 5.6b for an ac regulator with R load. To compare different types of converters of the same class, to know the effect of converters on the utility system (e.g. power distribution line), to know the level of electromagnetic interference (EMI) they cause, harmonic analysis is important. In general, Fourier series expansions are used to find out the harmonic contents of the voltage and current. Due to non-sinusoidal waveforms, some more terms are needed which are defined now.



(a) Voltage and current waveforms for harmonic analysis



(b) Current and voltage waveforms of ac regulator for R load

Figure 5.6 Non-sinusoidal waveforms for harmonic analysis.

***Displacement power factor* (DPF)** It is also known as *fundamental power* factor. It is cosine of the angle ϕ_1, between supply voltage and fundamental component of the current waveform, i.e.

$$\text{DPF} = \cos \phi_1 \tag{5.10}$$

***Distortion factor* (DF)** It is a measure of distortion in the input current waveform in comparison to the normal purely sinusoidal waveform. It is a ratio of fundamental component of the current (I_1) to the total current input (I). Both are in rms values.

$$\text{DF} = \frac{I_1}{I} \tag{5.11}$$

***Input power factor* (IPF)** It is a ratio of the real or average power input to the rms value of the apparent power input. If V, I, V_1, I_1 and ϕ_1 are input supply voltage, input current, fundamental component of the input voltage, fundamental component of the input current and phase angle between V and I_1, respectively, then the input power factor is given by

$$\text{PF} = \frac{V_1 I_1 \cos\phi_1}{VI} = \frac{VI_1 \cos\phi_1}{VI} = \frac{I_1}{I}\cos\phi_1 = (\text{DF})(\text{DPF}) \tag{5.12}$$

Here, the input supply voltage is considered to be perfectly sinusoidal (only fundamental without harmonics), i.e. $V = V_1$. Also, it will be proved later that the average or real power input to the load only depends upon the fundamental component of the input current.

***Harmonic factor* (HF) *or total harmonic distortion* (THD)** This is a most important parameter to compare the performance of different converters. It gives idea about EMI caused by the converter. It is a ratio of rms values of all the harmonic terms (other than fundamental) to the fundamental component of current (I_1). Therefore, HF or THD with respect to the fundamental is given by

$$\text{THD}_\text{f} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \cdots}}{I_1} = \frac{\sqrt{I^2 - I_1^2}}{I_1} = \sqrt{\left(\frac{I}{I_1}\right)^2 - 1} \tag{5.13}$$

where I_2, I_3, I_4, ... are the harmonic components of the current and I is the rms value of the input current. Sometimes, THD is defined in terms of the rms value of the input current. Therefore, HF or THD of current is given by

$$\text{THD}_\text{r} = \frac{\sqrt{I^2 - I_1^2}}{I} = \sqrt{1 - \left(\frac{I_1}{I}\right)^2} \tag{5.14}$$

***Ripple factor* (RF)** For an ac-to-dc converter, it is desirable that the voltage and current ripple in output should be as minimum as possible to maintain average value nearly a constant. Therefore, the ripple factor is the ratio of rms values of all harmonic terms, to the average value of the current (I_{av}). Therefore,

$$\text{RF} = \frac{\sqrt{I^2 - I_1^2}}{I_{av}} \tag{5.15}$$

Note: Here HF or THD and RF are defined in terms of current only. However, these definitions are valid for the output voltage, too.

Power input For any sinusoidal or non-sinusoidal voltage and current input, power is given by

$$P_{av} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)\, i(\omega t)\, d(\omega t) \tag{5.16}$$

Substituting the expressions of voltage and current in general form

$$P_{av} = \frac{1}{2\pi}\int_0^{2\pi}\left\{\left[V_{dc} + \sum_{n=1}^{\infty}\sqrt{2}V_n \sin(n\omega t + \theta_n)\right]\left[I_{dc} + \sum_{n=1}^{\infty}\sqrt{2}I_n \sin(n\omega t + \phi_n)\right] d(\omega t)\right\}$$

$$= \frac{1}{2\pi}V_{dc}I_{dc}(2\pi - 0) + \frac{1}{2\pi}\int_0^{2\pi} V_{dc}\sum_{n=1}^{\infty}\sqrt{2}I_n \sin(n + \phi_n)\, d(\omega t)$$

$$+ \frac{1}{2\pi}\int_0^{2\pi} I_{dc}\sum_{n=1}^{\infty}\sqrt{2}V_n \sin(n\omega t + \theta_n)\, d(\omega t)$$

$$+ \frac{1}{2\pi}\int_0^{2\pi}\sum_{n=1}^{\infty} 2V_nI_n \sin(n\omega t + \theta_n)\sin(n\omega t + \phi_n)\, d(\omega t)$$

Since average value of a sinusoidal function over a cycle is zero, we get

$$P_{av} = V_{dc}I_{dc} + 0 + 0 + \frac{1}{2\pi}\int_0^{2\pi}\sum_{n=1}^{\infty}V_nI_n\left[\cos(\theta_n - \phi_n) - \cos(2n\omega t + \theta_n + \phi_n)\right] d(\omega t) \quad (5.17)$$

$$= V_{dc}I_{dc} + \frac{1}{2\pi}\sum_{n=1}^{\infty}V_nI_n \cos(\theta_n - \phi_n)\, 2\pi + 0$$

$$= V_{dc}I_{dc} + V_nI_n \cos\psi_n, \qquad \text{where } \psi_n = \theta_n - \phi_n$$

Then

$$P_{av} = V_{dc}I_{dc} + V_1I_1 \cos\psi_1 + V_2I_2 \cos\psi_2 + \cdots + V_nI_n \cos\psi_n \quad (5.18)$$

This is a power equation in most general form. It is evident that the voltage and current of the same frequency contribute average (real or active) power.

Example 5.5 Find the contribution of the fundamental component of the current for the useful power.

Solution Any periodic current waveform can be represented by a series of sinusoidal and a dc waveform. For derivation of power factor of a non-sinusoidal input current, let the input voltage is perfectly sinusoidal (zero distortion) and it does not get affected by the switching (on and off of the power semiconductor devices). The input supply voltage is given by

$$v(\omega t) = V_m \sin\omega t = \sqrt{2}\, V \sin\omega t$$

For an alternating current, dc term is absent. Therefore,

$$i(\omega t) = \sqrt{2}\, I_1 \sin(\omega t + \phi_1) + \sum_{n\neq 1}^{\infty}\sqrt{2}\, I_n \sin(n\omega t + \phi_n)$$

The average power input is given by

$$P_{av} = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\, v(\omega t)\, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{2\pi} \sqrt{2}\, I_1 \sin(\omega t + \phi_1)\sqrt{2}V \sin \omega t\, d(\omega t)$$

$$+ \sum_{n\neq 1} \frac{1}{2\pi}\int_0^{2\pi} \sqrt{2}\, I_n \sin(n\omega t + \phi_n)\sqrt{2}\, V \sin \omega t\, d(\omega t)$$

$$= \frac{VI_1}{2\pi}\int_0^{2\pi} [\cos\phi_1 - \cos(2\omega t + \phi_1)]\, d(\omega t)$$

$$+ \sum_{n\neq 1} \frac{VI_n}{2\pi}\int_0^{2\pi} \{\cos[(n-1)\omega t + \phi_n] - \cos[(n+1)\omega t + \phi_n]\}\, d(\omega t)$$

Because

$$\sin A \sin B = \frac{1}{2}[\cos(A - B) - \cos(A + B)]$$

Then

$$P_{av} = \frac{VI_1}{2\pi}\left\{\left[\cos\phi_1(\omega t)\right]_0^{2\pi} - \left[\frac{1}{2}\sin(2\omega t + \phi_1)\right]_0^{2\pi}\right\}$$

$$+ \sum_{n\neq 1} \frac{VI_n}{2\pi}\left\{\left(\frac{1}{n-1}\sin\left[(n-1)\omega t + \phi_n\right]\right)_0^{2\pi} - \left(\frac{1}{n+1}\sin\left[(n+1)\omega t + \phi_n\right]\right)_0^{2\pi}\right\}$$

$$= \frac{VI_1}{2\pi}\left[\cos\phi_1(2\pi) - \frac{1}{2}(\sin\phi_1 - \sin\phi_1)\right]$$

$$+ \sum_{n\neq 1} \frac{VI_n}{2\pi}\left[\frac{1}{n-1}(\sin\phi_n - \sin\phi_n) - \frac{1}{n+1}(\sin\phi_n - \sin\phi_n)\right]$$

Because

$$\sin(2\pi + \phi_n) = \sin\phi_n$$

Then

$$P_{av} = \frac{VI_1}{2\pi}\left[\cos\phi_1(2\pi) + 0\right] + \sum_{n\neq 1} \frac{VI_n}{2\pi}(0 - 0) = VI_1 \cos\phi_1$$

Therefore, the sinusoidal input voltage, the fundamental component of the (load) current and their phase difference contribute useful power.

Fourier series expansion In general, any periodic signal or current waveform, $i(\omega t)$ can be represented by a series of sinusoidal terms and a dc term. Therefore,

$$i(\omega t) = I_{dc} + \sum_{n=1,2,\ldots}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)$$

$$= I_{dc} + \sum_{n=1}^{\infty} \sqrt{2}\, I_n \sin(n\omega t + \phi_n) \tag{5.19}$$

$$= I_{dc} + I_1 \sin(\omega t + \phi_1) + \sum_{n\neq 1}^{\infty} I_n \sin(n\omega t + \phi_n) \tag{5.20}$$

where $\phi_n = \tan^{-1}(a_n/b_n)$ and the rms value of fundamental and harmonic terms are given by

$$I_n = \sqrt{\frac{a_n^2 + b_n^2}{2}} \tag{5.21}$$

and

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i(\omega t)\, d(\omega t)$$

Also

$$a_n = \frac{1}{\pi} \int_0^{2\pi} i(\omega t) \cos(n\omega t)\, d(\omega t)$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} i(\omega t) \sin(n\omega t)\, d(\omega t) \tag{5.22}$$

Although for general type of converters, standard equations are available which can be used for the determination of the performance of the converters. However, these equations are valid for ideal conditions only, i.e. they are based on the assumption that either load is purely resistive or RL load is highly inductive. Therefore, the line current is assumed to be either sinusoidal or constant during the conduction period, respectively. Actual current or voltage should be considered for an accurate analysis.

Procedure for Calculation using Computer Program

Let a periodic waveform is expressed in Fourier series, as given:

$$y(\omega t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \tag{5.23}$$

$$= y_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \tag{5.24}$$

where a_0 is twice mean value (average or dc component) of function $y(\omega t)$.

The average or mean value is given by

$$y_0 = \frac{a_0}{2} = \frac{1}{2\pi} \int_0^{2\pi} y(\omega t)\, d(\omega t) \tag{5.25}$$

Similarly, a_n is twice the mean value of the product of $y(\omega t)\cos(n\omega t)$, i.e.

$$a_n = \frac{1}{\pi}\int_0^{2\pi} y(\omega t)\cos(n\omega t)\,d(\omega t) \tag{5.26}$$

and b_n is twice the mean value of the product of $y(\omega t)\sin(n\omega t)$, i.e.

$$b_n = \frac{1}{\pi}\int_0^{2\pi} y(\omega t)\sin(n\omega t)\,d(\omega t) \tag{5.27}$$

Now, $y_0, a_1, a_2, \ldots, a_n$ and $b_1, b_2, \ldots, b_n$ can be found by step-by-step numerical integration or integration using standard computational packages, e.g. MATLAB, MATHCAD, etc. For this purpose, let $y(\omega t)$ is sampled at m equidistant intervals in a cycle. Therefore, each sampling step is $2\pi/m$. Now, the value of $y(\omega t)$ at each step is given by $y_1, y_2, \ldots, y_m$. Therefore,

$$\left.\begin{aligned} a_0 &= \frac{2}{m}\sum_{m=1}^{m} y_m = \frac{1}{m}(y_1 + y_2 + \cdots + y_m) \\ a_n &= \frac{2}{m}\sum_{m=1}^{m} (y_m \cos n\omega t) = \frac{2}{m}(y_1 \cos n\omega t + y_2 \cos n\omega t + \cdots + y_m \cos n\omega t) \\ b_n &= \frac{2}{m}\sum_{m=1}^{m} (y_m \sin n\omega t) = \frac{2}{m}(y_1 \sin n\omega t + y_2 \sin n\omega t + \cdots + y_m \sin n\omega t) \end{aligned}\right\} \tag{5.28}$$

where

$$a_1 = \frac{2}{m}(y_1 \cos \omega t + y_2 \cos \omega t + \cdots + y_n \cos \omega t)$$

$$b_1 = \frac{2}{m}(y_1 \sin \omega t + y_2 \sin \omega t + \cdots + y_m \sin \omega t)$$

and

$$a_2 = \frac{2}{m}(y_1 \cos 2\omega t + y_2 \cos 2\omega t + \cdots + y_m \cos 2\omega t)$$

$$b_2 = \frac{2}{m}(y_1 \sin 2\omega t + y_2 \sin 2\omega t + \cdots + y_m \sin 2\omega t)$$

The rms value of each harmonic term can be found as

$$Y_n = \sqrt{\frac{a_n^2 + b_n^2}{2}} \quad \text{and} \quad \phi_n = \tan^{-1}\frac{a_n}{b_n} \tag{5.29}$$

Sometimes the rms value of function $y(\omega t)$ is also required, which is given by

$$Y_{\text{rms}} = \left[\frac{1}{2\pi}\int_0^{2\pi} y^2(\omega t)\,d(\omega t)\right]^{1/2} = \left(\frac{1}{m}\sum_{m=1}^{m} y_m^2\right)^{1/2} = \left[\frac{1}{m}(y_1^2 + y_2^2 + \cdots + y_m^2)\right]^{1/2} \tag{5.30}$$

In this chapter, several programs are given in BASIC to calculate THD, PF, harmonics and to plot harmonics for various types of converters. The nature of load current of a converter depends upon

the magnitude and the angle of impedance, the switching instant, etc. For example, it will be seen later in section 5.7 for an ac regulator with an RL-load, the line current is non-sinusoidal and discontinuous for $\alpha > \phi$. For $\alpha = \phi$, the current is just continuous and purely sinusoidal.

5.6

ANALYSIS OF AC VOLTAGE REGULATORS WITH *R* LOAD

The output voltage can be represented by the following Fourier series:

$$v_0 = \frac{a_0}{2} + \sum_{n}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)$$

where

$$\left.\begin{aligned} a_0 &= \frac{1}{\pi}\int_0^{2\pi} v_0(\omega t)\, d(\omega t) \\ a_n &= \frac{1}{\pi}\int_0^{2\pi} v_0(\omega t)(\cos n\omega t)\, d(\omega t) \\ b_n &= \frac{1}{\pi}\int_0^{2\pi} v_0(\omega t)(\sin n\omega t)\, d(\omega t) \end{aligned}\right\} \quad (5.31)$$

and $(a_0/2)$ is the average value of the function v_o, a_n and b_n are coefficients of sine and cosine functions, respectively. Since for resistive load, the output voltage is equal to the supply voltage between α to π and $\pi + \alpha$ to 2π (Fig. 5.6b), we have

$$a_0 = \frac{1}{\pi}\left[\int_{\alpha}^{\pi} (\sqrt{2}\, V \sin \omega t)^2\, d(\omega t) + \int_{\pi+\alpha}^{2\pi} (\sqrt{2}\, V \sin \omega t)^2\, d(\omega t)\right] = 0 \quad (5.32)$$

(because of half-wave symmetry)
and

$$\begin{aligned} a_n &= \frac{1}{\pi}\left[\int_0^{2\pi} \sqrt{2}\, V \sin \omega t \cos n\omega t\, d(\omega t)\right] \\ &= \frac{1}{\pi}\left[\int_{\alpha}^{\pi} \sqrt{2}\, V \sin \omega t\, (\cos n\omega t)\, d(\omega t) + \int_{\pi+\alpha}^{2\pi} \sqrt{2}\, V \sin \omega t\, (\cos n\omega t)\, d(\omega t)\right] \\ &= \frac{\sqrt{2}\, V}{\pi}\left[\frac{\cos(n+1)\alpha - 1}{n+1} - \frac{\cos(n-1)\alpha - 1}{n-1}\right], \quad \text{for } n = 3, 5, 7, \ldots, \text{ and } n \neq 1 \\ &= 0 \qquad\qquad \text{for } n = 2, 4, 6, \ldots \end{aligned} \quad (5.33)$$

$$b_n = \frac{1}{\pi}\left[\int_0^{2\pi} \sqrt{2}V \sin \omega t \sin (n\omega t)\, d(\omega t)\right]$$

$$= \frac{1}{\pi}\left[\int_\alpha^{\pi} \sqrt{2}V \sin \omega t \sin (n\omega t)\, d(\omega t) + \int_{\pi+\alpha}^{2\pi} \sqrt{2}V \sin \omega t \sin (n\omega t)\, d(\omega t)\right]$$

$$\left.\begin{aligned} &= \frac{\sqrt{2}V}{\pi}\left[\frac{\sin (n+1)\alpha}{n+1} - \frac{\sin (n-1)\alpha}{n-1}\right], && n = 3, 5, 7, \ldots, n \neq 1 \\ &= 0, && n = 2, 4, 8, \ldots \end{aligned}\right\} \quad (5.34)$$

It is important to note that there is a half-wave symmetry, i.e. the negative half-wave of the function is same as the positive half-wave (except the polarity). In other words, the variation in the positive half-wave is same as the variation in the negative half-wave (except the polarity). That is

$$\left[v_o(\pi + \omega t)\right]_\pi^{2\pi} = \left[-v_o(\omega t)\right]_0^{\pi} \quad (5.35)$$

In this case, only the odd harmonics are present and even harmonics become zero.
The rms value and phase difference of the nth harmonic of V_o is given by

$$V_{on} = \sqrt{\frac{a_n^2 + b_n^2}{2}}, \quad \phi_n = \tan^{-1}\frac{a_n}{b_n} \quad (5.36)$$

and

$$v_o(\omega t) = \sum_{n=1,3,5,\ldots}^{\infty} \left[\sqrt{2}V_{on} \sin (n\omega t + \phi n)\right] \quad (5.37)$$

The values of a_1 and b_1 can be found directly from the original equations of a_n and b_n (in the integral form), which are given by

$$a_1 = \frac{\sqrt{2}V}{\pi}\frac{\cos 2\alpha - 1}{2} \quad (5.38)$$

$$b_1 = \frac{\sqrt{2}V}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right] \quad (5.39)$$

Therefore,

$$V_{o1} = \sqrt{\frac{a_1^2 + b_1^2}{2}} = \frac{V}{\pi}\left\{\left(\frac{\cos 2\alpha - 1}{2}\right)^2 + \left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]^2\right\}^{1/2} \quad (5.40)$$

and

$$\phi_1 = \tan^{-1}\frac{\cos 2\alpha - 1}{2(\pi - \alpha) + \sin 2\alpha} \quad (5.41)$$

Similarly, the rms value of each harmonics can be found. For most of the cases, it is only the fundamental component which is important and which gives useful power. Therefore, higher order harmonics are undesirable. It is always desired to have a converter with lower higher-order harmonics or low HF or THD. Otherwise, higher THD causes more electromagnetic interference (EMI) to the neighbouring telecommunication or control/signal system lines. THD of the ac voltage regulator with a resistive load is given by

$$\text{THD} = \sqrt{\frac{V_o^2 - V_{o1}^2}{V_{o1}^2}} = \sqrt{\left(\frac{V_o}{V_{o1}}\right)^2 - 1} \tag{5.42}$$

Figure 5.7 shows a comprehensive graph for the fundamental and harmonics of the output voltages and the power factor of the ac voltage regulator with respect to the variation of the switching angle (α). Since nature of the current waveform is same as the output voltage waveform, i.e. $i_o = v_o/R$, it is simply their magnitude that varies. The individual current harmonics and THD are same as that of the voltage. Moreover, the input current (i) and the output current (i_o) are same. Program 5.1 in QBASIC gives calculation of different parameters for the performance evaluation of an ac regulator with a resistive load.

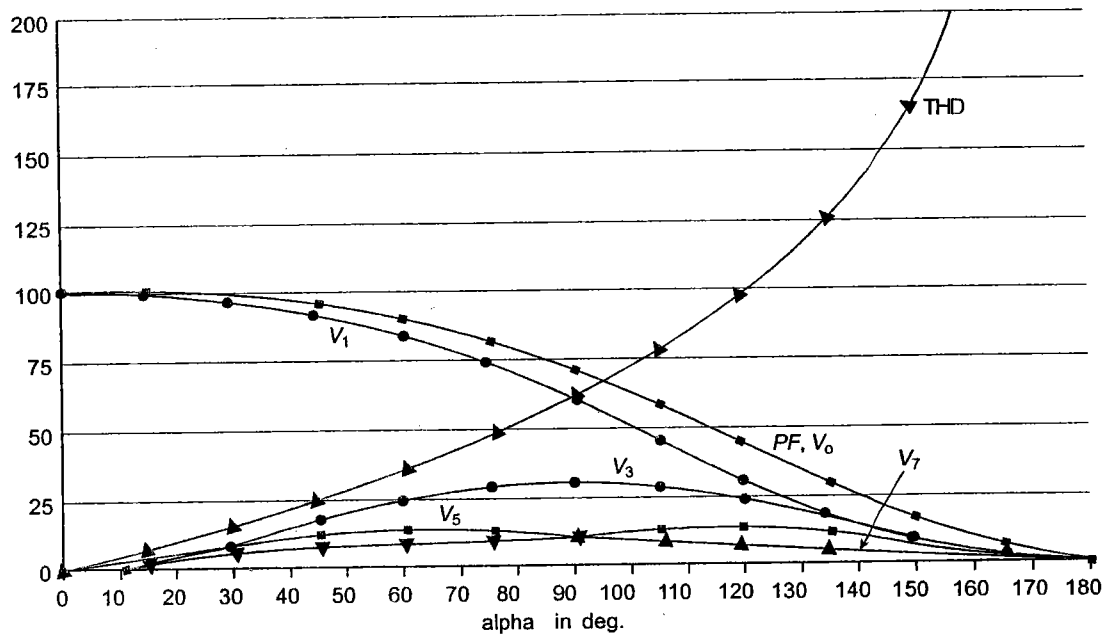


Figure 5.7 Performance of ac regulator with R load (all values in %).

PROGRAM 5.1

```
Cls
REM Fourier analysis by generation of data of given function. REM
for THD and PF of full ac phase-control (ac regulator with R load).
```

```
REM developed by Jamil Asghar, Aligarh Muslim University, Aligarh,
India.
DIM a(2000), b(2000), Y(2000), h(100)
pi# = 4 * ATN(1) / 180rad# = rad# * 180
PRINT "Switching angle, ALPHA (in deg) = ?"
INPUT alfad
th1 = 0
PRINT " last harmonic for calculation = ? "
INPUT lasthar
REM generate data for REED = 1..to.... total no. of data.
REM ttdat = total number of the data to be generated.
REM generate data by giving the function for 180 deg. (waveform
symmetry).
ttdat = 1800
gap = 180 / ttdat
REM here calculation step is, gap = 0.1 deg.
FOR reed = 1 TO ttdat STEP 1
REM generate data for 180/gap points.
  alfa = alfad * rad#
  wttd = gap * reed
  wtt = wttd * rad#
REM generate data by defining the function and boundary
condition.
REM*************************************************************
REM scr can only be triggered when (wt>alfa) for a discontinuous
current.
REM Equat.for input current or output voltage of an ac regulator
with R-load.
10 i1 = 141.42 * SIN(wtt)
20 IF wtt <= alfa THEN i1 = 0
30 i = i1
PRINT wttd, i
REM*************************************************************
REM here y(reed) = given function to be analyzed and stored in
vector.
Y(reed) = I
NEXT reed
FOR j = 1 TO lasthar STEP 2
sinsum# = 0
cossum# = 0
a(j) = 0
b(j) = 0
REM Give gap of wtd calculation.
FOR m = 1 TO ttdat STEP 1
wt = m * gap * rad#
REM calculate different function product for 1/2 time-period (pi)
cossum# = cossum# + Y(m) * COS(j * wt)
sinsum# = sinsum# + Y(m) * SIN(j * wt)
```

```
NEXT m
REM for averaging divide by totat no. of data ttdat.
a(j) = cossum# * 2 / ttdat
b(j) = sinsum# * 2 / ttdat
NEXT j
th1 = 0
th1 = a(1) * a(1) + b(1) * b(1)
fund = SQR(th1 / 2)
th2 = 0
FOR k = 3 TO lasthar STEP 2
h(k) = SQR((a(k) * a(k) + b(k) * b(k)) / 2)
th2 = th2 + a(k) * a(k) + b(k) * b(k)
NEXT k
Irms = SQR((th1 + th2) / 2)
rto = Irms / fund
thd = SQR((rto * rto) - 1)
THDf = 100 * thd
cosphi1 = COS(ATN(a(1) / b(1)))
dpf = 100 * cosphi1
PRINT
"*************************************************************"
PRINT " alpha (deg) Fund'l (%) Irms (%) THDf(%) DPF(%)"
PRINT alfad, fund, Irms, THDf, dpf
PRINT
"*************************************************************"
PRINT " h(3) h(5) h(7) h(9) h(11)"
PRINT h(3), h(5), h(7), h(9), h(11)
PRINT
"*************************************************************"
STOP
END
```

Note: Here in place of statement nos. 10–30, any function of current or voltage of a converter can be defined for the analysis of the converter. Since data are generated from the expression of given function. The logic and boundary conditions of expression of given functions are imposed for different periods of a cycle. Since the actual current (or voltage) response equations are used, the results correspond to the actual circuit conditions.

5.7

FULL WAVE WITH *RL* LOAD

When there is an *RL* load, the load current and hence the thyristor/SCR current does not reduce to zero at $\omega t = \pi$ (Fig. 5.8). Therefore, commutation of SCR does not take place at this instant rather

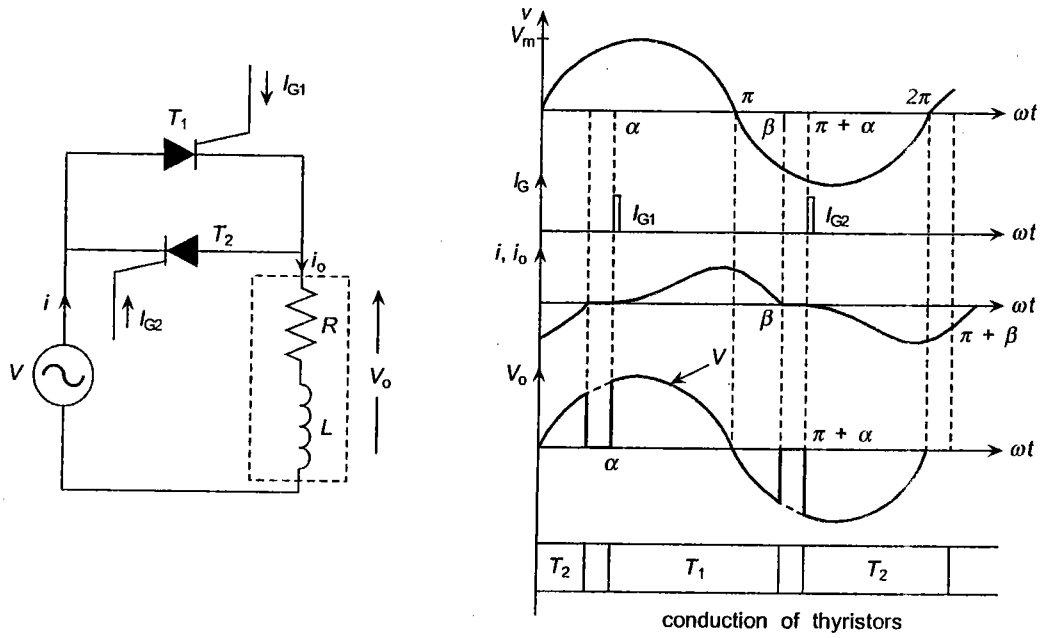


Figure 5.8 AC regulator with RL load.

it depends upon the power-factor angle or the impedance angle of the *RL* load (ϕ). If $\alpha \leq \phi$, the control becomes ineffective, the output voltage remains same as that of the input sinusoidal voltage ($v_o = V$). When $\alpha \geq \theta$, the commutation of thyristor takes place at the extinction angle β, where the load or thyristor current reduces to almost zero level (holding current level). The output voltage and current (v_o, i_o) become discontinuous and the control is possible from 0 to V or (V/Z) for voltage and current, respectively. The expression of current (i_o) for an *RL* load (see Appendix B), is given by

$$i_o = \frac{\sqrt{2}V}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)\exp\frac{\alpha - \omega t}{\tan\phi}\right], \quad \alpha \leq \omega t \leq \beta \quad \text{and} \quad \alpha \geq \phi \quad (5.43)$$

where

$$Z = [R^2 + (\omega L)^2]^{1/2} \quad \text{and} \quad \phi = \tan^{-1}\frac{\omega L}{R}$$

The value of β can be found by solving the above equation for $i_o(\beta) = 0$, which gives

$$\sin(\beta - \phi) - \sin(\alpha - \phi)\exp\frac{\alpha - \beta}{\tan\phi} = 0 \quad (5.44)$$

This is a transcendental equation which can be solved for β. Figure 5.9 and Program 5.2 show β for different values of ϕ. The value of the extinction angle (β) can be found with the help of a simple computer program using the direct substitution technique. Since (for *RL* load,) the current becomes zero between 180° and 360°, computation of β is required in this range only.

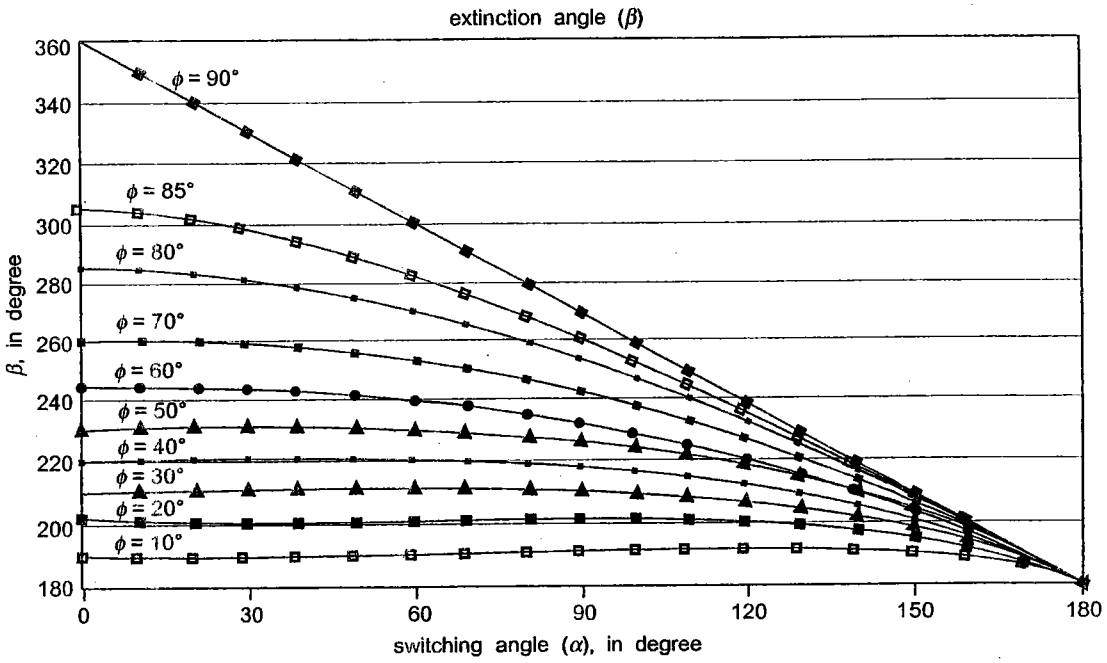


Figure 5.9 Variation of β with respect to ϕ and α.

PROGRAM 5.2

```
PRINT "Program for the extinction angle beta in RL load"
REM developed by Jamil Asghar, Aligarh Muslim University,
Aligarh, India.
pi# = 4 * ATN(1)
PRINT " Program for extinction angle beta for given phi and alpha"
PRINT " Give values of phi and alpha (in degree)"
INPUT phid, alfad
alfa = pi# * alfad / 180
pia = pi# - alfa
phi = phid * pi# / 180
REM calculation is done in p.u. of Im.
FOR jwt = 181 TO 360 STEP 1
wt = jwt * pi# / 180
f = SIN(wt - phi) - (EXP((alfa - wt) / TAN(phi))) * (SIN(alfa -
phi))
BB = jwt
IF f <= 0 THEN GOTO 11
NEXT jwt
11 beta = BB
PRINT phid; alfad; beta
STOP
END
```

The expression of the rms value of the output voltage is given by

$$V_o = \left[\frac{1}{\pi}\int_{\alpha}^{\beta}(\sqrt{2}\,V\sin\omega t)^2\,d(\omega t)\right]^{1/2} = V\left\{\frac{1}{\pi}\left[(\beta-\alpha)+\frac{1}{2}\sin 2\alpha-\frac{1}{2}\sin 2\beta\right]\right\}^{1/2} \quad (5.45)$$

Similarly, the rms value of the line or load current is given by

$$I_o = \left\{\frac{1}{\pi}\int_{\alpha}^{\beta}[i_o(\omega t)]^2\,d(\omega t)\right\}^{1/2} = \left\{\frac{1}{\pi}\int_{\alpha}^{\beta}\left[\frac{\sqrt{2}\,V}{Z}\left(\sin(\omega t-\phi)-\sin(\alpha-\phi)\exp\frac{\alpha-\omega t}{\tan\phi}\right)\right]^2 d(\omega t)\right\}^{1/2}$$

The above equation can be solved by numerical technique or by direct integration. Alternatively, the harmonic analysis of the current can be done with the help of the voltage expression and the impedance of the load. Therefore,

$$v_o(\omega t) = \frac{a_0}{2} + \sum_{n=1,2,\ldots}^{\infty}[a_n\cos(n\omega t) + b_n\sin(n\omega t)]$$

where

$$a_0 = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t)\,d(\omega t) = 0$$

$$a_n = \frac{2}{\pi}\int_{\alpha}^{\beta}\sqrt{2}\,V\sin\omega t\cos(n\omega t)\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\int_{\alpha}^{\beta}[\sin(1-n)\,\omega t+\sin(1+n)\,\omega t]\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\left\{\frac{1}{1-n}[\cos(1-n)\,\alpha-\cos(1-n)\beta]+\frac{1}{1+n}[\cos(1+n)\alpha-\cos(1+n)\beta]\right\} \quad (5.46)$$

$$b_n = \frac{2}{\pi}\int_{\alpha}^{\beta}\sqrt{2}\,V\sin\omega t\sin(n\omega t)\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\int_{\alpha}^{\beta}[\cos(1-n)\,\omega t-\cos(1+n)\,\omega t]\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\left\{\frac{1}{1-n}[\sin(1-n)\beta-\sin(1-n)\,\alpha]+\frac{1}{1+n}[\sin(1+n)\beta-\sin(1+n)\alpha]\right\} \quad (5.47)$$

for $n = 3, 5, \ldots, n \neq 1$.

Also,

$$a_1 = \frac{2}{\pi}\int_{\alpha}^{\beta}\sqrt{2}\,V\sin(\omega t)\cos(\omega t)\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\int_{\alpha}^{\beta}\sin(2\omega t)\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{2\pi}(\cos 2\alpha - \cos 2\beta) \tag{5.48}$$

$$b_1 = \frac{2}{\pi}\int_{\alpha}^{\beta}\sqrt{2}V\sin(\omega t)\sin(\omega t)\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\int_{\alpha}^{\beta}(1-\cos 2\omega t)\,d(\omega t)$$

$$= \frac{\sqrt{2}V}{\pi}\left[(\beta-\alpha) + \frac{1}{2}\sin 2\alpha - \frac{1}{2}\sin 2\beta\right] \tag{5.49}$$

The load impedance (Z) is given by

$$Z = \sqrt{\left[R^2 + (n\omega L)^2\right]}\angle\phi_n \quad \text{and} \quad \phi_n = \tan^{-1}\frac{n\omega L}{R} \tag{5.50}$$

Now, the required expression for the load current is given by

$$i_o(\omega t) = \sum_{n=1,3,5}^{\infty}\sqrt{2}\,I_n\sin(n\omega t - \phi_n + \theta_n) \tag{5.51}$$

where

$$\theta_n = \tan^{-1}\frac{a_n}{b_n} \quad \text{and} \quad I_n = \left[\frac{(a_n^2 + b_n^2)/2}{R^2 + (n\omega L)^2}\right]^{1/2} \tag{5.52}$$

Alternatively, Program 5.3 gives the calculation of various parameters for *RL* load. Here data are generated from the current equation from α to $\pi + \alpha$ and for half-cycle duration. Accordingly, the limits are defined for the calculation.

PROGRAM 5.3

```
CLS
REM Fourier analysis by GENERATION of data of the given FUNCTION.
REM Developed by Jamil Asghar, Aligarh Muslim University, Aligarh,
India.
DIM a(2000), b(2000), Y(2000), h(200)
OPEN "o", #1, "resultfile"
pi# = 4 * ATN(1)
rad# = pi# / 180
```

```
PRINT "Impedance angle of RL cicuit, PHI (in deg) = ?"
INPUT phid
PRINT "Switching angle, ALPHA (in deg) = ?",
INPUT alfad
PRINT "last harmonic = ?"
INPUT lasthar
th1 = 0
REM generate data for REED = 1..to.... total no. of data.
REM ttdat = total number of the data to be generated.
REM generate data by giving the function for 180 deg. (waveform
symmetry).
ttdat = 1800
gap = 180/ttdat

REM here calculation step is, gap = 0.1 deg.
FOR reed = 1 TO ttdat STEP 1
REM generate data for 180/gap points.
  alfa = alfad * rad#
  phi = phid * rad#
  wttd = gap * reed
  wtt = wttd * rad#
REM generate data by defining the function and boundary
condition.
REM*************************************************************
REM scr can only be triggered when (wt>alfa) for a discontinuous
current.
10 i1 = 141.42 * (SIN(wtt - phi) - SIN(alfa - phi) * EXP((alfa -
wtt) / TAN(phi)))
20 IF wtt <= alfa THEN i1 = 0
30 i2 = -141.42 * (SIN(wtt + pi# - phi) - SIN(alfa - phi) *
EXP((alfa - wtt - pi#) / TAN(phi)))
40 IF i2 > 0 THEN i2 = 0
50 i = i1 + i2
60 PRINT wttd, i
REM*************************************************************
REM here y(reed) = given function to be analysed and stored in
vector.
Y(reed) = i
NEXT reed
FOR j = 1 TO lasthar STEP 2
sinsum# = 0
cossum# = 0
a(j) = 0
b(j) = 0
REM Give gap of wtd calculation.
FOR m = 1 TO ttdat STEP 1
wt = m * gap * rad#
REM Calculate different function product for 1/2 time-period (pi)
```

```
cossum# = cossum# + Y(m) * COS(j * wt)
sinsum# = sinsum# + Y(m) * SIN(j * wt)
NEXT m
REM For averaging divide by totat no. of data ttdat.
a(j) = cossum# * 2 / ttdat
b(j) = sinsum# * 2 / ttdat
NEXT j
th1 = 0
th1 = a(1) * a(1) + b(1) * b(1)
fund = SQR(th1 / 2)
th2 = 0
FOR k = 3 TO lasthar STEP 2
h(k) = SQR((a(k) * a(k) + b(k) * b(k)) / 2)
th2 = th2 + a(k) * a(k) + b(k) * b(k)
NEXT k
Irms = SQR((th1 + th2) / 2)
rto = Irms / fund
thd = SQR((rto * rto) - 1)
THDf = 100 * thd
cosphi1 = COS(ATN(a(1) / b(1)))
pf = 100 * cosphi1 / rto
PRINT "*************************************************************"
PRINT " alpha (deg) Fund'l (%) Irms (%) THDf(%) PF(%)"
PRINT alfad, fund, Irms, THDf, pf
PRINT "-------------------------------------"
PRINT " h(3) h(5) h(7) h(9) h(11)"
PRINT h(3), h(5), h(7), h(9), h(11)
PRINT "*************************************************************"
STOP
END
```

Note: Most part of this program is same as given in Program 5.1.

5.8

AC REGULATORS WITH PURE INDUCTORS

For a purely inductive load, $\phi = 90°$. The output voltage control is effective for $\pi/2 \leq \alpha \leq \pi$ only, for which v_o varies from V to 0. The current and voltage waveforms of a thyristor controlled reactor (TCR) are shown in Fig. 5.10. The expression for the load current is given by

$$i_o(\omega t) = \frac{\sqrt{2}V}{\omega L}\left[\sin\left(\omega t - \frac{\pi}{2}\right) - \sin\left(\alpha - \frac{\pi}{2}\right)\exp\frac{\alpha - \omega t}{\tan(\pi/2)}\right]$$

$$= \frac{\sqrt{2}V}{\omega L}(\cos\alpha - \cos\omega t) \qquad (5.53)$$

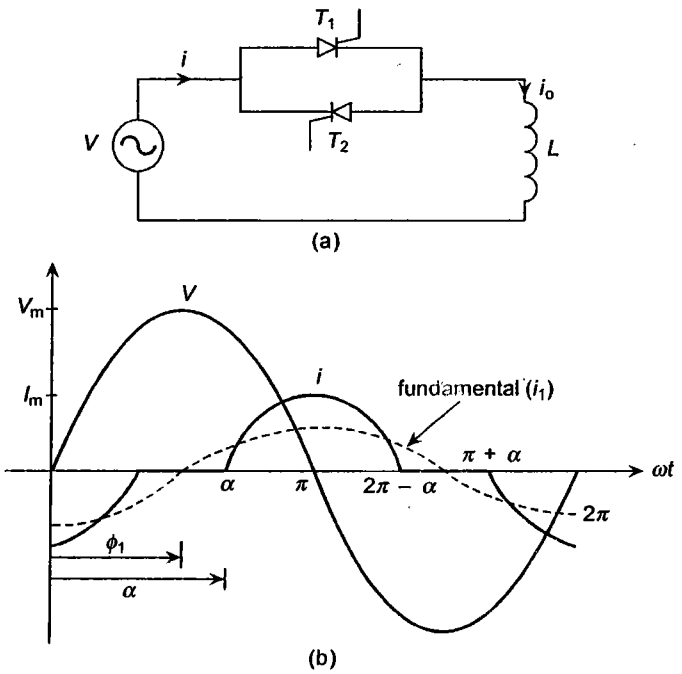


Figure 5.10 Voltage and current waveforms of TCR or *L* load.

The line and the load current are discontinuous and partially sinusoidal. The value of β can be found as

$$i_o(\beta) = 0 = \cos\alpha - \cos\beta$$

which gives,

$$\beta = 2\pi - \alpha \tag{5.54}$$

The fundamental and harmonic terms can be found from the Fourier series. For purely inductive load, $\beta = 2\pi - \alpha$. Therefore,

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} i_o(\omega t)(\cos\omega t)\, d(\omega t)$$

Integrating for half-cycle, we get

$$a_1 = \frac{2}{\pi}\int_\alpha^\beta \frac{\sqrt{2}V}{\omega L}(\cos\alpha - \cos\omega t)(\cos\omega t)\, d(\omega t)$$

$$= \frac{2\sqrt{2}V}{\pi\omega L}\int_\alpha^\beta \left[\cos\alpha\cos\omega t - \frac{1}{2}(1 + \cos 2\omega t)\right] d(\omega t)$$

$$= \frac{2\sqrt{2}V}{\pi\omega L}\left\{\cos\alpha(\sin\beta - \sin\alpha) - \frac{1}{2}\left[(\beta - \alpha) + \frac{1}{2}(\sin 2\beta - \sin 2\alpha)\right]\right\} \tag{5.55}$$

$$= \frac{\sqrt{2}V}{\pi\omega L}\left[2(\pi - \alpha) + \sin 2\alpha\right] \qquad \text{for } \beta = 2\pi - \alpha \tag{5.56}$$

Also,

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} i_o(\omega t)(\sin \omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\int_\alpha^\beta \frac{\sqrt{2}V}{\omega L}(\cos\alpha - \cos\omega t)(\sin\omega t)\, d(\omega t)$$

$$= \frac{\sqrt{2}V}{2\pi\omega L}\left[-\cos 2\alpha + \cos 2\beta - 4\cos\alpha(\cos\beta - \cos\alpha)\right]$$

$$= 0 \quad (\text{for } \beta = 2\pi - \alpha) \tag{5.57}$$

Similarly,

$$a_n = \frac{2}{\pi}\int_\alpha^\beta \frac{\sqrt{2}V}{\omega L}(\cos\alpha - \cos\omega t)(\cos n\omega t)\, d(\omega t)$$

$$= \frac{\sqrt{2}V}{2\pi\omega L}\left\{\frac{2}{n+1}\left[\sin(n+1)\alpha - \sin(n+1)\beta\right] - \frac{2}{n-1}\left[\sin(n-1)\alpha - \sin(n-1)\beta\right]\right.$$

$$\left. - \frac{4\cos\alpha}{n}(-\sin n\beta + \sin n\alpha)\right\} \quad \text{for } n = 3, 5, 7, \ldots, n \neq 1 \tag{5.58}$$

and

$$b_n = \frac{2}{\pi}\int_\alpha^\beta \frac{\sqrt{2}V}{\omega L}(\cos\alpha - \cos\omega t)(\sin n\omega t)\, d(\omega t)$$

$$= \frac{\sqrt{2}V}{2\pi\omega L}\left\{\frac{2}{n+1}\left[-\cos(n+1)\alpha + \cos(n+1)\beta\right] - \frac{2}{n-1}\left[-\cos(n-1)\alpha + \cos(n-1)\beta\right]\right.$$

$$\left. - \frac{4\cos\alpha}{n}(\cos n\beta - \cos n\alpha)\right\}, \quad \text{for } n = 3, 5, 7, \ldots, n \neq 1 \tag{5.59}$$

The rms value of the fundamental components of the current is given by

$$I_1 = \left(\frac{a_1^2 + b_1^2}{2}\right)^{1/2} = \frac{V}{\pi\omega L}\left[2(\pi - \alpha) + \sin 2\alpha\right] \tag{5.60}$$

The rms value of the line or input current (I) and the load current (I_o) can be found from the current equation, which is given by

$$I = I_o = \left[\frac{1}{\pi}\int_\alpha^\beta I_m^2(\cos\alpha - \cos\omega t)^2\, d(\omega t)\right]^{1/2}, \quad \text{where } I_m = \frac{\sqrt{2}V}{\omega L}$$

$$= I_m \left\{ \frac{1}{\pi} \int_{\alpha}^{2\pi-\alpha} [\cos^2\alpha + \cos^2(\omega t) - 2\cos\alpha \cos\omega t]\, d(\omega t) \right\}^{1/2}$$

$$= I_m \left\{ \frac{1}{\pi} \left[\cos^2\alpha \int_{\alpha}^{2\pi-\alpha} d(\omega t) + \frac{1}{2} \int_{\alpha}^{2\pi-\alpha} (1 + \cos 2\omega t)\, d(\omega t) - 2\cos\alpha \int_{\alpha}^{2\pi-\alpha} \cos(\omega t)\, d(\omega t) \right] \right\}^{1/2}$$

$$= I_m \left(\frac{1}{\pi} \left\{ \cos^2\alpha (2\pi - 2\alpha) + \frac{1}{2} \left[2(\pi - \alpha) - \frac{1}{2}\sin 2\alpha - \frac{1}{2}\sin 2\alpha \right] - 2\cos\alpha (-\sin\alpha - \sin\alpha) \right\} \right)^{1/2}$$

$$= I_m \left\{ \frac{1}{\pi} \left[(\pi - \alpha)(1 + 2\cos^2\alpha) + \frac{3}{2}\sin 2\alpha \right] \right\}^{1/2} \tag{5.61}$$

Now, with the help of I_1 and I, THD can be found.

Example 5.6 For a thyristor-controlled reactor (TCR), the switching angle, $\alpha = 150°$. Find the fundamental components and the total harmonic distortion (THD) of the input current in per-unit value.

Solution A TCR is an ac voltage regulator with a purely inductive load (Fig. 5.10). The input current for a purely inductive circuit is given by

$$i(\omega t) = I_m (\cos\alpha - \cos\omega t), \qquad \text{for } \frac{\pi}{2} \le \alpha \le 2\pi - \alpha$$

and the rms value of the input current is

$$I = I_m \left\{ \frac{1}{\pi} \left[(\pi - \alpha)(1 + 2\cos^2\alpha) + \frac{3}{2}\sin 2\alpha \right] \right\}^{1/2}$$

For $\alpha = 150°$ (or $5\pi/6$),

$$I = I_m \sqrt{\frac{1}{\pi} \left[\frac{\pi}{6} + \frac{\pi}{3}\left(\frac{3}{4}\right) + \frac{3}{2}\left(-\frac{\sqrt{3}}{2}\right) \right]} = 0.056 I_m$$

The fundamental of the input current is given by

$$I_1 = \frac{I_m}{\sqrt{2}\pi} \left[(2\pi - \alpha) + \sin 2\alpha \right] = \frac{I_m}{\sqrt{2}\pi} \left(\frac{1}{3}\pi - \frac{\sqrt{3}}{2} \right) = 0.04 I_m$$

Therefore,

$$\text{THD} = \sqrt{\left(\frac{I}{I_1}\right)^2 - 1} = \sqrt{\left(\frac{0.056 I_m}{0.04 I_m}\right)^2 - 1} = 0.0979 \quad \text{or} \quad 97.9\%$$

Example 5.7 A capacitor is connected across a TCR to control the fine capacitive VAR (Fig. 5.11). Calculate, for $\alpha = 135°$: (a) the total reactive power, (b) the fundamental component of the input-line current, (c) THD of the inductive current alone and (d) THD of the line current.

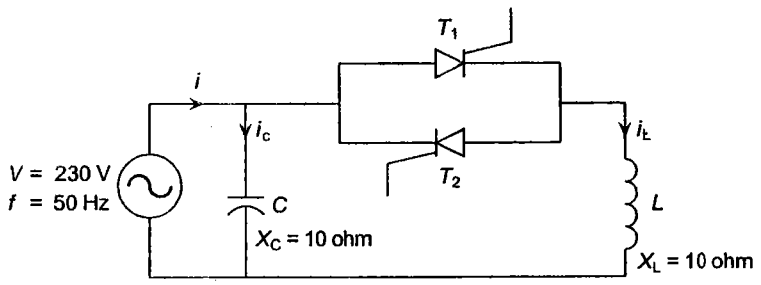


Figure 5.11 Fine capacitive VAR control by TCR (Example 5.7).

Solution The rms value of the fundamental inductor current is given by

$$I_{L1} = \frac{\sqrt{2}V}{\pi\omega L}(2\alpha - 2\pi - 2\sin 2\alpha)$$

$$= \frac{\sqrt{2} \times 230}{10\pi}\left(\frac{3\pi}{2} - 2\pi - 2\sin\frac{3\pi}{2}\right)$$

$$= -4.17 \text{ A}$$

The effective impedance and VAR of TCR, at $\alpha = 135°$, are given by

$$X_1 = \frac{V}{I_{L1}} = \frac{230}{4.17} = 55.15\ \Omega$$

$$Q_L = \frac{V_2}{X_1} = \frac{(230)^2}{55.15} = 959.2 \text{ VA}$$

Also,

$$I_C = \frac{V}{X_C} = \frac{230}{10} = 23 \text{ A}$$

$$Q_C = \frac{V^2}{X_C} = \frac{(230)^2}{10} = 5290 \text{ VA}$$

(a) The net reactive VAR is given by

$$Q = Q_C - Q_L = 5290 - 959.2 = 4330.8 \text{ VA} \quad \text{(leading)}$$

Also it can be found as

$$Q = VI_C - VI_{L1} = 230 \times 23 - 230 \times 4.17 = 4330.9 \text{ VA (leading)}$$

(b) The rms value of the fundamental input current,

$$I_1 = \sqrt{I_{L1}^2 + I_C^2} = \sqrt{(4.17)^2 + (23)^2} = 23.37 \text{ A}$$

(c) The rms value of the inductor current,

$$I_L = I_m \left\{\frac{1}{\pi}\left[(\pi - \alpha)(1 + 2\cos^2\alpha) + \frac{3}{2}\sin 2\alpha\right]\right\}^{1/2}$$

$$= \frac{\sqrt{2}V}{\omega L}\left(\frac{1}{\pi}\left\{\left(\pi - \frac{3\pi}{4}\right)\left[1 + 2(\cos 135°)^2\right] + \frac{3}{2}\sin(270°)\right\}\right)^{1/2}$$

$$= \frac{\sqrt{2}V}{10}\left\{\frac{1}{\pi}\left[\frac{\pi}{4}(1 + 1) - \frac{3}{2}\right]\right\}^{1/2}$$

$$= 4.88 \text{ A}$$

THD of the inductive current I_L alone, is given by

$$\text{THD}_{IL} = 100\sqrt{\left(\frac{I_L}{I_{L1}}\right)^2 - 1} = 100\sqrt{\left(\frac{4.88}{4.17}\right)^2 - 1} = 60.78\%$$

The rms value of the line current is given by

$$I = \sqrt{I_L^2 + I_C^2} = \sqrt{(4.88)^2 + (23)^2} = 23.51 \text{ A}$$

THD of the line current is given by

$$\text{THD}_I = 100\sqrt{\left(\frac{I}{I_1}\right)^2 - 1} = 100\sqrt{\left(\frac{23.51}{23.37}\right)^2 - 1} = 10.96\%$$

5.9

THREE-PHASE AC REGULATORS

For high-power requirements, the distorted waveform of the line current, causes unbalancing in the three-phase line current. An unbalanced current flows in the neutral. Although a substantial magnitude (about 15%) is allowed but, in general, it is avoided. Therefore, for high power applications (above a few kW), three-phase systems are used.

5.9.1 Circuit Configurations

A large number of a three-phase ac regulator circuit configurations are possible as shown in Fig. 5.12. However, the circuit configurations shown in Figs. 5.12a and 5.12e are most commonly used circuits for Y and Δ connected loads, respectively. In these two cases, only the line current flows and no current flows in neutral. Therefore, at least two thyristors of different phases should be conducting. The circuit configurations shown in Figs. 5.12b and 5.12g are, in fact, three single-phase ac regulators connected in Y and Δ, respectively. Each switch (thyristor pair) independently controls the voltage across each load. The configuration, as shown in Fig. 5.12b, is restricted to lower-power ac regulators only (because the third harmonics are present in current due

to a large neutral current). In case of a delta configuration (Fig. 5.12d), the third harmonic current is restricted in the line current. The analysis of the single-phase ac regulator is valid for these cases.

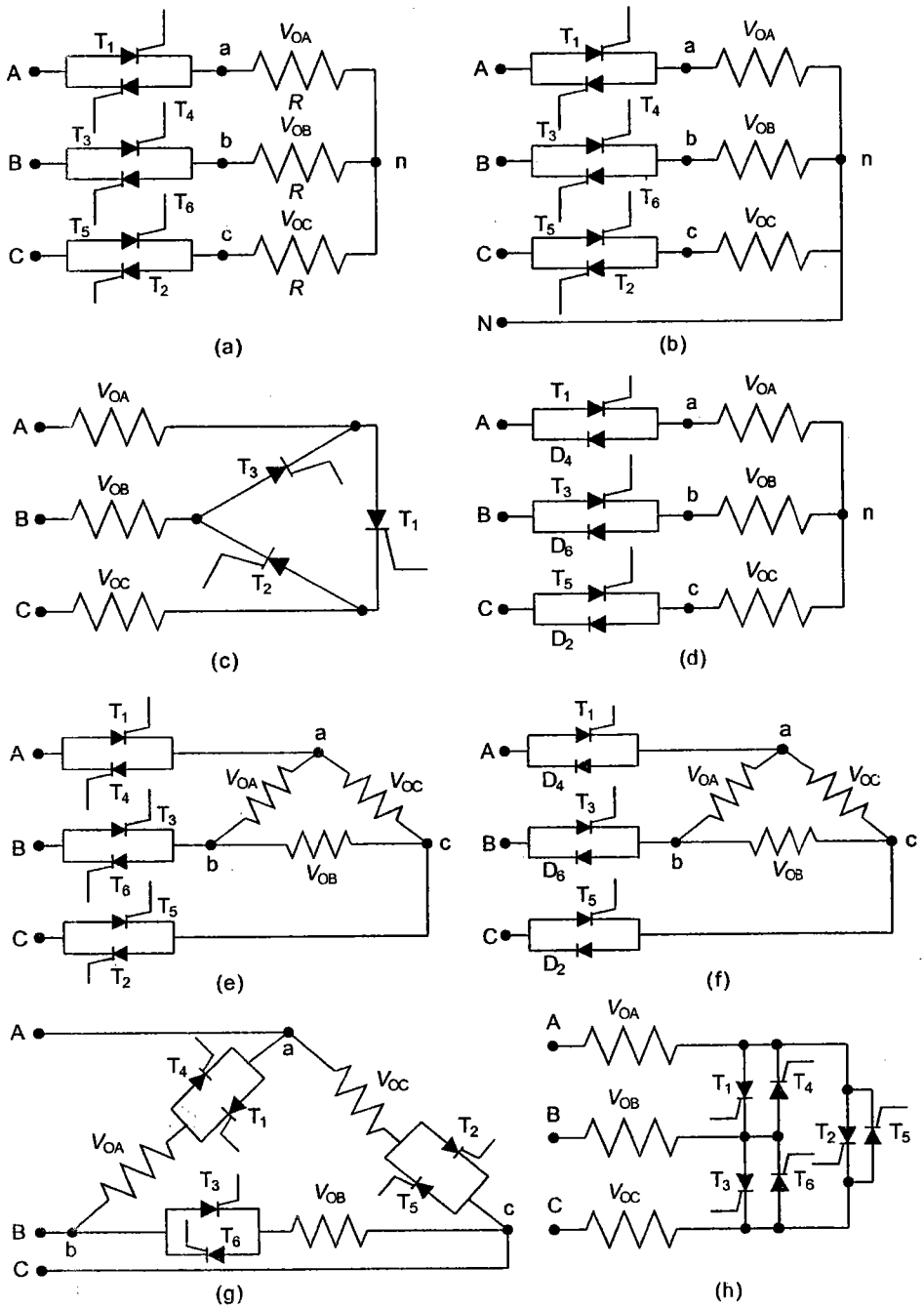


Figure 5.12 Circuit configurations of ac regulators with Y and delta-connected loads.

The remaining configurations are not very common as they suffer from different demerits. All the six terminals of the loads should be available for the configurations shown in Figs. 5.12e and 5.12g. By replacing one thyristor/SCR with a diode, the cost of regulators can be reduced (Fig. 5.12d). However, due to unidirectional control (e.g. in positive half-cycle only), the voltage waveforms are not symmetric in both the half-cycles. Therefore, even harmonics are present in the line current, which is undesirable.

5.9.2 Y-CONNECTED, *R* LOADS

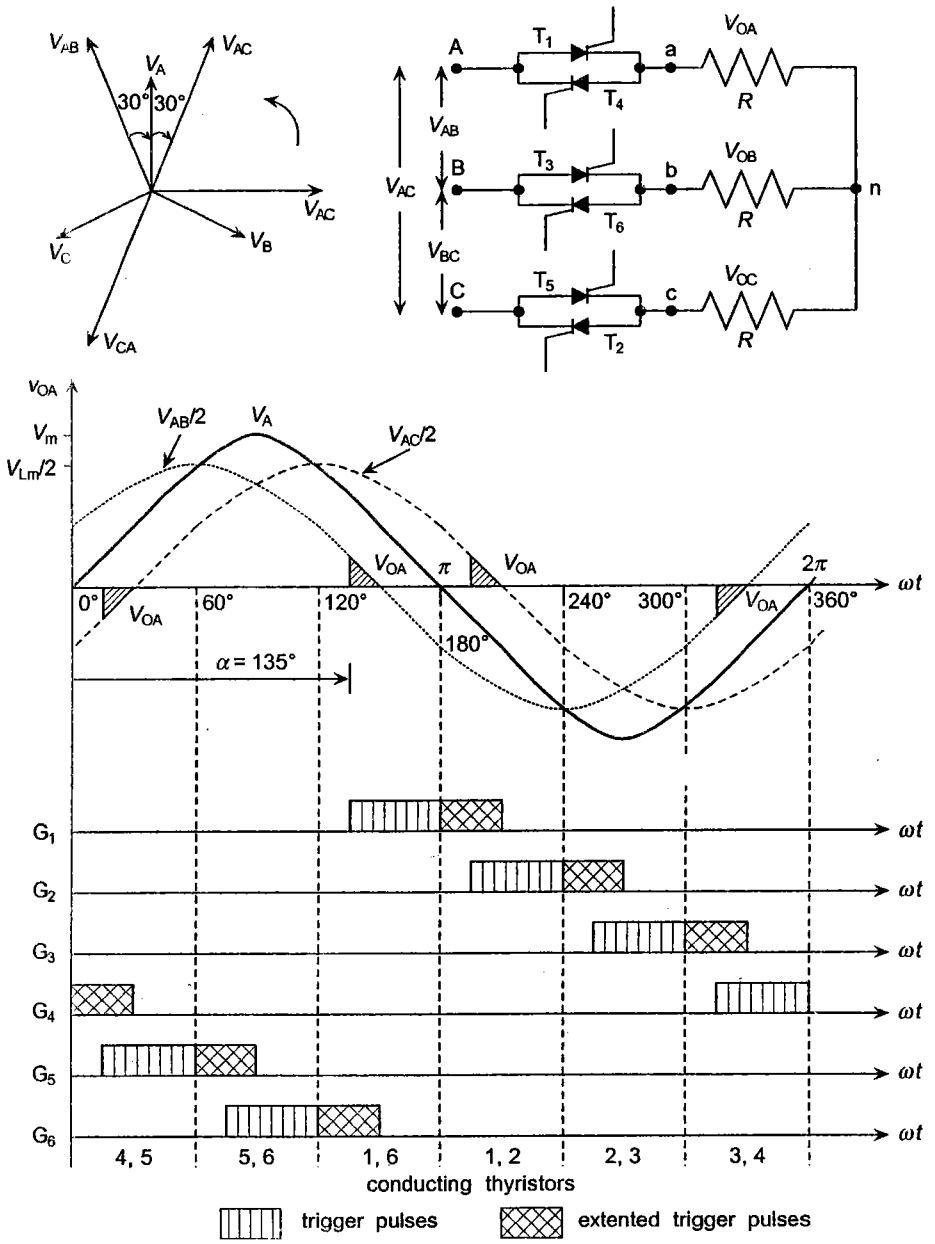
As discussed earlier, three-phase, three-wire (without neutral) type configurations are common. Since the commutation of thyristors depends upon the load current, which in turn, depends upon the applied voltage as well as impedance angle (ϕ). Therefore, to analyze a resistive load is simpler than an RL load. Here, for the sake of simplicity, only purely resistive loads are considered. Since phase voltage or half of the line voltage appears across the load, therefore the phase voltage (V_A) vector is taken as reference (Fig. 5.13). For a three-phase system, each line-voltage remains higher than all the other line-voltages for 120° (duration) only, e.g. from 30° to 150°, in case of V_{AB}. It will be seen as Chapter 6, a three-phase diode bridge starts conduction at $\omega t = 30°$ for the input current in phase *A*. Moreover, at this instant v_A is also zero. Therefore, this point is taken as reference for triggering a thyristor. Different line and phase voltages are shown in Fig. 5.13 for phase A and their equations are given by:

$$\left.\begin{aligned} V_A &= \sqrt{2}\, V \sin \omega t \\ V_{AB} &= (\sqrt{3}\sqrt{2}V) \sin\left(\omega t + \frac{\pi}{6}\right) \\ V_{AC} &= (\sqrt{3}\sqrt{2}V) \sin\left(\omega t - \frac{\pi}{6}\right) \end{aligned}\right\} \quad (5.62)$$

It becomes easy to draw the waveforms using the waveform exercise sheet, given in Appendix (Fig. A12).

For a successful conduction, two or three thyristors of different phases must be conducting at a time. Therefore, a single-pulse gate-signal is not enough, as the switching instant of each thyristor is different. Thus a train of trigger signal is required for the whole duration of conduction. Moreover, with the help of duration of triggering pulse, the duration of conduction of a thyristor for each phase can be easily found. For a resistive load, the thyristor for each line-voltage can conduct up to $\omega t = 180°$ only. The conduction can start at $\omega t = 30°$ and ends at $\omega t = 180°$. Therefore, the range of control of α is $5\pi/6$ or 150° only. To maintain a balanced line-current, it is necessary to symmetrically trigger the thyristors. Therefore, the trigger sequence should be α, $\alpha + 120°$ and $\alpha + 240°$ for the positive group thyristors, T_1, T_3 and T_5, respectively. Similarly, the trigger sequence should be $(\alpha + 180°)$, $(\alpha + 300°)$ and $(\alpha + 420°)$ or $(\alpha + 60°)$ for negative group thyristors T_2, T_4 and T_6, respectively. G_1, G_2, G_3, G_4, G_5 and G_6 are the gate terminals of these thyristors. Depending upon the value of α, there are three different modes of switching. It is important to note that two thyristors must be conducting at a time. Therefore, either double gate pulses with a separation of 60° are required for each thyristor, or a train of gate pulses of desired duration (about 180° or 210°). For example, the trigger pulses for T_1 which start at α and cease at 180°, will be sufficient. However, when α becomes large ($\alpha \geq 120°$), this duration should be extended slightly higher than 210°.

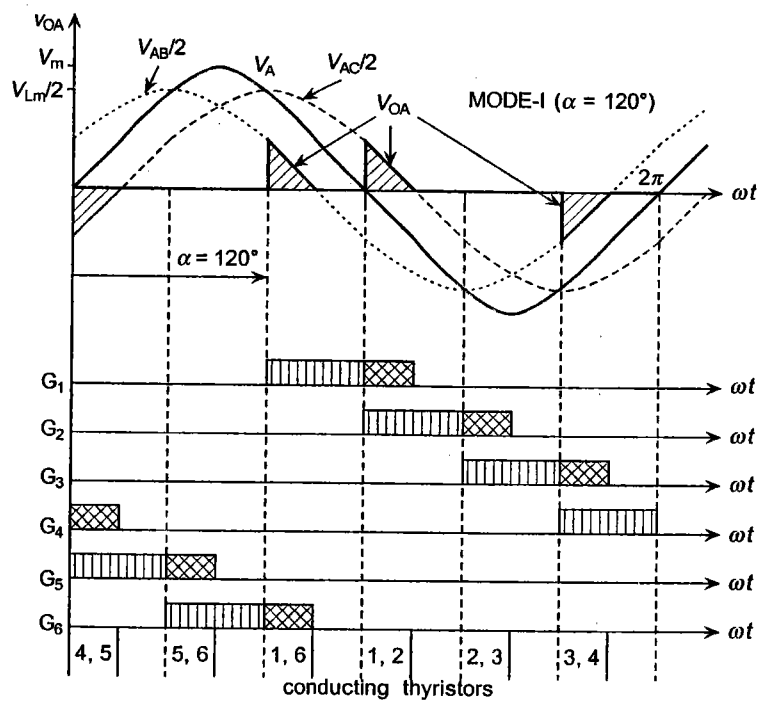
Therefore, in general, the duration of the trigger pulses should be $(180° - \alpha)$. For $\alpha \geq 120°$, it should be extended to slightly more than $(210° - \alpha)$. The shaded portion shows the extended trigger pulses (Fig. 5.13a). It may also be noted that if the triggering pulses are extended up to 210°, switching of the regulator is possible in all modes but ascertaining the switching status of a thyristor becomes difficult (in the presence of gate signals). Since, even in the presence of gate pulses, the beginning of



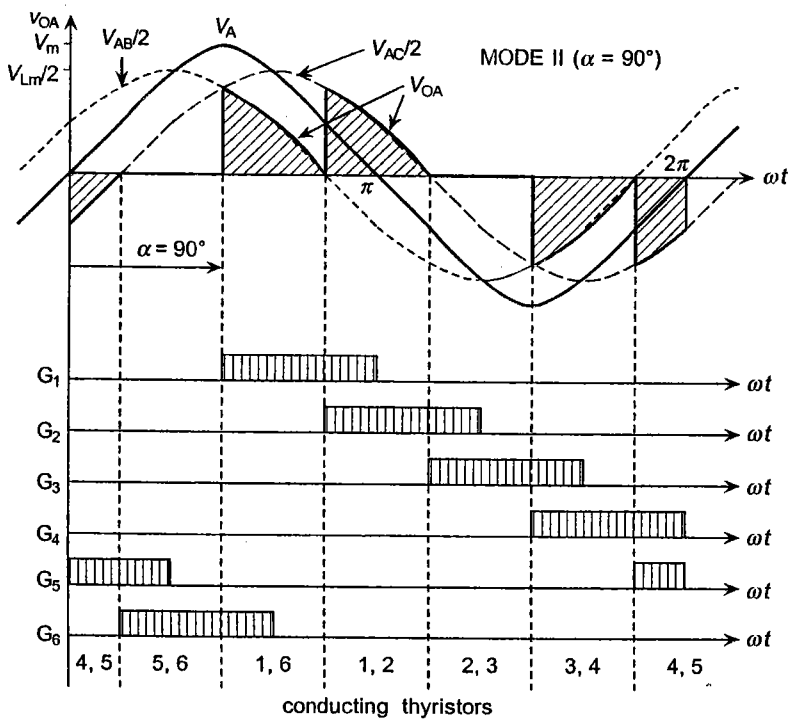
Mode-I (α = 135°)

(a)

Figure 5.13 *(Cont.)*



(b)



(c)

Figure 5.13 (*Cont.*)

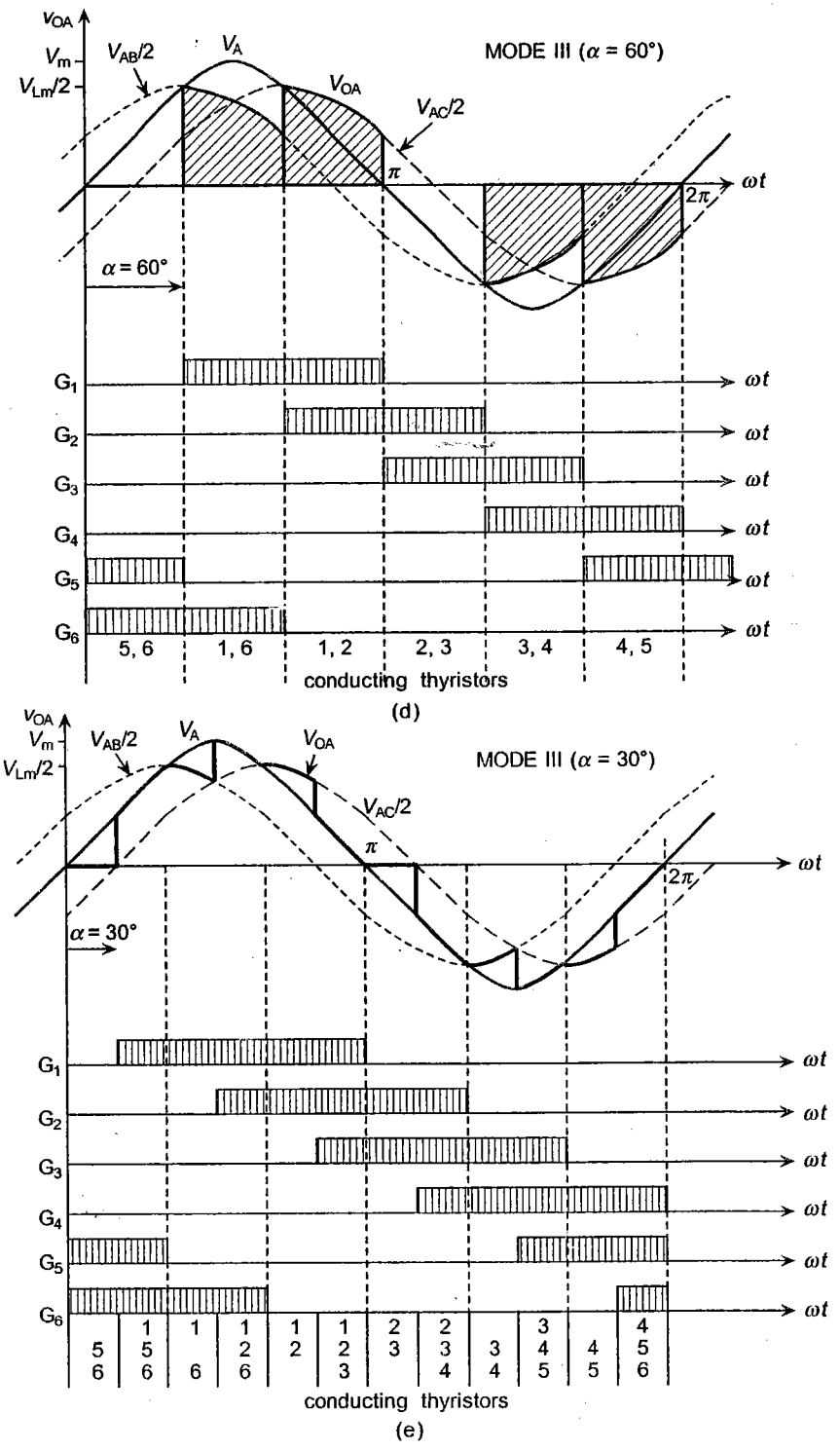


Figure 5.13 Three-phase, three-wire, Y-connected R loads ac regulator: (a) α = 135°, (b) α = 120° (c) α = 90°, (d) α = 60° and (e) α = 30°.

conduction of a thyristor depends upon the biasing, i.e. it conducts only when the anode voltage exceeds the cathode voltage. There are different modes of switching which are being discussed here:

(a) Mode I ($90° \le \alpha \le 150°$): In this mode either two thyristors of different phase conduct together or none conducts at all (Fig. 5.13a and b). If α exceeds 150°, two thyristors cannot conduct simultaneously and hence the load voltage becomes zero. Therefore, the load voltages v_{OA}, v_{OB} and v_{OC} are either zero or equal to half of the line voltage v_L. The output is discontinuous with two voltage pulses in each half-cycle. The load voltage v_{OA} is either $(1/2)v_{AB}$, $(1/2)v_{AC}$ or zero. Similarly for v_{OB}, it is $(1/2)v_{BC}$, $(1/2)v_{BA}$ or zero and v_{OC} is $(1/2)v_{CA}$, $(1/2)v_{CB}$ or zero. Therefore, a sustained trigger signal or a second trigger signal after 60°, is required for each thyristor. The rms value of load voltage of phase A is given by

$$V_{an} = V_{OA} = \left[2\frac{1}{\pi}\int_{\alpha}^{5\pi/6}\left[\frac{\sqrt{3}\sqrt{2}V}{2}\sin\left(\omega t + \frac{\pi}{6}\right)\right]^2 d(\omega t)\right]^{1/2}, \quad 90° \le \alpha \le 150° \qquad (5.63)$$

For simplification, if reference of the sine function and hence its limits are changed by $\pi/6$, the analysis will be similar to that of a single-phase ac regulator. Therefore,

$$V_{OA} = \left[2\frac{1}{\pi}\int_{\alpha+(\pi/6)}^{\pi}\left(\frac{\sqrt{3}\sqrt{2}V}{2}\sin\omega t\right)^2 d(\omega t)\right]^{1/2} \qquad (5.64)$$

$$= \sqrt{3}V\left\{\frac{1}{2\pi}\left[\pi - \alpha - \frac{\pi}{6} + \frac{1}{2}\sin 2\left(\alpha + \frac{\pi}{6}\right)\right]\right\}^{1/2}$$

$$= V_L\left[\frac{1}{2\pi}\left(\frac{5\pi}{6} - \alpha + \frac{1}{4}\sin 2\alpha + \frac{\sqrt{3}}{4}\cos 2\alpha\right)\right]^{1/2} \qquad (5.65)$$

(b) Mode II ($60° \le \alpha \le 90°$): In this mode, two thyristors of different phases always conduct (Figs. 5.13c and d). Therefore, the load voltage is always $(1/2)V_L$, i.e. either $(1/2)V_{AB}$ or $(1/2)V_{AC}$ for the load voltage, v_{OA}. The rms value of the load voltage is given by

$$V_{OA} = \left\{2\frac{1}{\pi}\int_{\alpha}^{\alpha+(\pi/3)}\left[\frac{\sqrt{3}\sqrt{2}V}{2}\sin\left(\omega t + \frac{\pi}{6}\right)\right]^2 d(\omega t)\right\}^{1/2}, \quad 60° \le \alpha \le 90°$$

$$= \left[\frac{2}{\pi}\int_{\alpha+(\pi/6)}^{\alpha+(\pi/2)}\left(\frac{\sqrt{3}\sqrt{2}V}{2}\sin\omega t\right)^2 d(\omega t)\right]^{1/2} \quad \text{(reference changed)}$$

$$= V_L\left[\frac{1}{2\pi}\left(\frac{\pi}{3} + \frac{3}{4}\sin 2\alpha + \frac{\sqrt{3}}{4}\cos 2\alpha\right)\right]^{1/2} \qquad (5.66)$$

(c) Mode III ($0 \le \alpha \le 60°$): In this mode, when $\alpha = 0$, three thyristors of different phases always conduct and the load voltage (v_{OA}) is equal to the phase voltage, v_A (Fig. 5.13e). However, if α is increased, sometimes only two thyristors conduct at a time depending upon the circuit conditions. Therefore, for example, the load voltage (v_{OA}) will be either the phase voltage (v_A) or the half of the line voltage [$(1/2)v_{AB}$ or $(1/2)v_{AC}$]. The rms value of the load voltage is given by

$$V_{OA} = \left\{ \frac{2}{\pi} \left[\int_{\alpha}^{\pi/3} v_A^2 \, d(\omega t) + \int_{\alpha}^{\alpha+(\pi/3)} \left(\frac{v_{AB}}{2} \right)^2 d(\omega t) + \int_{\alpha+(\pi/3)}^{2\pi/3} v_A^2 \, d(\omega t) \right. \right.$$

$$\left. \left. + \int_{2\pi/3}^{\alpha+(2\pi/3)} \frac{v_{AC}}{2} \, d(\omega t) + \int_{\alpha+(2\pi/3)}^{\pi} v_A^2 \, d(\omega t) \right] \right\}^{1/2} \tag{5.67}$$

where

$$v_A = \sqrt{2}\, V \sin \omega t, \quad v_{AB} = \sqrt{2}\sqrt{3}\, V \sin\left(\omega t + \frac{\pi}{6} \right)$$

and

$$v_{AC} = \sqrt{2}\sqrt{3}\, V \sin\left(\omega t - \frac{\pi}{6} \right)$$

or,

$$V_{an} = V_{OA} = V_L \left[\frac{1}{\pi} \left(\frac{\pi}{3} - \frac{\alpha}{2} + \frac{\sin 2\alpha}{4} \right) \right]^{1/2} \tag{5.68}$$

The load voltage (v_{OA}) is shown for $\omega t = 60°$ in Fig. 5.13d. Since T_1 is triggered at $\omega t = 60°$, and T_6 was conducting, which allows $(1/2)v_{AB}$ voltage to appear across the load. Again, when T_2 is triggered, commutation of T_6 takes place (line commutation). The conduction takes place through T_1 and T_2, as now v_{AC} becomes higher than v_{AB} (or phase C is more negative than phase B). In the same manner, although T_1 and T_2 are conducting at $\omega t = 180°$, where $v_{AC} \neq 0$. But, due to incoming conduction of T_3, it commutates T_1, where v_B is higher than v_A (anode of T_1, i.e. $v_A = 0$ and cathode of T_1 attains a higher potential through the load due to v_B).

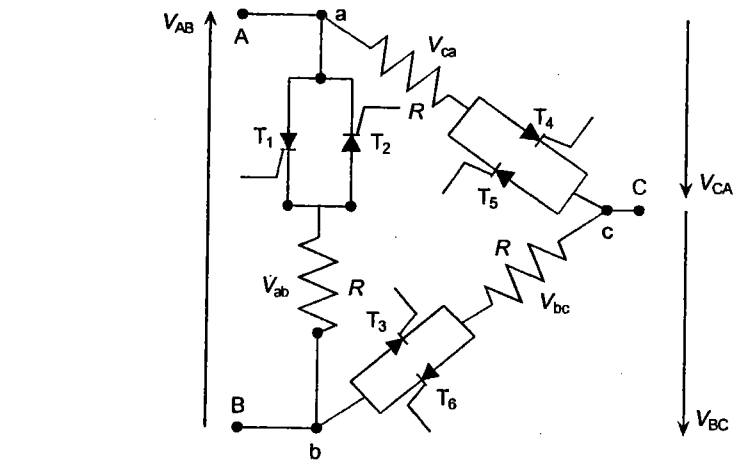
5.9.3 Delta-connected Load (*T-R* Load Configuration)

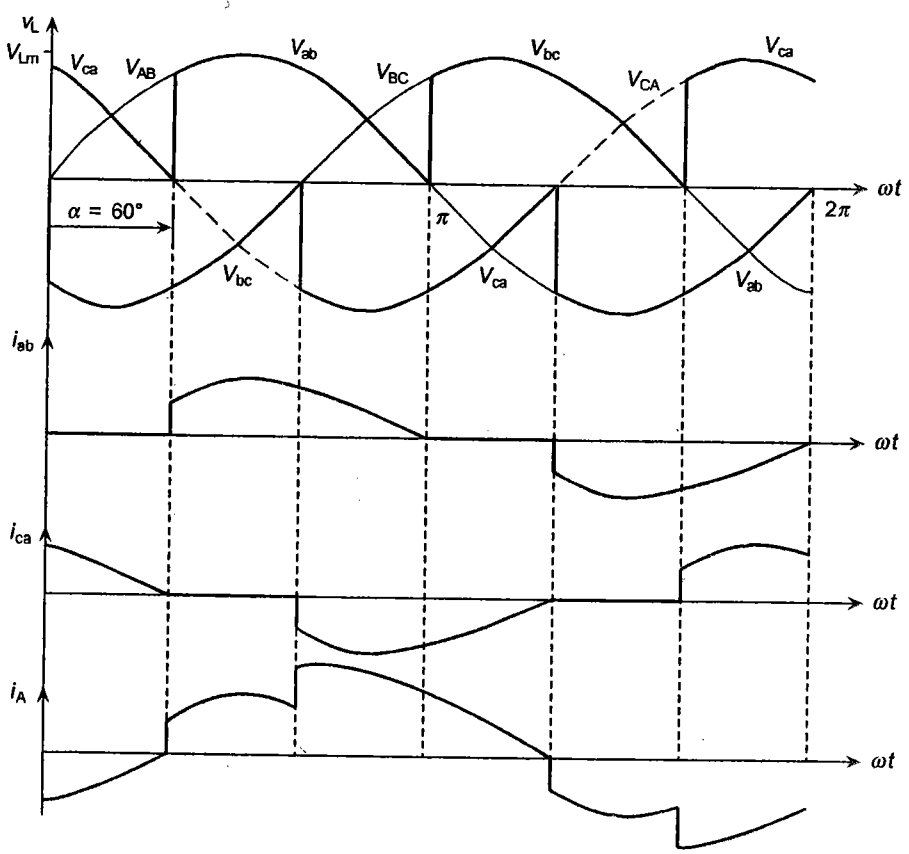
In this case, the conduction of each thyristor is independent of the other (Fig. 5.14). Therefore, each load behaves as a single-phase load. Similarly, the load voltage of one phase is independent of other phases. However, the line current is sum of instantaneous currents of two phases, i.e.

$$i_A = i_{ab} + i_{ac}, \quad i_B = i_{bc} + i_{ba}, \quad i_C = i_{ca} + i_{cb} \tag{5.69}$$

where i_A, i_B, i_C and i_{ab}, i_{bc}, i_{ca} are line and phase currents, respectively. Here the line voltage (V_L) is taken as a reference. The rms value of the output voltage of phase *A*, is given by

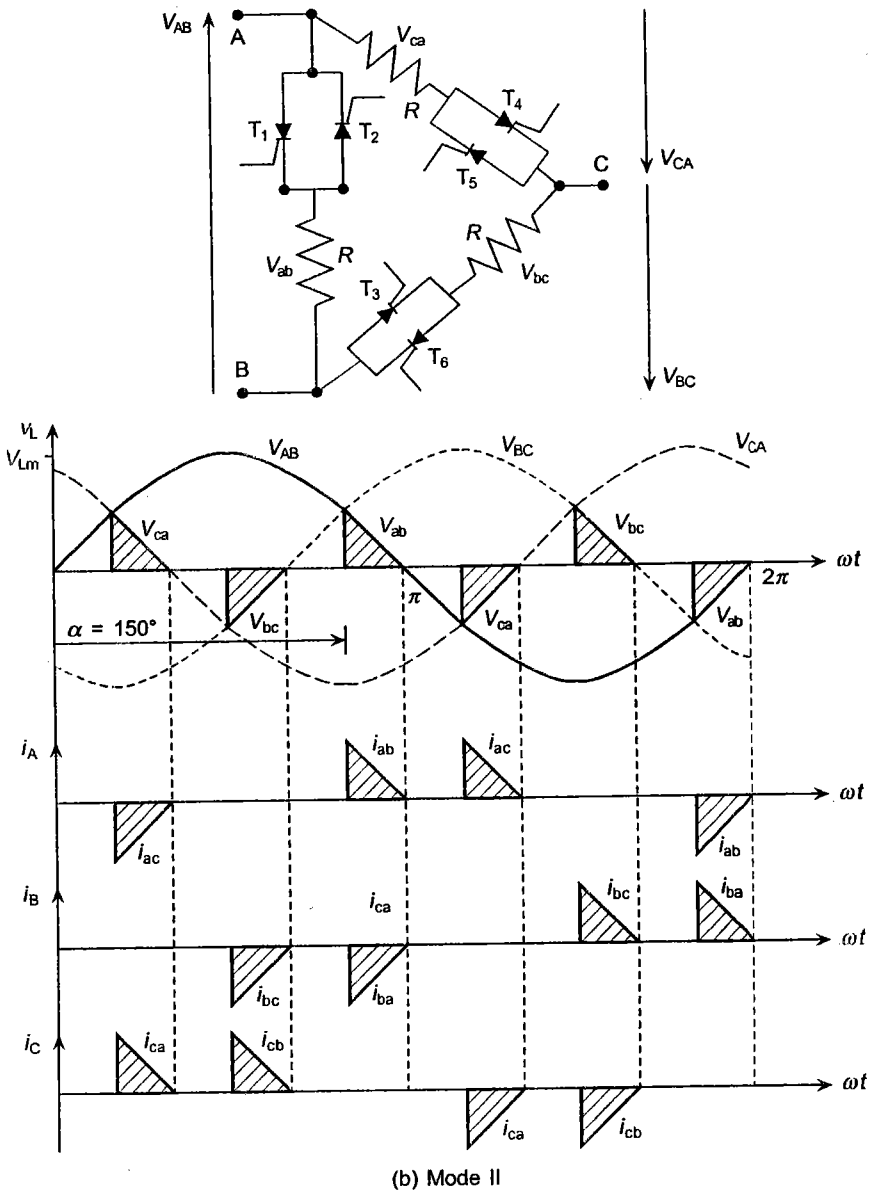
$$V_{ab} = V_L \left\{ \frac{1}{\pi} \left[(\pi - \alpha) + \frac{1}{2} \sin 2\alpha \right] \right\}^{1/2} \tag{5.70}$$





(a) Mode I

Figure 5.14 (*Cont.*)



(b) Mode II

Figure 5.14 Three-phase, delta-connected thyristor and load (*T-R*) configuration.

where V_{AB}, V_{BC} and V_{CA} are line voltages. The output voltage or the voltage across the resistance (R) connected between the terminals ab, bc and ca are V_{ab}, V_{bc} and V_{ca}, respectively. Figure 5.14b shows the load voltage phase and line currents for $\alpha = 150°$. Here, both the line current and phase current are discontinuous. The rms value of the phase current is given by

$$I_{ab} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} i_{ab}^2(\omega t)\, d(\omega t)\right]^{1/2} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi}\left(\frac{v_{ab}}{R}\right)^2 d(\omega t)\right]^{1/2} = \frac{V_{ab}}{R} \tag{5.71}$$

Since the line current is sum of the phase current ($i_A = i_{ab} + i_{ac}$). In this case, the waveforms of both i_{ab} and i_{ac} are similar. The rms value of I_A is given by

$$I_A = \left[\frac{2}{\pi}\int_{\alpha}^{\pi} i_{ab}^2(\omega t)\, d(\omega t)\right]^{1/2} = \sqrt{2}\, I_{ab} \tag{5.72}$$

For $\alpha < 120°$, the conduction period of different phase current overlaps. At $\alpha = 60°$, the conduction period for each half-cycle is 180°, as shown in Fig. 5.14a. The rms value of the phase current can be found using the equation for I_{ab}. The rms value of the line current can be found using the expression

$$I_A = \left\{\frac{1}{\pi}\left[\int_0^{\pi/3}(-i_{ca})^2\, d(\omega t) + \int_{\alpha}^{2\pi/3}(i_{ab})^2\, d(\omega t) + \int_{2\pi/3}^{\pi}(i_{ab} - i_{ca})^2 d(\omega t)\right]\right\}^{1/2} \tag{5.73}$$

5.9.4 Delta-connected *R* Loads

In this case, two thyristors of different phases must be conducting for the flow of current. When the current is flowing in one resistor, it also flows in two resistors of other phases with a half magnitude due to double impedance (2R). The current flows through the resistor between *ab* terminals, when T_1–T_4 and T_3–T_6 pair are conducting. At this condition (Fig. 5.15), the output voltage is given by

$$V_{OA} = V_{ab} = V_L\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)\right]^{1/2} \tag{5.74}$$

Whenever, the current flows in a load due to conduction of thyristor pairs, it also flows in the remaining two-load impedances of the delta circuit. A voltage equal to the half of the line voltage appears across these two-load impedances. Therefore, when T_1–T_4 and T_5–T_2 pairs are conducting,

$$V_{OA} = V_{ab} = \frac{V_L}{2}\left[\frac{1}{\pi}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)\right]^{1/2} \tag{5.75}$$

Therefore, the line current is given by

$$\begin{aligned} i_A &= i_{ab} - i_{ca} = \frac{V_{ab} - V_{ca}}{R} \\ i_B &= i_{bc} - i_{ab} = \frac{V_{bc} - V_{ab}}{R} \\ i_C &= i_{ca} - i_{bc} = \frac{V_{ca} - V_{bc}}{R} \end{aligned} \tag{5.76}$$

The output voltage for the above case can be found using the expression

$$V_{OA} = \frac{1}{\pi}\left\{\left[\int_{\pi/3}^{2\pi/3}\left(\frac{-v_{BC}}{2}\right)^2 d(\omega t) + \int_{2\pi/3}^{\pi}(v_{AB})^2\, d(\omega t) + \int_{\pi}^{4\pi/3}\left(\frac{-v_{CA}}{2}\right)^2 d(\omega t)\right]\right\}^{1/2} \tag{5.77}$$

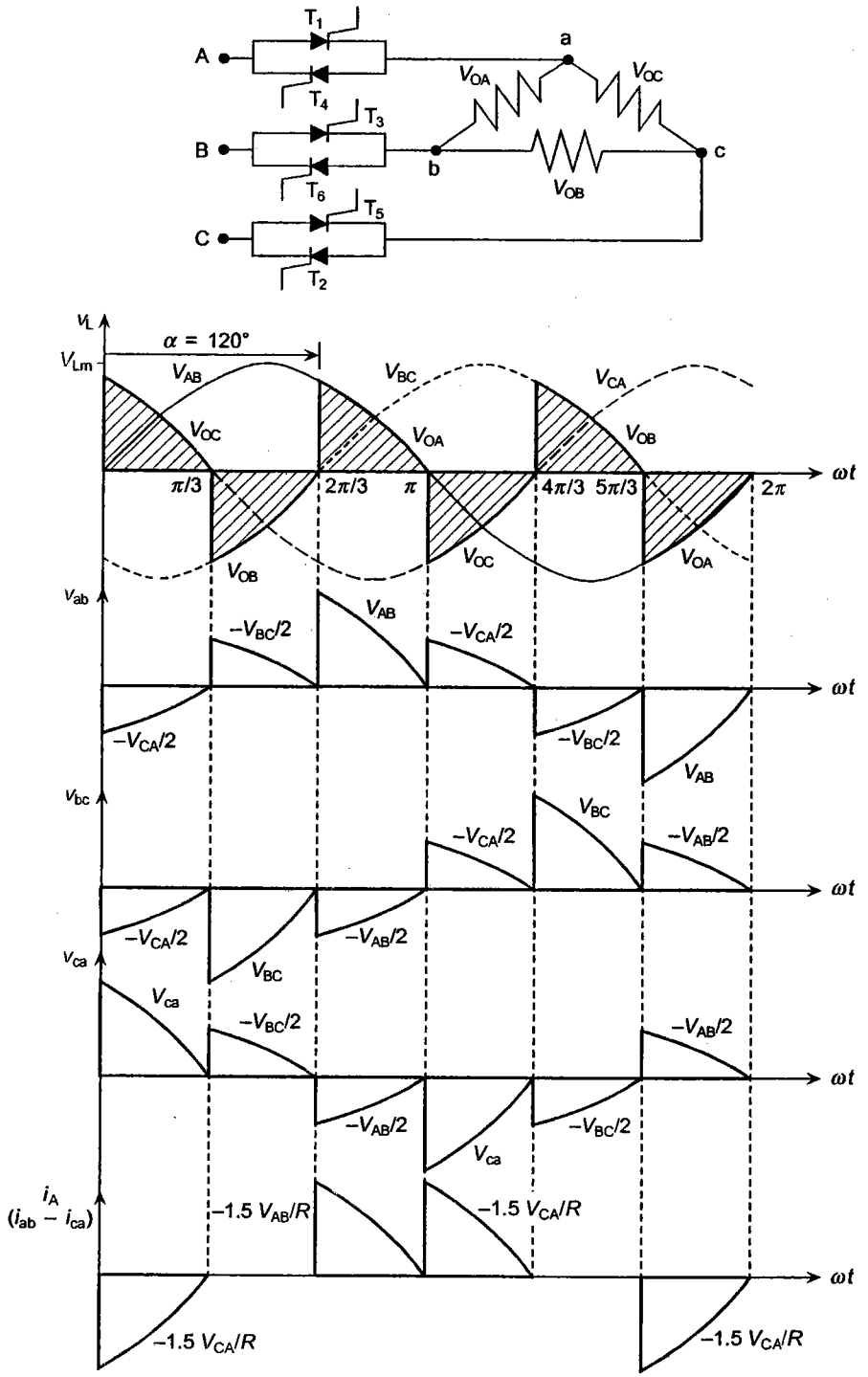


Figure 5.15 Three-phase, ac regulator with delta-connected R load.

where

$$\left.\begin{aligned} v_{AB} &= \sqrt{2}\, V_L \sin \omega t = \sqrt{2}\sqrt{3}\, V \sin \omega t \\ v_{BC} &= \sqrt{2}\sqrt{3}\, V \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_{CA} &= \sqrt{2}\sqrt{3}\ V \sin\left(\omega t + \frac{2\pi}{3}\right) \\ V_{Lm} &= \sqrt{2}\, V_L \end{aligned}\right\} \quad (5.78)$$

5.10 ELECTRONIC TAP CHANGERS

The output voltage does not remain sinusoidal for the fine voltage control by ac regulators. It becomes discontinuous and contains higher-order harmonics. A conventional tap-changer switching arrangement can be used to control the output or secondary voltage of a transformer in steps (Fig. 5.16a). When S_1 or S_2 is closed, the output voltage (V_o) becomes equal to V or xV, respectively (where $x \leq 1$). Similarly, V_o can be controlled in several steps, by increasing the number of tappings and switches. In this arrangement, a fine control of V_o is not possible. The conventional tap changer circuit becomes an electronic tap changer, if switches are replaced by thyristor-pairs. In this case, a fine voltage control of V_o is possible from 0 to V, using a phase-control switching technique (as discussed in Section 5.3). For the output voltage $0 < V_o < xV$, only T_3 and T_4 are switched between α to π and $(\pi + \alpha)$ to 2π, respectively (just like any other ac voltage regulator). The output voltage is given by

$$V_o = xV \left\{\frac{1}{\pi}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]\right\}^{1/2} \quad (5.79)$$

However, for the output voltage, $xV \leq V_o \leq V$, T_3 and T_4 are switched at 0 and π, respectively. While T_1 and T_2 are switched at α and $(\pi + \alpha)$, respectively, as shown in Fig. 5.16b. Here, since there is no discontinuity and the output voltage is close to sinusoidal wave shape, THD reduces drastically. For a resistive load, the current waveform is same as V_o, where $i_o = V_o/R$.

For an *RL* load, the load current continues to flow even after $\omega t = \pi$ and extinct at β. Figure 5.16c shows the current and the output voltage waveforms. Just after $\omega t = 2\pi$ or 0, T_2 continues to conduct due to the inductive load current. Thus the voltage V reaches at the cathode of T_3. When T_3 receives trigger signal at $\omega t = 2\pi$ or 0, it does not come into conduction as its anode voltage, xV is lower than V. Similarly, since T_1 conducts beyond π and up to β, during this period, V reaches at the anode of T_4 (where V is more negative than xV). Thus T_4 does not conduct till T_1 ceases its conduction at β.

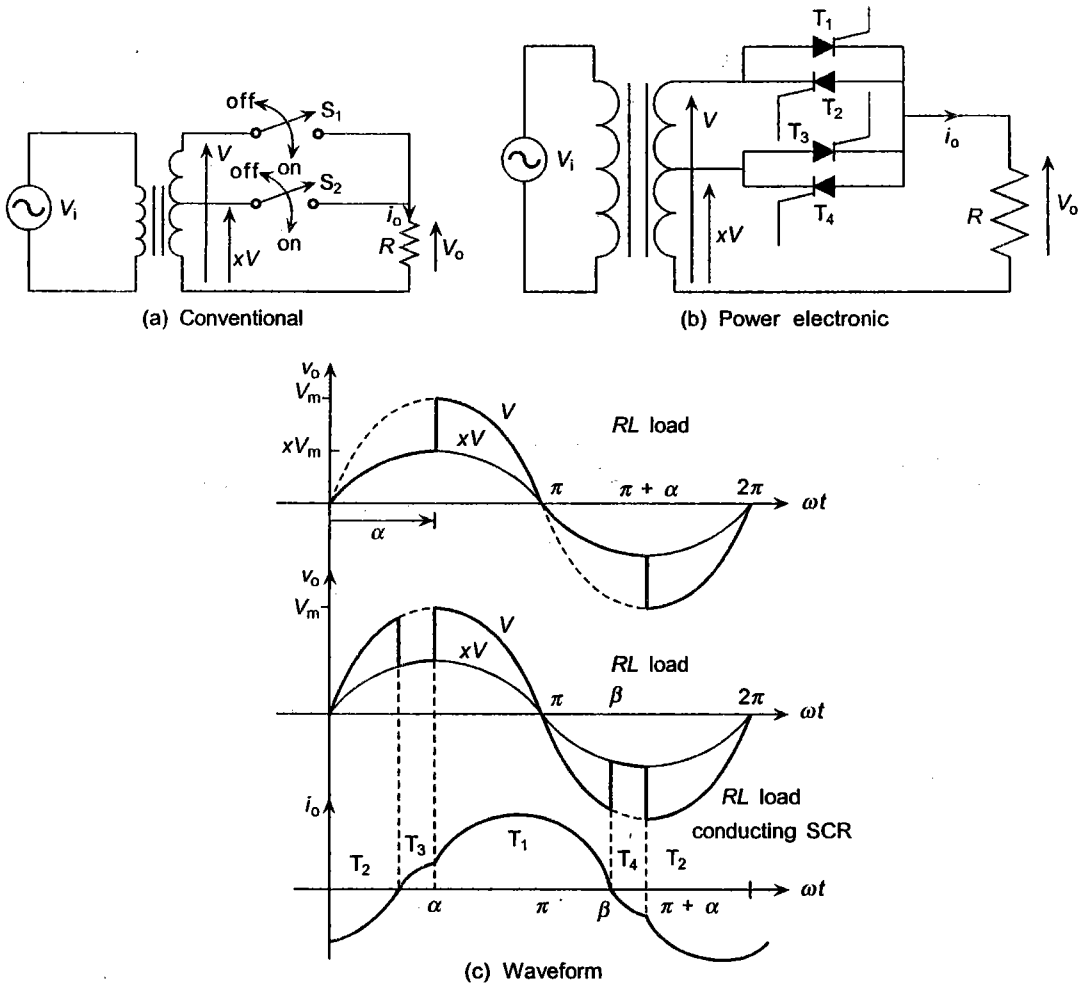


Figure 5.16 Tap changer arrangement.

For a resistive load, the harmonics of the output voltage can be found by Fourier series, which are given by

$$a_n = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t)(\cos n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\left[\int_0^{\alpha} x\sqrt{2}\,V(\sin \omega t)(\cos n\omega t)\, d(\omega t) + \int_{\alpha}^{\pi}\sqrt{2}V(\sin \omega t)(\cos n\omega t)\, d(\omega t)\right]$$

$$= \frac{\sqrt{2}V}{\pi}(1 - x)\left[\frac{\sin (n + 1)\,\alpha}{n + 1} - \frac{\sin (n - 1)\,\alpha}{n - 1}\right] \qquad (5.80)$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t)(\sin n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\left[\int_0^{\alpha} x\sqrt{2}V(\sin \omega t)(\sin n\omega t)\, d(\omega t) + \int_{\alpha}^{\pi} \sqrt{2}\, V(\sin \omega t)(\sin n\omega t)\, d(\omega t)\right]$$

$$= \frac{\sqrt{2}V}{\pi}\left\{(1-x)\left[\frac{\cos(n+1)\alpha}{n+1} - \frac{\cos(n-1)\alpha}{n-1}\right] - \frac{1}{n+1} + \frac{1}{n-1}\right\} \quad (5.81)$$

Also,

$$a_1 = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t)(\cos \omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\left[\int_0^{\alpha} x\sqrt{2}\, V(\sin \omega t)(\cos \omega t)\, d(\omega t) + \int_{\alpha}^{\pi} \sqrt{2}\, V(\sin \omega t)(\cos \omega t)\, d(\omega t)\right]$$

$$= \frac{\sqrt{2}V}{2\pi}\left[(1-x)(\sin 2\alpha - 2\alpha) + 2\pi\right] \quad (5.82)$$

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} v_o(\omega t)(\sin \omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\left[\int_0^{\alpha} x\sqrt{2}\, V(\sin \omega t)(\sin \omega t)\, d(\omega t) + \int_{\alpha}^{\pi} \sqrt{2}\, V(\sin \omega t)(\sin \omega t)\, d(\omega t)\right]$$

$$= \frac{\sqrt{2}V}{2\pi}(1-x)(\cos 2\alpha - 1) \quad (5.83)$$

The rms value of output voltage is given by

$$V_o = \left\{\frac{1}{\pi}\left[\int_0^{\alpha} (\sqrt{2}\, xV \sin \omega t)^2\, d(\omega t) + \int_{\alpha}^{\pi} (\sqrt{2}\, V \sin \omega t)^2\, d(\omega t)\right]\right\}^{1/2}$$

$$= V\left\{\frac{1}{2\pi}\left[(1-x^2)(\sin 2\alpha) + 2\pi\right]\right\}^{1/2} \quad (5.84)$$

Since, for a resistive load, the current waveform is same as the voltage waveform, THD of the line or input current will be same as that of the output voltage. It can be found using the above three equations. The input power factor is given by

$$\text{PF} = \frac{V_o}{V} = \left\{\frac{1}{2\pi}\left[(1-x^2)(\sin 2\alpha - 2\alpha) + 2\pi\right]\right\}^{1/2} \quad (5.85)$$

5.11

AC CHOPPER REGULATORS

This type of ac voltage regulator is not very common because it requires either gate-commutation devices (e.g. GTO, MOSFET or IGBT) or thyristors with forced commutation circuit. The circuit arrangements and the relevant waveforms are shown in Fig. 5.17. To make the waveform

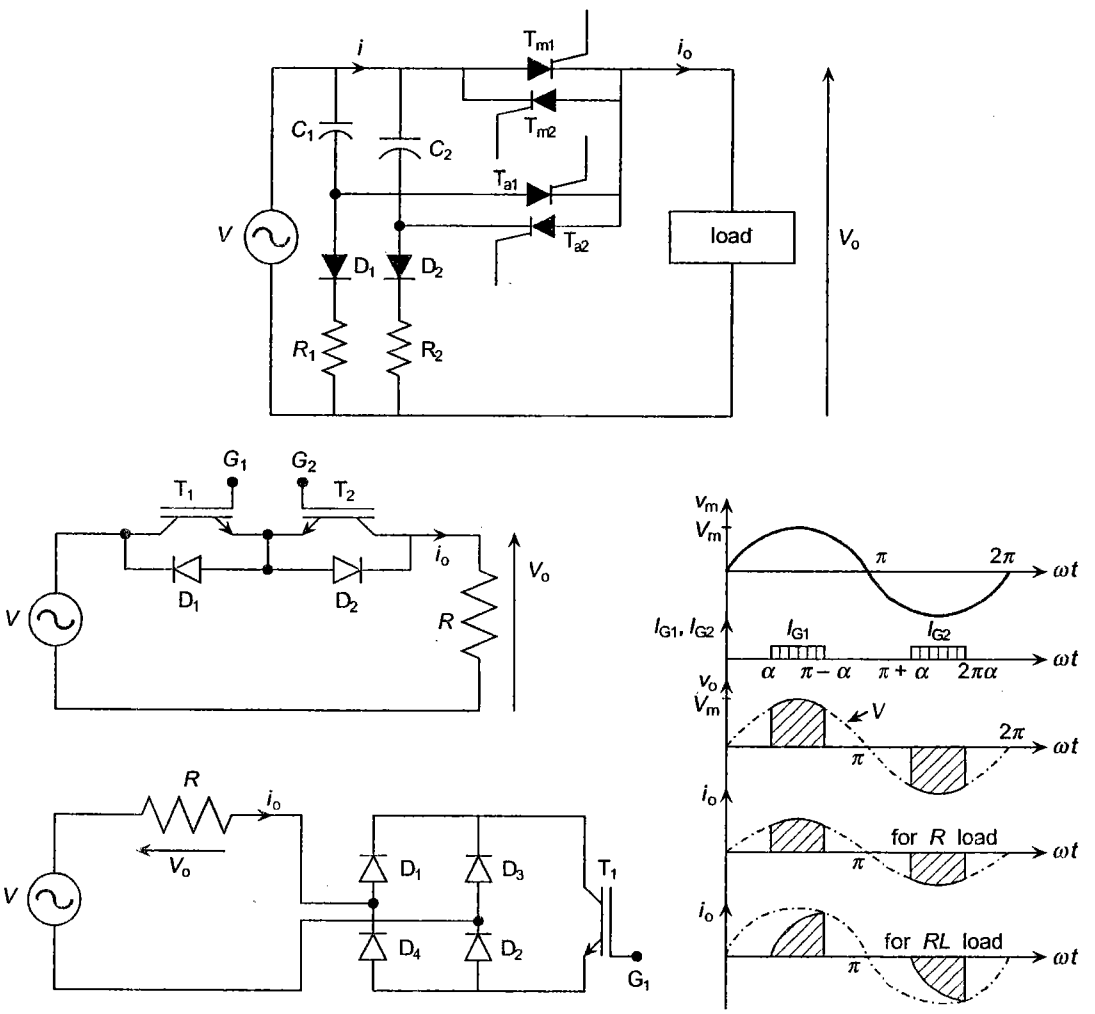


Figure 5.17 AC chopper circuits.

symmetric (with respect to the peak voltage), the device or switch should open at $\omega t = \pi - \alpha$ and $2\pi - \alpha$. Therefore, gate-commutation devices should snap the load current, which has sufficiently high magnitude at these instants. The rms value of the output voltage is given by

$$V_o = \left[\frac{1}{\pi}\int_{\alpha}^{\pi-\alpha} (\sqrt{2}\,V \sin \omega t)^2\, d(\omega t)\right]$$

$$= V\left\{\frac{1}{\pi}\left[(\pi - 2\alpha) + \sin 2\alpha\right]\right\}^{1/2} \tag{5.86}$$

The fundamental component (rms) of the output voltage (V_{o1}) can be found as

$$a_1 = \frac{2}{\pi}\int_{\alpha}^{2\pi-\alpha} \sqrt{2}\,V \sin \omega t \cos \omega t\, d(\omega t)$$

$$= \frac{\sqrt{2}\,V}{\pi}\left[\frac{1}{2}\cos 2\omega t\right]_{\alpha}^{\pi-\alpha} = 0$$

$$b_1 = \frac{2}{\pi}\int_{\alpha}^{2\pi-\alpha} \sqrt{2}\,V \sin \omega t \sin \omega t\, d(\omega t)$$

$$= \frac{\sqrt{2}\,V}{\pi}\left[\omega t - \frac{1}{2}\sin 2\omega t\right]_{\alpha}^{\pi-\alpha}$$

$$= \frac{\sqrt{2}\,V}{\pi}\left[(\pi - 2\alpha) + \sin 2\alpha\right] \tag{5.87}$$

Then

$$V_{o1} = \sqrt{\frac{a_1^2 + b_1^2}{2}} = V\left\{\frac{1}{\pi}\left[(\pi - 2\alpha) + \sin 2\alpha\right]\right\}^{1/2} \tag{5.88}$$

For a resistive load, $i_o = V_o/R$. The rms value of the input line current and its fundamental are given by

$$I = I_o = \frac{V_o}{R} \quad \text{and} \quad I_1 = \frac{V_{o1}}{R} \tag{5.89}$$

Therefore, THD can be found from these values. Also, the power factor of the resistive load (as given in 5.12), i.e.

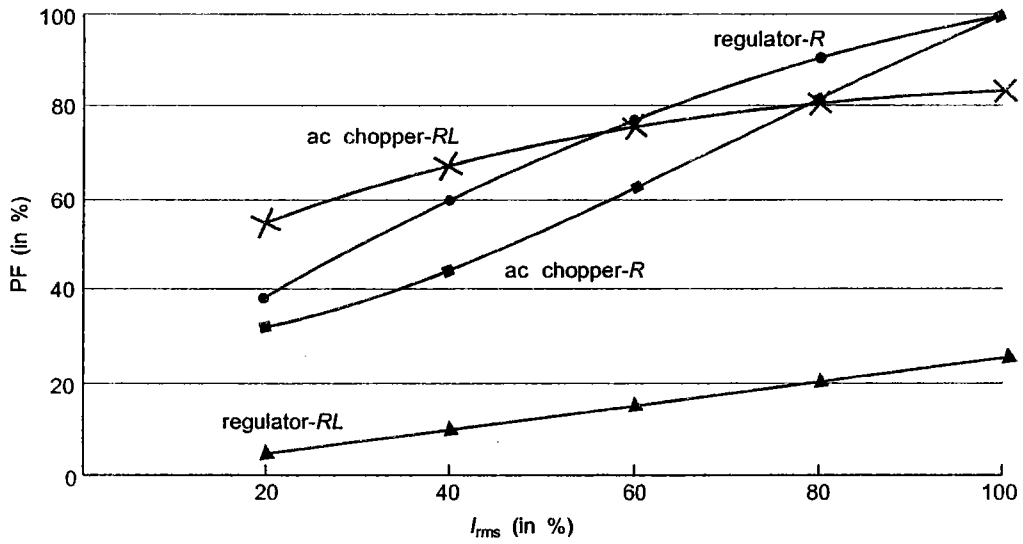
$$\text{PF} = \frac{V_o}{V} = \left\{\frac{1}{\pi}\left[(\pi - 2\alpha) + \sin 2\alpha\right]\right\}^{1/2} \tag{5.90}$$

For an *RL* load, the current response is given by

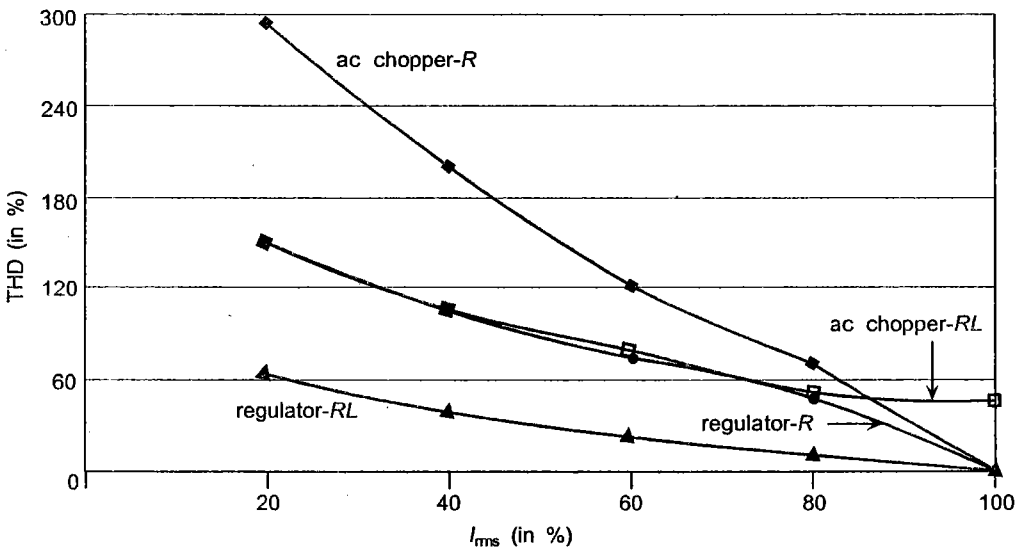
$$i_o(\omega t) = \frac{V}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)\exp\frac{\alpha - \omega t}{\tan \phi}\right], \qquad \text{for } \alpha \le \omega t \le \pi - \alpha$$

This expression may be used to find out THD, DPF, etc., as discussed earlier. In case of phase control switching based ac regulators, the input power factor is always lagging for the resistive

load. However, in this case, the fundamental or displacement power factor (DPF) is always unity due to symmetric waveform. Due to nearly square shape of voltage/current, THD increases significantly for resistive or high power-factor (low ϕ) loads. Figure 5.18 shows the relative performance of ac choppers with respect to ac regulators, for purely resistive ($\phi = 0°$) and *RL* load ($\phi = 75°$). It shows the weakness and strength of the ac choppers for different load conditions.



(a) PF of ac regulator and ac chopper with *R* and *RL* ($\phi = 75°$) load



(b) THD of ac regulator and ac chopper with *R* and *RL* ($\phi = 75°$) load

Figure 5.18 Relative performance of ac choppers.

5.12

AC CHOPPER WITH MULTIPLE PWM CONTROL

It has been shown (in case of ac choppers) that a single pulse can be modulated to control the output or the load voltage. However, the load voltage has almost square wave shapes, and therefore, the load voltage and the line current carry higher-order harmonics. If multiple output voltage pulses are used instead of a single pulse, it significantly reduces the harmonics. Figure 5.19 shows the output voltage for *R* and *RL* loads. It is evident for an *RL* load, the line current is very close to the sinusoidal wave shape. The higher-order-harmonics, therefore, reduces drastically. Here, all the switches are gate-commutation devices, viz., MOSFET, IGBT, etc. Gate signals for these switches at G_1, G_2, G_3 and G_4, show the duration of the on-period of each switch. S_1 and S_2 are operated (on and off) during the positive half-cycle. During the negative half-cycle, S_3 and S_4 are operated. During the intermittent period within a positive half-cycle when S_1 is open, S_2 conducts and a free-wheeling current flows through the inductive or *RL* load. Similarly, S_4 conducts for freewheeling current during negative half-cycle.

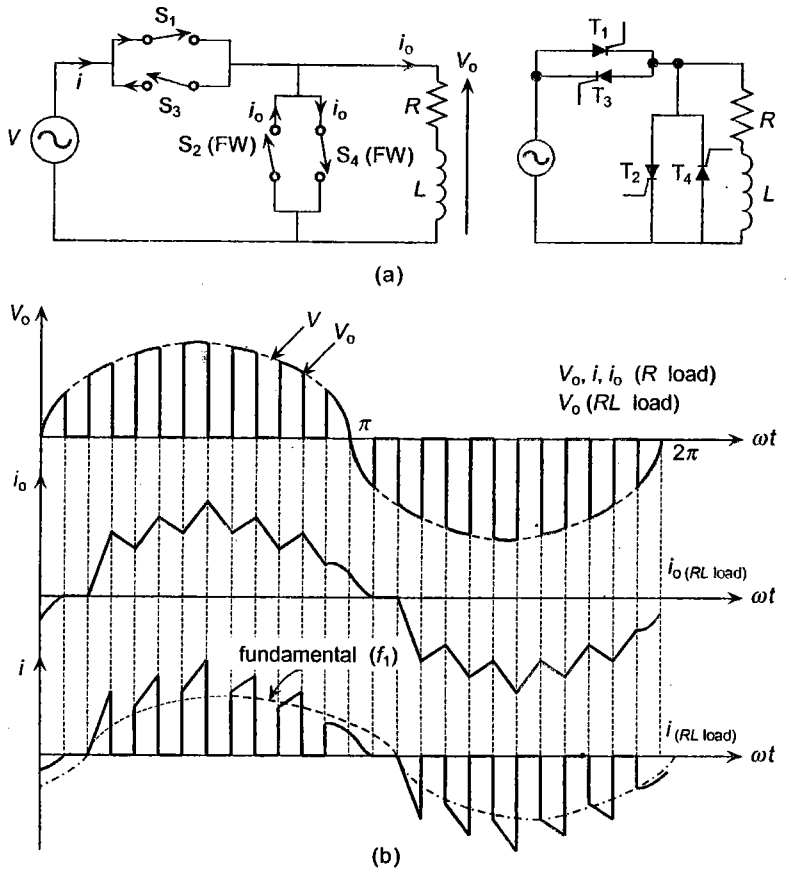


Figure 5.19 Output voltage and current of ac choppers with PWM control.

5.13

CYCLOCONVERTERS

AC voltage regulators control the magnitude of output ac voltage but at the same frequency of the supply voltage. To control the output voltage at adjustable (lower) frequency, cycloconverters are used. It is a direct frequency-changer (ac-to-ac conversion). Here frequency-change is in steps. Normally, cycloconverters are thyristor (SCR) based very high power (up to several MW) converters with line or natural commutation of thyristors. The triggering or switching controller circuits are not simple because a large number of SCR (4 or 8 for single phase and 36 for three phase) are used. Therefore, a microprocessor, microcomputer or digital-single processor (DSP) based triggering controller circuit is used. Normally, it is used for (i) very high-power (MW range), low-speed, ac motors and (ii) low-frequency (50 Hz to $16\frac{2}{3}$ Hz), three-phase to single-phase, traction ac power supply (e.g. used in Germany and central Europe). It is also used as variable-speed constant frequency generator system for aircraft applications, where the speed of prime mover (jet/gas turbine) changes drastically. Moreover, to reduce harmonic contents and to improve efficiency and PF of the converter, gate-commutation devices based cycloconverters are also used for certain applications. Sometimes, an ac voltage is converted into dc (using rectifiers) and a high-frequency ac voltage is generated (using dc-to-ac inverter or resonant constant-frequency dc-link converter). Then a cycloconverter is used to control the output frequency. If the frequency of the output voltage is higher than that of the input voltage ac frequency, it is called a *step-up* cycloconverter. If phase-controlled switching is also applied, the cycloconverter can provide an adjustable-voltage, adjustable-frequency power supply, that is suitable for driving large ac machines.

5.13.1 Single-phase Cycloconverters

A single-phase-to-single-phase cycloconverter is rarely used in practice. However, the fundamental principle of a cycloconverter can be explained with the help of it (Fig. 5.20). It consists of two ac-to-dc converters (or two ac regulators) connected such that the desired positive and negative output voltages can be obtained. It is evident from Fig. 5.21, by controlling the switching of T_1 and T_2, the time period of the positive half-wave of the output voltage ($\tau_0/2$) can be controlled. Similarly, by controlling the switching of T_3 and T_4, the time-period of the negative half-wave can

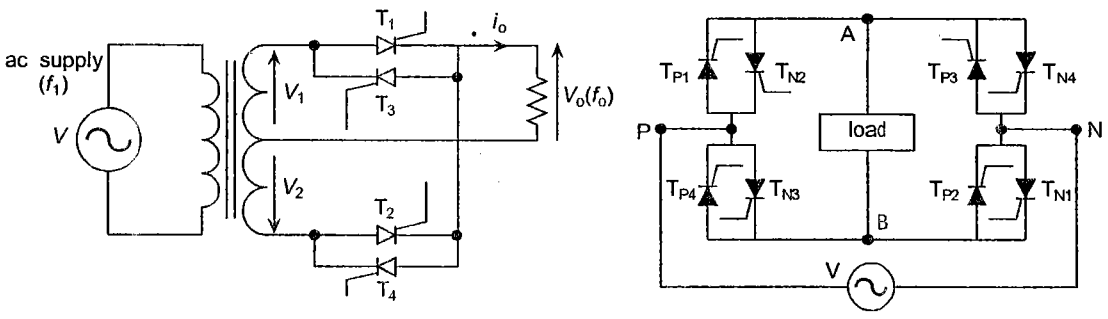


Figure 5.20 Single-phase cycloconverters.

be controlled (Fig. 5.21). Thus, by controlling the integral number of half-cycles, the period (τ_o) hence the frequency of the output voltage (f_o) can be controlled. The frequency of the fundamental of the output voltage can be easily reduced in steps (i.e. 1/2, 1/3, 1/4 and so on). Here, f_i and τ_i are the frequency and the time-period of the input voltage, respectively.

Figure 5.20 shows another single-phase, cycloconverter without using a transformer. The performance of this circuit is same as the previous one. Here, four ac regulators are used at a time two thyristors conduct. For the positive half-period ($\tau_o/2$) of the output voltage (v_o), thyristor pairs T_{P1}–T_{P2} and T_{P3}–T_{P4} conduct during the positive half-cycles and the negative half-cycles of the supply voltage, respectively. During this period, A remains positive. T_{P1}, T_{P2}, T_{P3} and T_{P4} are called positive group of thyristors. Similarly, T_{N1}, T_{N2}, T_{N3} and T_{N4} are called *negative group* of thyristors. It will be seen later, in fact, these thyristors form two ac-to-dc converter bridges. The output voltage waveform, in this case, is no more sinusoidal rather it has about square shape with a high THD (Fig. 5.22a). The wave shape can be improved, if phase control switching is also incorporated, as shown in Figs. 5.22b and c. The switching angle is kept constant (Fig. 5.22b) as well as it is adjusted in each cycle (Fig 5.22c) for better wave-shaping and performance. For this type of cycloconverters, both voltage and frequency are adjustable, independently.

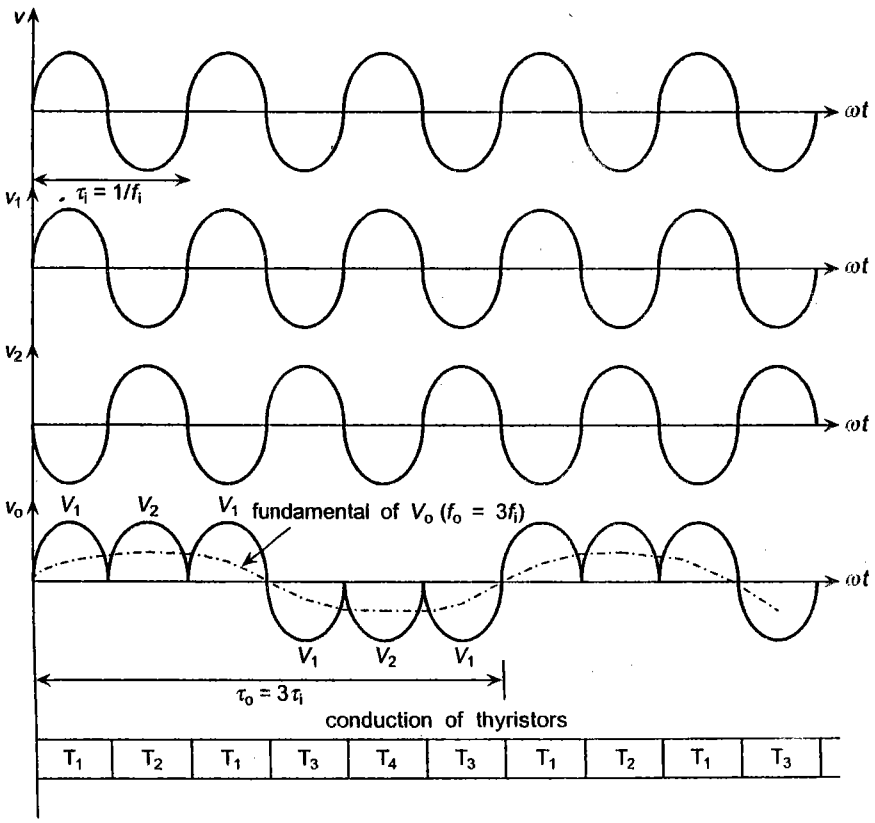


Figure 5.21 Waveforms of single-phase cycloconverter.

For a constant value of α (Fig. 5.22b), the rms value of the output voltage is same as in case of ac regulator for a resistive load (as given in equation 5.8). The rms value of the current is, therefore, V_o/R. However, for an inductive RL load, due to the variation of f_o, even for the same α, the load current is frequency dependent.

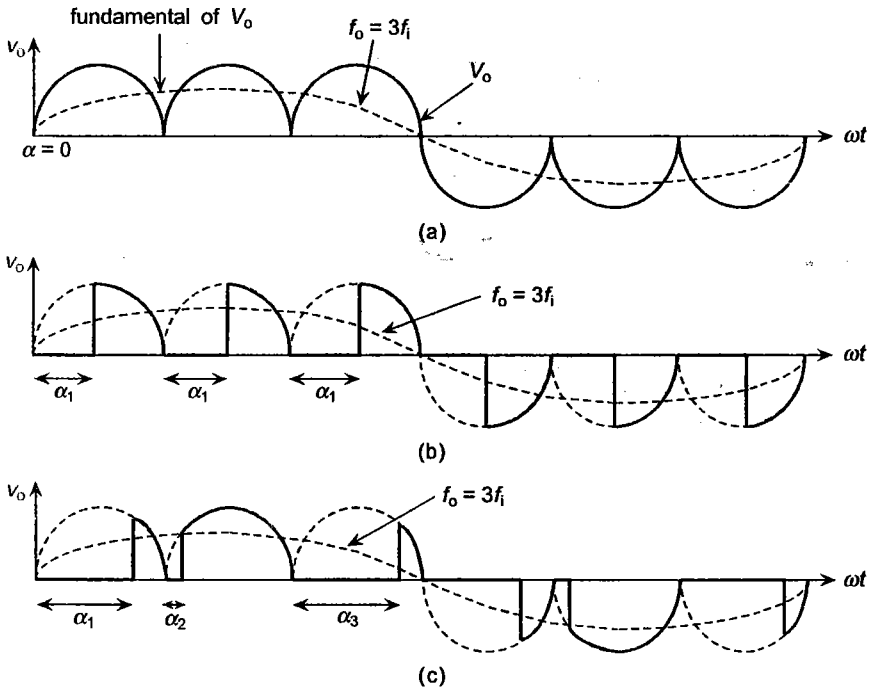


Figure 5.22 Waveforms of the output voltage of cycloconverters: (a) without phase control and with phase control (b) constant α and (c) adjustable α.

5.13.2 THREE-PHASE-TO-SINGLE-PHASE CYCLOCONVERTERS

It consists of two groups of thyristors namely, positive group and negative group. There are three thyristors of each group connected to each phase, as shown Fig. 5.23. It is a three-phase, half-wave cycloconverter. The positive half-period of the load or output voltage can be controlled by keeping conduction of either T_1, T_2 or T_3. Each thyristor can conduct for one-third period (120°) of the input voltage for which its anode voltage (phase voltage) will be higher than the rest of the phase voltage. Similarly, the negative half-period is maintained by the conduction control of T_4, T_5 and T_6. If phase-control is also applied, a fine voltage control becomes possible. The thyristors are triggered at such angles so that the fundamental of the output current (or voltage for resistive load) becomes nearly sinusoidal. The output voltage of a cycloconverter depends upon the segments of its input voltage (combination of half-cycles of the input voltage). The delay angles (α) are varied in each half-cycle (Fig. 5.22c), to achieve the average value of the segment being close to the variation of the reference or desired sinusoidal output voltage. In this way, the harmonics of the output voltage minimize. The delay angles are generated by comparing a cosine control signal at input or source frequency with a sinusoidal reference voltage at the output

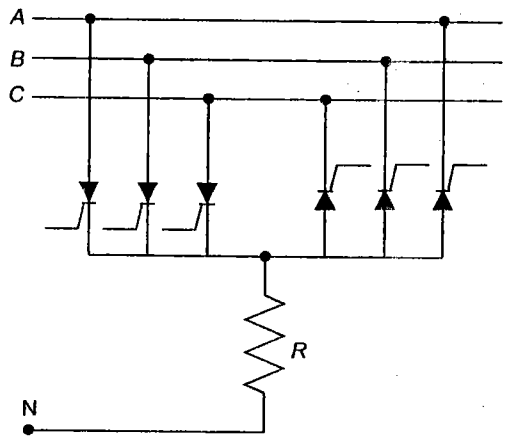


Figure 5.23 Three-phase-to-single-phase cycloconverter.

frequency, f_o. Therefore, the maximum average value of segment is equal to the peak value of the output voltage. It is the output voltage of a three-phase ac-to-dc converter for *RL* load. The maximum output voltage and the maximum average dc voltage become the same, which is given by

$$V_{o(max)} = V_{o(avg)} = \frac{3\sqrt{6}}{2\pi} V \cos \alpha \tag{5.91}$$

where V is rms value of the phase voltage.

5.13.3 Three-phase Cycloconverters

If there is a three-phase load, the arrangement shown in Fig. 5.23 can be repeated for the remaining two-phase loads. Thus, instead of six, eighteen thyristors are required, as shown in Fig. 5.24. Both adjustable and constant value of α can be employed to control the output voltage. Similarly, for a full-bridge type, three-phase cycloconverter, six such bridge circuits as shown in Fig. 5.24 are used. Therefore, in this circuit configuration, thirty-six thyristors (SCR) are required.

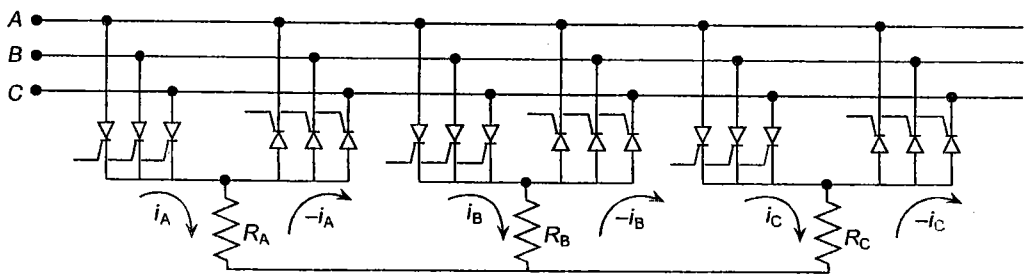


Figure 5.24 Three-phase cycloconverter.

5.14

DISCONTINUOUS PHASE-CONTROLLED SWITCHING*

A phase controlled switching (PCS) is extensively used for an adjustable ac-to-ac, and ac-to-dc power conversion. In case of heat controllers with a resistive load (R), phase-control circuits cause higher-order harmonics, generate radio-frequency interference (RFI) and heavy in-rush currents while switching-on from cold. At large power levels, to minimize RFI, bulky and expensive line-filters are required. When α varies between 60° and 120°, the supply voltage is close to its peak value (86.7% to 100% of V_m). The corresponding output voltage (V_o) control-range is from 89.7% to 44.2%. Therefore, at the switching instant ($\omega t = \alpha$), the line current jumps from zero to almost its peak value. Thus di/dt is high for wide range of control of α. Moreover, there is a heavy in-rush current when a furnace resistance-element (R) is heated from cold because at this condition, the resistance of the element is very low (due to high temperature-coefficient of resistance). At lower value of V_o, PF is also low and THD is significantly high, as shown earlier in Fig. 5.7. Alternately, a zero-voltage switching (ZVS) method is employed to reduce di/dt, where α is kept zero and the voltage control is accomplished by integral-cycle control (ICC) method. However, in addition to step control of V_o, PF also decreases proportionately to V_o. On increasing the total number of cycles ($n + m$), the resolution can be increased but at the cost of large fluctuations in the output voltage. A step voltage control, low PF and introduction of sub-synchronous harmonics are main drawbacks of ICC method. While, in case of phase-controlled switching of ac regulators, THD is high and PF is low for lower output voltage. By combination of both above-mentioned methods, a new technique, named as *discontinuous phase-controlled switching*, was introduced. In this method, the drawbacks of integral-cycle control and phase-controlled switching techniques are removed. Both step and fine voltage variations are achieved by the former and the latter methods, respectively. The load resistance is replaced by equivalent several resistances connected in parallel. In this case, sub-synchronous harmonics are eliminated completely, higher-order harmonics and THD are reduced significantly and PF is brought close to unity.

To remove the above-mentioned defects of phase-control, here switching is done in discontinuous manner. Then, both step and fine type of control of V_o are possible. If, both ICC and PCS techniques are applied together for ac power control, the rms value of the output voltage is given by

$$V_o = \left[\frac{k}{\pi}\int_{\alpha}^{\pi} (\sqrt{2}\,V \sin \omega t)^2\, d(\omega t)\right]^{1/2} \tag{5.92}$$

or

$$V_o = \left[\frac{k}{\pi}\int_{\alpha}^{\pi} (V_m \sin \omega t)^2 d(\omega t)\right]^{1/2} = V\left[\frac{k}{\pi}(\pi - \alpha + \frac{1}{2}\sin 2\alpha)\right]^{1/2} \tag{5.93}$$

For conventional phase control (PCS), off cycle does not exist ($m = 0$ and $k = 1$).
Therefore, for $\alpha = 0$ and $k = 1$, the maximum power (P_{max}) will be supplied to the load such that

*M.S.J. Asghar, 'Fine power control by discontinuous phase-controlled switching', IEEE Transcations on circuits and Systems-I, Vol. 46, No. 3, March 1999, pp. 402–405.

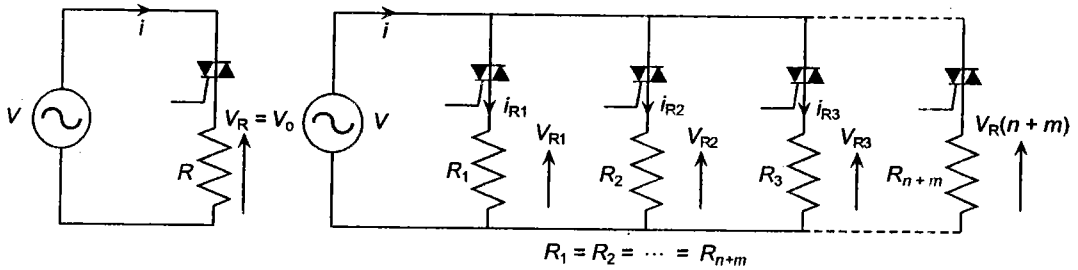
$$P = P_{max} = \frac{V_o^2}{R} = \frac{V^2}{R} \tag{5.94}$$

In case of discontinuous phase-controlled switching, the load resistance (R) is replaced by several branches of R_1 resistance. According to the requirement of resolution of control, R is replaced by $(n + m)$ number of parallel resistances (R_1) as shown in Fig. 5.25, such that

$$R_1 = (n + m)\, R \tag{5.95}$$

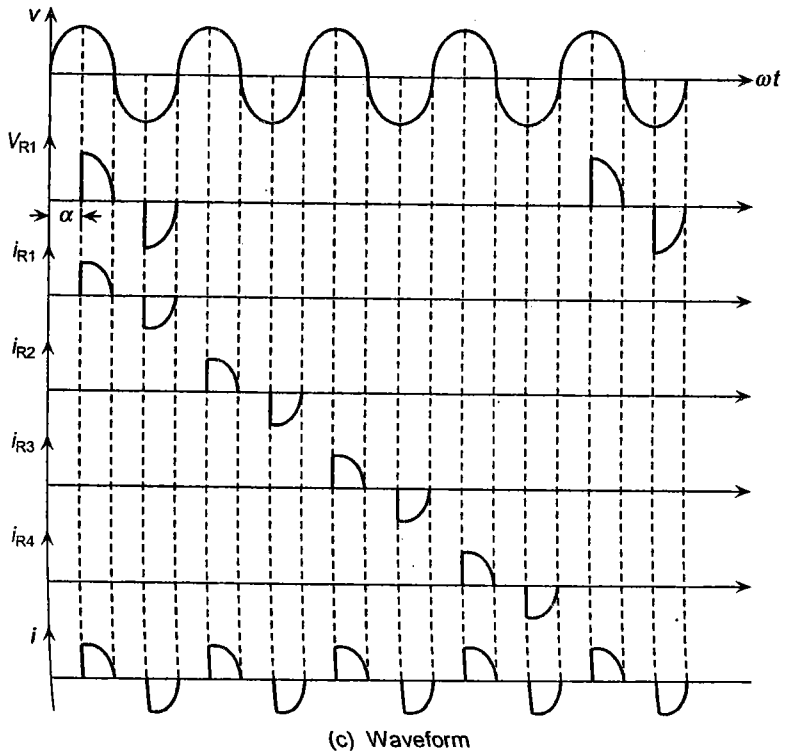
Now, P_{max} corresponds to the condition where all resistances R_1, are switched continuously at $\alpha = 0$. Thus,

$$P_{max} = \frac{(n + m)\, V_o^2}{R_1} = \frac{V^2}{R} \tag{5.96}$$



(a) ac phase control

(b) Discontinuous phase control



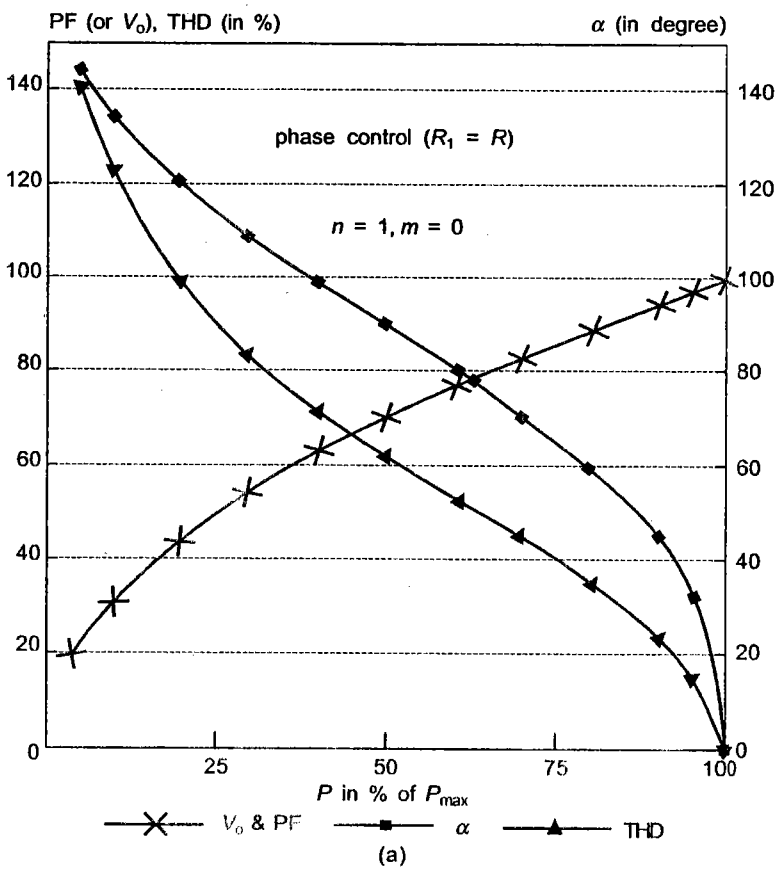
(c) Waveform

Figure 5.25 Discontinuous phase-controller circuit and waveforms for n + m = 4.

Similarly, for minimum output power only one R_1 is switched at a time, sequentially, for one cycle ($n = 1$). Thus, the line current remains same in each cycle. The minimum output power is given by

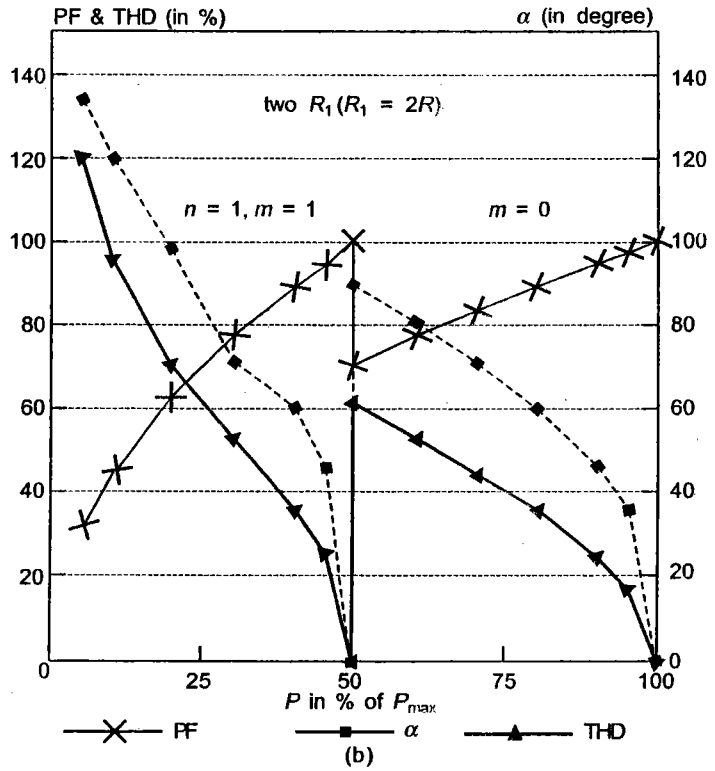
$$P_{min} = \frac{V_o^2}{R_1} = \frac{V^2}{R_1}\left[\frac{k}{\pi}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)\right] \tag{5.97}$$

When $\alpha = 0$ and $k = 1$, $P_{min} = V^2/R_1$ and PF becomes unity. Thus V_o and P can be controlled in steps of $[1/(n + m)]^{1/2}$ and $1/(n + m)$, respectively, at unity PF (without sub-synchronous and higher-order harmonics, therefore, THD becomes zero). Fine variation can also be done by controlling α at a PF close to unity, as shown in Fig. 5.26. In case of single resistor ($R = R_1$), if α is controlled by PCS, to get 50% output power [$P = (1/2)P_{max}$], the PF and THD are 70.7% and 61.7% respectively (Fig. 5.7 and 5.26a). If P is to be reduced further, PF also reduces and THD increases. However, if R is replaced by two R_1 resistors in parallel ($R_1 = 2R$) and both are switched alternately by ICC method, the PF becomes unity and THD becomes zero at $P = (1/2)P_{max}$ (Fig. 5.26b). If fine control (reduction) in P is needed, it can be achieved by controlling α. Therefore, as the number of branches of R_1 is increased, THD as well as RFI reduce drastically and PF improves significantly due to small variation of α, as shown in Figs. 5.26c and d. Thus, P can be controlled between P_{max} and P_{min} effectively.

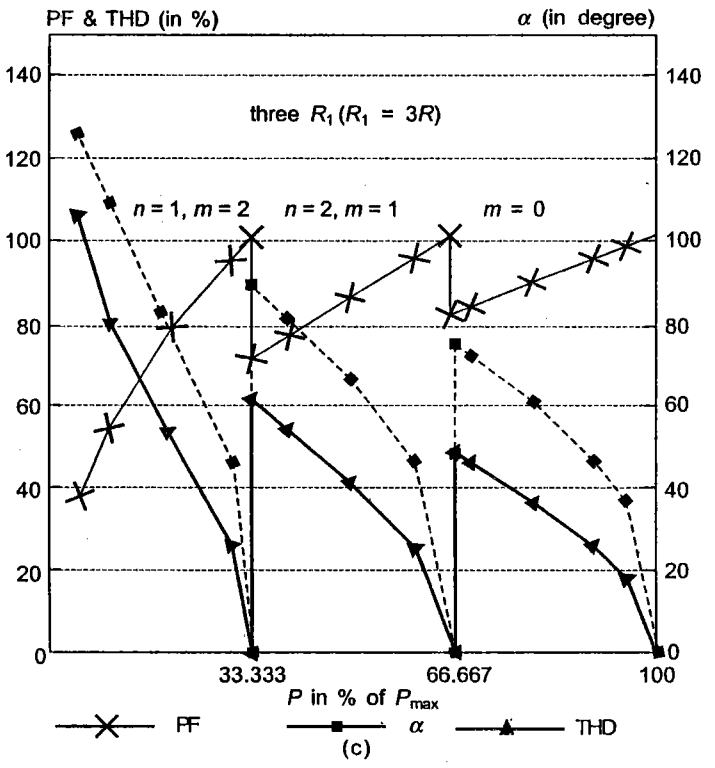


(a)

Figure 5.26 (*Cont.*)



(b)



(c)

Figure 5.26 (*Cont.*)

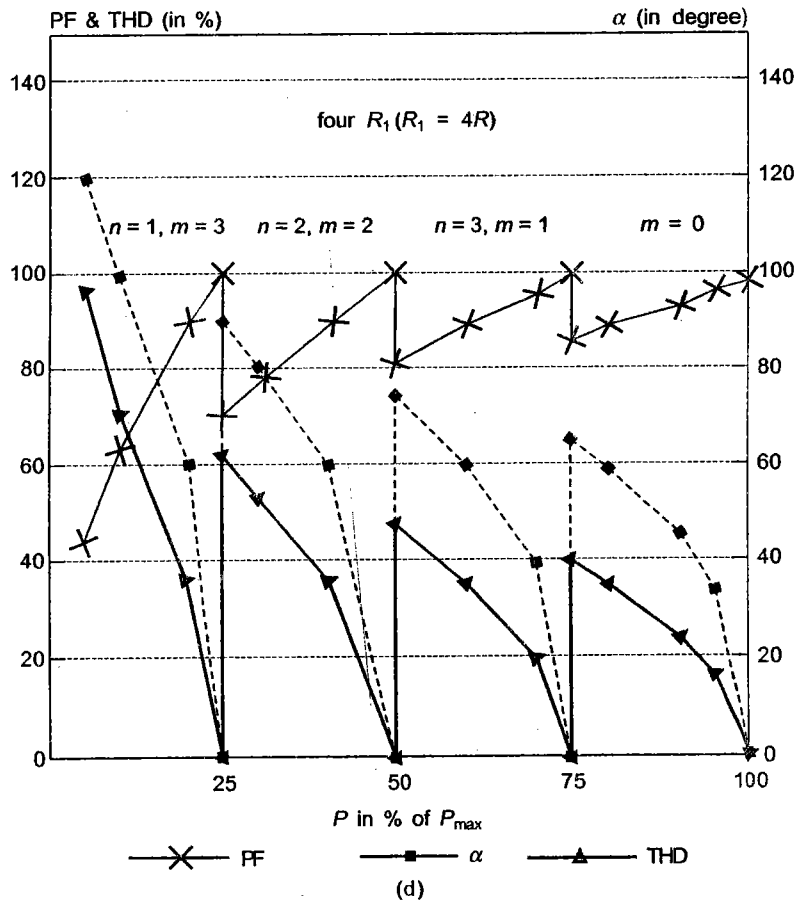


Figure 5.26 Variation of PF, α and THD with respect to output power, P: (a) Conventional phase control; discontinuous phase-control (DPC) with different number of parallel load resistances, (b) 2 R, (c) 3 R and (d) 4 R.

SUMMARY

There are several methods by which the output ac voltage can be controlled from a fixed frequency, fixed ac voltage source. AC voltage controllers or regulators control the output voltage (magnitude only) from a fixed voltage ac source. The voltage magnitude is controlled using ac phase-controlled switching. These ac controllers are compact, light in weight and cheaper in comparison to the conventional methods (e.g. using autotransformers or tape-changing transformers). However, due to non-sinusoidal output voltage waveforms, these ac controllers introduce harmonics in the line current and reduces the effective PF of the load. The integral-cycle control (ICC) method was used earlier to control for the same applications. However, due to introduction of sub-synchronous (low frequency) harmonics in the line, it was abandoned.

Alternately, ac choppers and electronic tap-changers arrangements are also used. However, they have limited applications due to the requirements of forced-commutation circuits and tap-changing transformers for the former and the latter methods, respectively. Cycloconverters are also used for very high power applications. In this case, both voltage (magnitude) and frequency are controllable. Although a fine voltage control is possible, using phase-controlled switching, but frequency control (reduction) is possible in steps only.

A discontinuous-phase controlled technique is recently introduced to eliminate drawbacks of both integral-cycle control and phase controlled switching. In this case, both high PF and low distortion (THD) are obtained in comparison to ac regulators. However, in this case, more thyristors are needed and load impedance requires modifications.

REVIEW QUESTIONS

1. In what respect the performance of an ac regulator is better than the conventional ac voltage controllers?
2. What are merits and demerits of integral-cycle switching?
3. Find the power factor and the rms value of output voltage of a 230-V, single-phase ac regulator with a resistive load at $\alpha = 60°$.
4. For a resistive load of an ac regulator, find the condition when THD of the line current is 100%.
5. Find the extinction angle β and the rms value of the output voltage for an RL load when thyristors are trigged at 120°. The load power-factor angle, $\phi = 45°$.
6. Explain the application of an ac regulator with a purely inductive load.
7. Find the rms value and THD of line current in case of Exampie 5.7, if the capacitive VAR is reduced to a half. (*Hint:* $I_C = 11.5$ A, then find the rms values of I_1 and I, and calculate THD).
8. What are applications of three-phase ac regulators?
9. Why three-phase, three-wire, ac regulators are preferred over three-phase four-wire systems?
10. For a 400-V, 3-phase, 3-wire, Y-connected R loads, find the rms value of the load current through each resistor of 10 Ω. The switching angle $\alpha = 90°$.
11. Find the rms value of the output voltage of a 400-V, 3-phase, delta-connected, R-loads for $\alpha = 90°$. Each load resistor is connected with a pair of SCR in each branch of delta connection.
12. What are merits and demerits of cycloconverters? Why it is not popular?
13. What are merits of the discontinuous-phase controlled switching?

6

Phase-controlled (AC-to-DC) Converters

6.1

INTRODUCTION

There are several conventional methods by which the output dc voltage can be controlled, e.g. a diode bridge with a tap-changing transformer or with an auto-transformer, as shown in Fig. 6.1. Although these methods are simple, but suffer from the demerits due to size, weight and cost of transformers. Previously, this type of control scheme (a diode bridge with tap-changing transformer) was used to control the dc voltage hence speed of dc motors used in electric traction of Indian Railways.

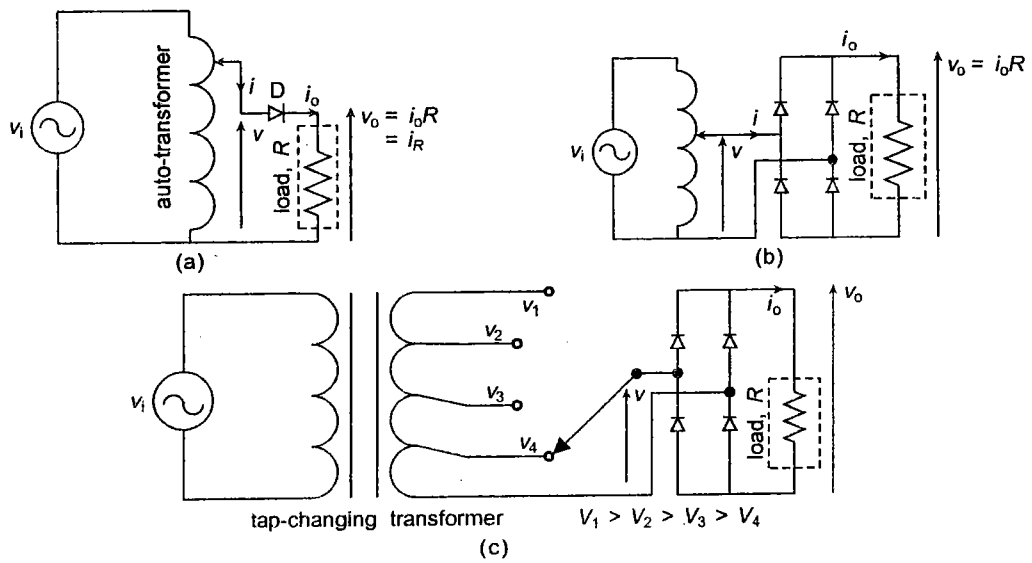


Figure 6.1 Conventional ac-to-dc voltage converters using transformers.

In case of an ac-to-dc phase-controlled switching, the phase controller works as an ordinary contactor switch, as discussed in Section 5.2. For a certain period of time, the switch is closed (on), thus the input supply voltage (v) reaches the load and the output voltage becomes equal to v. Similarly, for a certain period of time, the switch is open (off), thus the input voltage does not reach the load. Thus, instead of the complete input voltage (whole cycle) reaching the load, the switch (phase-controlled converter) slices the input voltage and only its part (or parts) reaches to the load. In this arrangement, no transformer is required. Thus, the size, weight and cost are small and the efficiency is very high. Here, the power semiconductor switching devices (e.g. diodes, SCR, etc.) work as unilateral switch, therefore, the load current flows in one direction only. By proper circuit connections, the output voltage and the current is maintained unidirectional (or dc). In fact, the converter works as a commutator of a dc generator.

6.2 CONVERTER RECTIFIERS

Converter rectifier circuits are used to convert ac power into dc power. The converter circuits employing only diodes are called *uncontrolled* converters. In this case, both conduction and commutation (turn-off) of the switching devices (diodes) depend upon the circuit conditions. The output voltage does not vary for a given load and a given ac supply. Therefore, it is called an uncontrolled converter.

A converter circuit, employing both diodes and thyristors (SCR), is called a *semi* or *half-controlled* converter (or simply semiconverter). An adjustable output voltage (dc or average) is obtained by controlling the switching angle of the thyristors. The controlled output voltage and current are unidirectional and the power flows only in one direction, i.e. from the ac source to the load.

A converter circuit employing only thyristors, is called a *fully-controlled* converter (or full-converter); the output dc voltage is adjustable. However, in this case, the direction of the current remains same but the output dc voltage can be reversed, to allow the power flow from the load to the supply. This process is called *inversion* and the converter operating under this condition is called inverter.

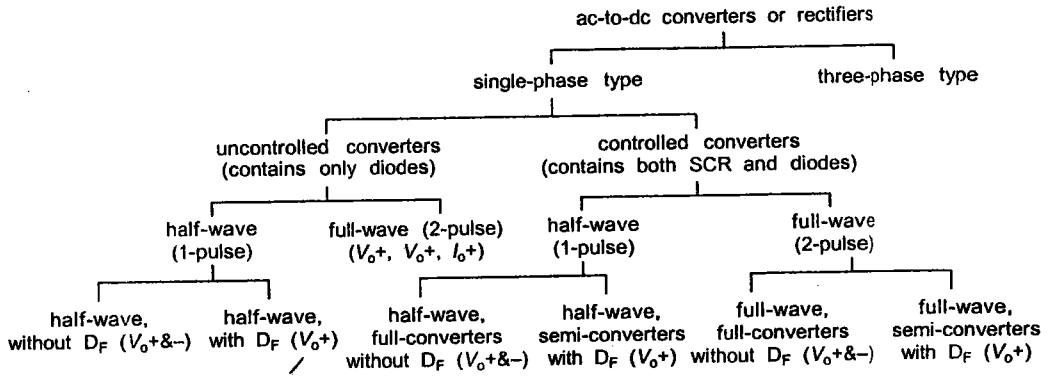
Since the commutation of the thyristors in the above converters depends upon the ac supply, these converters are also called *line* or *naturally-commutated* converters. The direction of flow of the load current remains unidirectional for all the above converters.

Moreover, when either positive or negative half-cycle voltage (uncontrolled or controlled) applied to the load, it is called a *half-wave* converter. Similarly, when both half-cycles are used, it is called a *full-wave* converter.

Figure 6.2 shows a general classification of ac-to-dc converters for single-phase. However, the same classification is valid for three-phase systems except that the number of pulses is three and six, for half-wave and full-wave configurations, respectively.

6.3 UNCONTROLLED CONVERTERS

Semiconductor diodes are widely used in ac-to-dc converter circuits. However, the output average (or dc) voltage is not adjustable (rather constant), depending upon input ac voltage and the load-



Note: V is instataneous value of the output voltage and current. + and – indicates both positive and negative values, + indicates only positive values. For all these converters i_o and I_o are positive.

Figure 6.2 Classification of converters.

circuit parameters. It will be seen later that both output voltage and load current depend upon the load impedance (magnitude as well as type, e.g. *R*, *RL*, *RC*, *RLC*, etc.). It contains only diodes. Thus, whenever diodes are in forward-biased condition, they conduct. However, the commutation (turn-off) depends only upon the nature of the circuit. When the current through diode ceases, commutation takes place. Various types of single-phase, uncontrolled converters are discussed in the following sections.

6.3.1 Half-wave, Uncontrolled Converters

Half-wave, single-pulse, rectifier circuit is a most simple ac-to-dc converter with a fixed output voltage. Semiconductor diode conducts whenever it is in forward-bias condition (acts as a closed switch). The conduction ceases (opening of the switch), only when the current through it becomes almost zero irrespective of that whether the supply voltage at the anode is positive or negative. When a diode or other power semiconductor device (e.g. SCR) conducts, it is flooded with carriers (holes and electrons) and it behave like an ordinary conductor. A turn-off operation or commutation takes place only when the number of carriers becomes very small ($i_A < I_H$ for SCR) and the depletion layer forms again. Figure 6.3a shows a half-wave, uncontrolled converter circuits with a purely resistive load. Here the wave shapes of the output voltage (v_o) and output current (i_o) are same. At $\omega t = \pi$, the input current (i) becomes zero and commutation takes place. Subsequent reverse voltage (during negative half-cycle) keeps the diode in reverse bias or blocking state.

Figure 6.3b shows various waveforms for an *RL* load. The load inductor (*L*) stores energy in the initial part of positive half-cycle of the applied voltage and maintains conduction of current during the negative half-cycle by releasing the stored energy for a substantial period. The stretched conduction period of current (i) depends upon the value of *L*. During the conduction period, the diode (or any power semiconductor device) behaves as an ordinary mechanical contactor switch. Thus, whatever supply voltage is there, the same appears at the load circuit (except the small voltage drop across the device, which is normally neglected). The output voltage is sum of voltage across resistor (v_R) and the voltage across inductor (v_L). Since an inductor is an energy storing element and the energy stored over a cycle is zero (average of $v_L \times i$), the energy stored and the energy released are equal. At the peak of i or v_R, $\omega t = \nu$, the slope of current (di/dt) is zero and thereafter it becomes negative, as shown in Fig. 6.3b. The supply voltage appears across the diode during the blocking

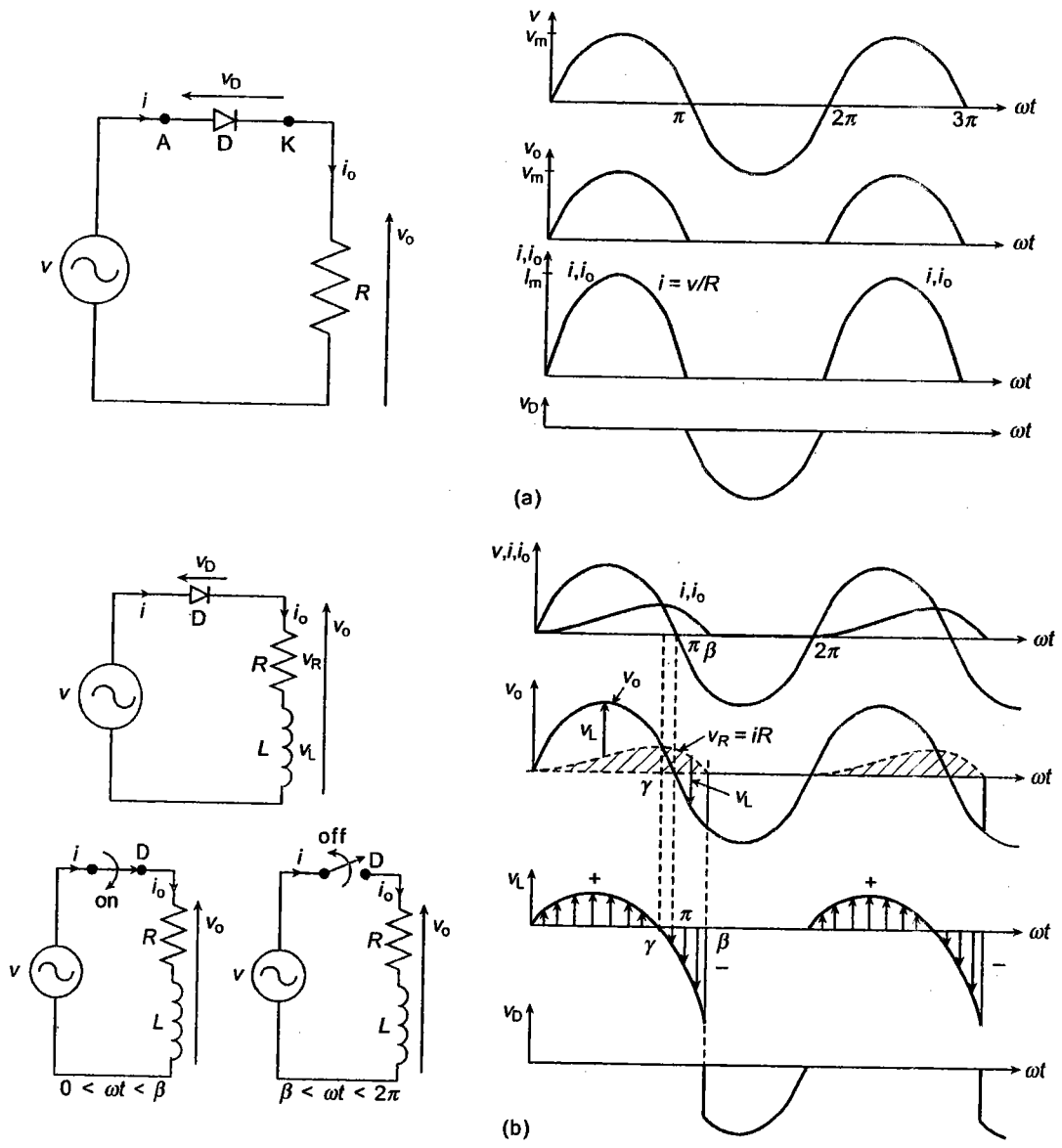


Figure 6.3 Half-wave circuits with (a) R and (b) RL loads.

period (β to 2π). At $\omega t = \pi$, since D is conducting with a significantly high magnitude of the current, it does not commutate (turn-off). Because it is flooded with carriers (electron-hole pairs) and the depletion layer does not form across the pn junction of the diode. Moreover, the inductor provides a negative voltage at the cathode of diode, which is more negative than anode. Thus, the conduction of device continues even after the input supply voltage (v) becomes negative. It behaves as a closed contactor-switch and the negative input voltage reaches the load. The conduction of the diode continues till the current through it reduces to ideally zero level (practically few milli-amperes to

few tens of milli-amperes) and the depletion layer of pn junction forms again with a reverse-biased condition. The current extinction-angle (β) depends upon the nature of the load impedance, as shown in Fig. 5.7, for an RL load (here $\alpha = 0$).

The diode acts as an ordinary switch during the period of conduction and thus even negative voltage reaches the load. The diode conducts up to the current extinction angle (β). The voltage equation of the circuit during the conduction period of the diode is given by

$$L\frac{di(\omega t)}{dt} + Ri(\omega t) = V_m \sin \omega t, \qquad 0 \le \omega t \le \beta \tag{6.1}$$

where $V_m = \sqrt{2}\, V$. Thus, the input or line current (i), as well as the output current (i_o), are given by

$$i_o(\omega t) = i(\omega t) = \frac{V_m}{Z}\left[\sin(\omega t - \phi) - \sin\phi \exp\left(-\frac{\omega t}{\tan\phi}\right)\right] \tag{6.2}$$

where

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) \quad \text{and} \quad Z = [R^2 + (\omega L)^2]^{1/2}$$

The voltage drop across the inductor becomes zero at $v_o = v = v_R$ (when the slope of the current, di/dt, hence, v_L becomes zero). Thereafter, the slope (hence v_L) becomes negative. Thus inductor returns the previously stored energy to the source.

6.3.2 Half-wave, Uncontrolled Converters with A Freewheeling Diode

In the previous case, the load current (i_o) was discontinuous and it was same as the line current (i). If a freewheeling diode is connected across the load, only positive voltage reaches the load. Figure 6.4 shows an *RL* load with a freewheeling diode (D_F). Just after $\omega t = \pi$, due to the conduction of the diode (D), the negative supply voltage appears across the load and at the

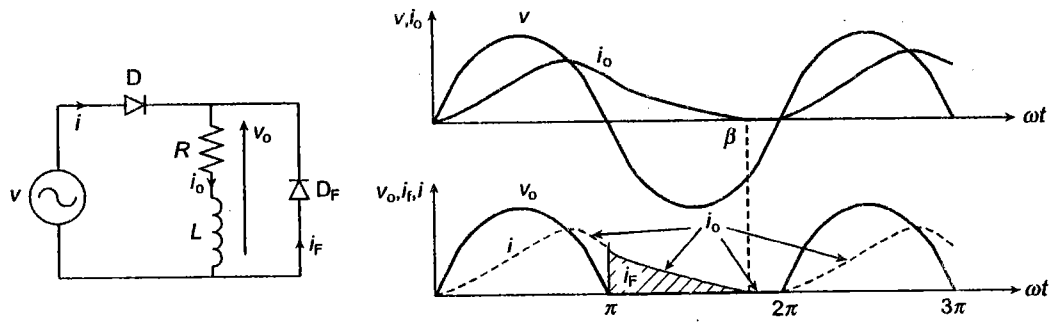


Figure 6.4 Half-wave circuit with freewheeling diode.

cathode of the D_F. It makes D_F to come into conduction because it achieves a forward-bias condition. Now, the load current circulates through a very-low impedance path (practically short circuited) offered by D_F and the current through D ceases. Thus, D immediately comes into blocking mode (commutation accomplishes). Contrary to the previous case, the line current ceases

to flow at $\omega t = \pi$. However, the load current (i_o) keeps on flowing through D_F. It may be continuous or discontinuous that depends upon value of β, which in turn depends upon L. Although the output voltage is same as in case of a resistive load but the load current flows up to β which depend upon ϕ. Moreover, the load or output voltage never goes to its negative excursion. The average (dc) values of the output voltage and current are given by

$$V_o = \frac{1}{2\pi}\int_0^{\beta} V_m(\sin \omega t)\, d(\omega t)$$

$$= \frac{V_m}{2\pi}(1 - \cos\beta) \tag{6.3}$$

and

$$I_o = \frac{V_o}{R} \tag{6.4}$$

The value of β varies from π to 2π for $\phi = 0$ (purely resistive), to $\phi = \pi/2$ (purely inductive) circuits, respectively.

6.3.3 Half-wave, Uncontrolled Converters with *RC* Loads

In this case, during a small portion (half part) of the positive half-cycle, the input current flows through the diode, i.e. when the source or input voltage is higher than the capacitor voltage (Fig. 6.5). The load current may be continuous or discontinuous that depends upon the high (case I) or low (case II) value of RC, respectively.

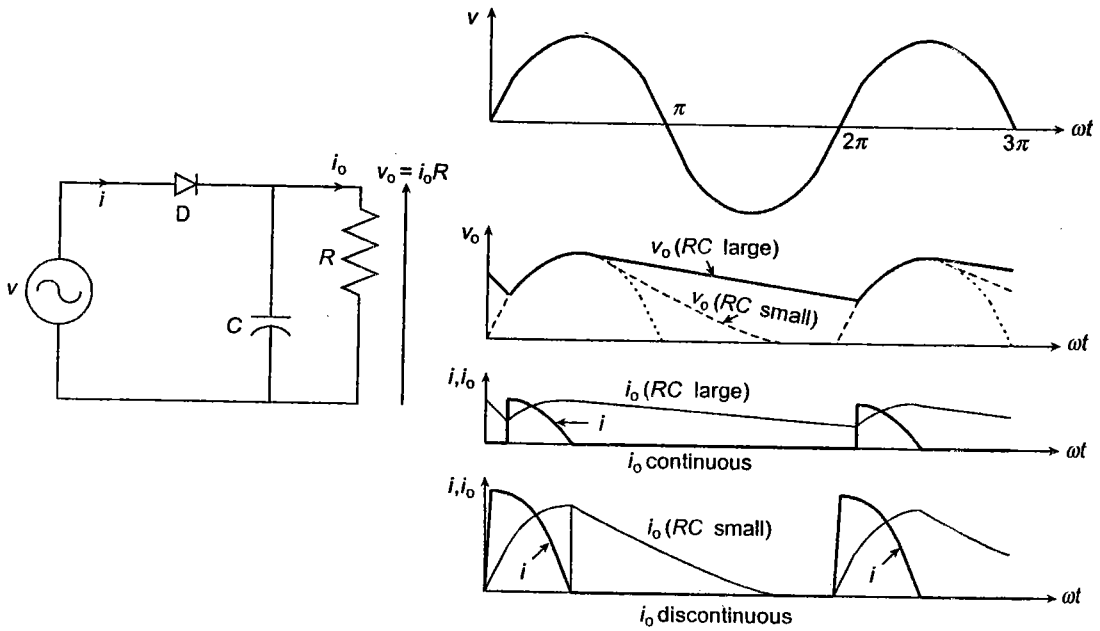
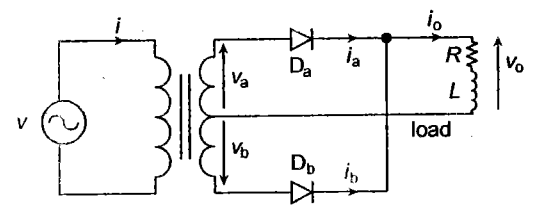


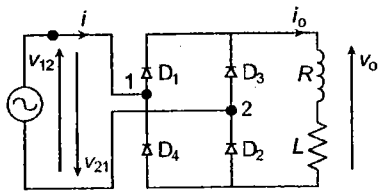
Figure 6.5 A half-wave, uncontrolled rectifier with *RC* loads.

6.3.4 Full-wave, Uncontrolled Converters

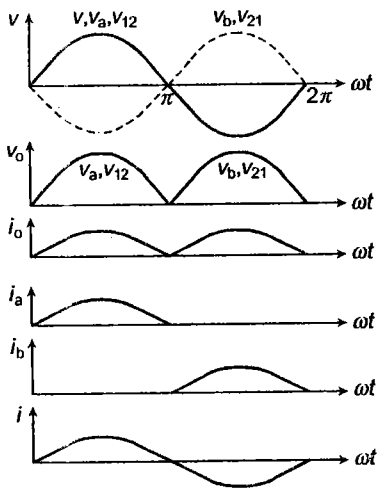
Half-wave, single-pulse, uncontrolled converters, as discussed above, are seldom used in practice. A practical and commonly used uncontrolled converter uses full-wave configurations. Two configurations are possible for this type of converters, as shown in Fig. 6.6. The nature of the load



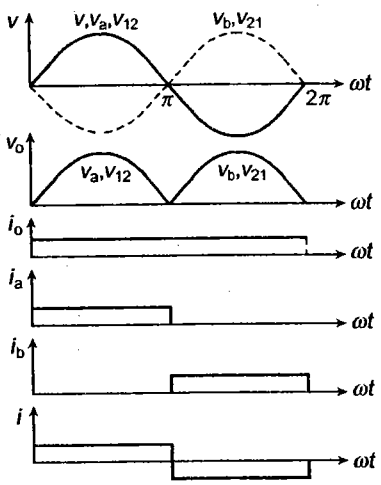
(a) Diodes with transformer



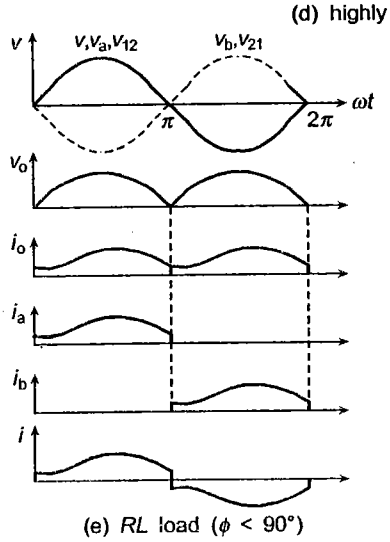
(b) Diode bridge configuration



(c) *R*-load (ϕ = 0)



(d) highly inductive *RL* load ($\phi \cong 90°$)



(e) *RL* load (ϕ < 90°)

Figure 6.6 Full-wave uncontrolled converters with different loads (ϕ).

current and the line current depends upon the nature of the load impedance and ϕ. The load voltage is always positive. The first configuration requires less number of devices but a centre-tapped transformer is necessary. Moreover, the transformer is under-utilized because one part of the secondary winding remains idle for each half-cycle.

For an *R*-load, the current through the diodes ceases to zero at $\omega t = \pi$ and 2π. Therefore, the commutation of D_a and D_b takes place at $\omega t = \pi$ and 2π, respectively. The load or the output voltage has a constant magnitude (sinusoidal half-wave). The expression of the average value of the output voltage is given by

$$V_o = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, d(\omega t) = \frac{2V_m}{\pi} \tag{6.5}$$

For an *RL* load, the average of output voltage and the conduction period of each diode remain same but the wave shape of load current changes and it becomes continuous (non zero). The line current is no more sinusoidal, therefore THD increases.

The diode D_a (or D_1–D_2 pair in bridge configuration) conducts with a current (i_a) between $\omega t = 0$ and π. Similarly, D_b (or D_3–D_4 pair) conducts with a current (i_b) between π and 2π. For an *RL* load, at $\omega t = \pi$, a significant amount of load current flows through D_a and therefore, D_a is flooded with carriers (electron-hole pair). However, just after $\omega t = \pi$, D_a (or D_3–D_4 pair) becomes forward biased hence conducts, and the supply voltage appears across these conducting diodes. Both diodes (which work as switch) are shorting the input supply voltage v_a and v_b. Momentarily, a short-circuit current tries to flow from cathode to anode of D_a. When the magnitude of current becomes almost equal and opposite to i_a, the net current through the device (D_a) becomes zero (ideally). It neutralizes the carriers inside the diode (D_a) and therefore commutation takes place. Moreover, due to the conduction of D_b, v_b reaches (positive voltage) at the cathode of D_a. Since $v_b > v_a$, it reverse biases the diode D_a.

In case of a parallel *RC* load, the load current and the output voltage become continuous or non-zero (as discussed in Section 6.3.3). Here the line current flows in the first-half part of each half-cycle.

Example 6.1 The input ac voltage of a half-wave, uncontrolled converter is 100 V. Show that for different *RL* loads, the average or dc output voltage of converter is load dependent.

Solution The expression of the output dc voltage for an *RL* load is given by

$$V_o = \frac{V_m}{2\pi}(1 - \cos\beta) = \frac{\sqrt{2}\,100}{2\pi}(1 - \cos\beta) = 22.5(1 - \cos\beta)$$

It is evident from Fig. 5.7, β varies for different values of ϕ. Here for uncontrolled converter, $\alpha = 0$. The computed V_o is shown in the tabular form below.

ϕ	β	V_o
0°	180°	45 V
30°	210.1°	41.96 V
60°	244.3°	32.26 V
90°	360°	0

6.4

CONTROLLED CONVERTERS

In the previous circuits, the average output voltage (V_o) was constant for a given load and the given input or mains voltage (v). If an autotransformer is used, adjustable dc output voltage can be obtained by varying the input ac voltage. However, this involves a costly and bulky autotransformer. Alternatively, the diodes in the previous circuits (Figs. 6.2 to 6.6), can be replaced by thyristors. Now, V_o can be controlled by the delay or switching angle (α). Thus, an adjustable output dc voltage can be obtained. There are several configurations of such circuits. They are half-wave or 1-pulse type (when control is done in the half-cycle only) and full-wave or 2-pulse type (when control is done in both the half-cycles). They supply positive average output voltage (half or semi-converters) as well as both positive and negative average output voltage (full converters). A full-wave, two-pulse, full-converter is also called a *full-wave, fully-controlled* converter. It may operate in the first as well as in the fourth quadrant of the output v_o–i_o characteristics plane. However, it operates in the fourth quadrant only for an active *R-L-E* load (e.g. forward braking of dc motor) or for *R-L-E* (negative) load in inversion or dc-to-ac mode (e.g. from dc source). While the semi or half-converters operate in the first quadrant only.

6.4.1 Half-wave, Fully-controlled Converters

This converter is an extension of half-wave, single-pulse, uncontrolled converters. For a resistive load, the conduction starts at $\omega t = \alpha$, and commutation takes place at $\omega t = \pi$ (Fig. 6.7a). The average value of the output voltage is always positive. The converter operates in the first quadrant of v_o–i_o characteristics only. The average value of v_o is given by

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t \, d(\omega t)$$

$$= \frac{V_m}{2\pi}(1 + \cos\alpha) \tag{6.6}$$

For the resistive load, the load current, $i_o = v_o/R$ and its average value, $I_o = V_o/R$. Figure 6.7b shows the converter with an *RL* load. Here, the thyristor (SCR) remains in conduction state even after $\omega t = \pi$, and finally commutates at β. During the conduction period of the SCR, the voltage equation is given by

$$L\frac{di}{dt} + Ri = V_m \sin\omega t, \qquad \alpha \le \omega t \le \beta \tag{6.7}$$

Thus, the input or line current (i) as well as the load current (i) for an *RL* load is given by

$$i_o = \frac{V_m}{Z}\left[\sin(\omega t - \phi) + \sin(\alpha - \phi)\exp\frac{\alpha - \omega t}{\tan\phi}\right], \qquad \alpha \le \omega t \le \beta \tag{6.8}$$

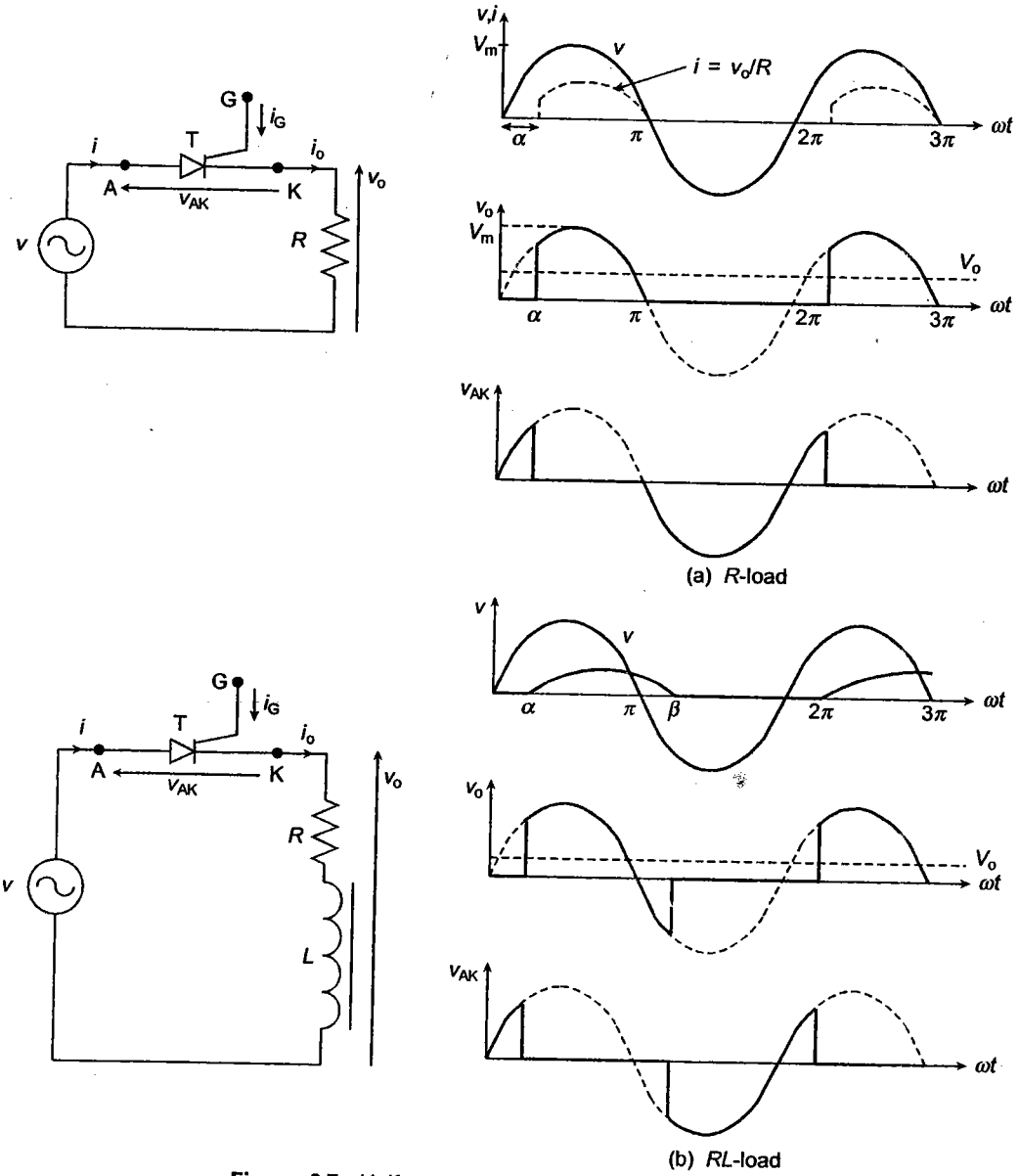


Figure 6.7 Half-wave, fully-controlled converters.

A family of curves for β versus the switching-angle α was shown in Fig. 5.7. The effect of switching angle is shown in Fig. 6.7b. The average value of the output voltage is given by

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{\beta} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{2\pi}(\cos\alpha - \cos\beta) \tag{6.9}$$

Here the conduction period of the thyristor in positive half-cycle ($\pi - \alpha$) is more than the conduction period in the negative half-cycle ($\beta - \pi$). It depends upon α and ϕ. Therefore, the

average values of the load current (I_o) and load voltage (V_o) are always positive. The converter operates only in the first quadrant of the v_o-i_o plane for R and RL loads. Moreover, V_o is also equal to the voltage drop across the resistor, because the average voltage drop of an inductor (v_L) over a cycle is zero. Thus,

$$V_o = V_R + V_L = I_o R \tag{6.10}$$

6.4.2 Half-wave, Half-controlled Converters

If a freewheeling diode (D_f) is also connected across the load in the above converter (Fig. 6.7), this converter becomes a half-wave, half-controlled converter. In this case, SCR commutates at $\omega t = \pi$ and therefore v_o is always positive for R as well as RL loads. The average value of v_o is same, as given in (6.6).

6.4.3 Full-wave, Half-controlled Converters

The half-wave, controlled converters discussed above, are seldom used in practice. A practical and commonly used controlled converter uses full-wave, 2-pulse, configurations. There are several configurations of this converter, as shown in Fig. 6.8. It is also called a *two-pulse, half* or

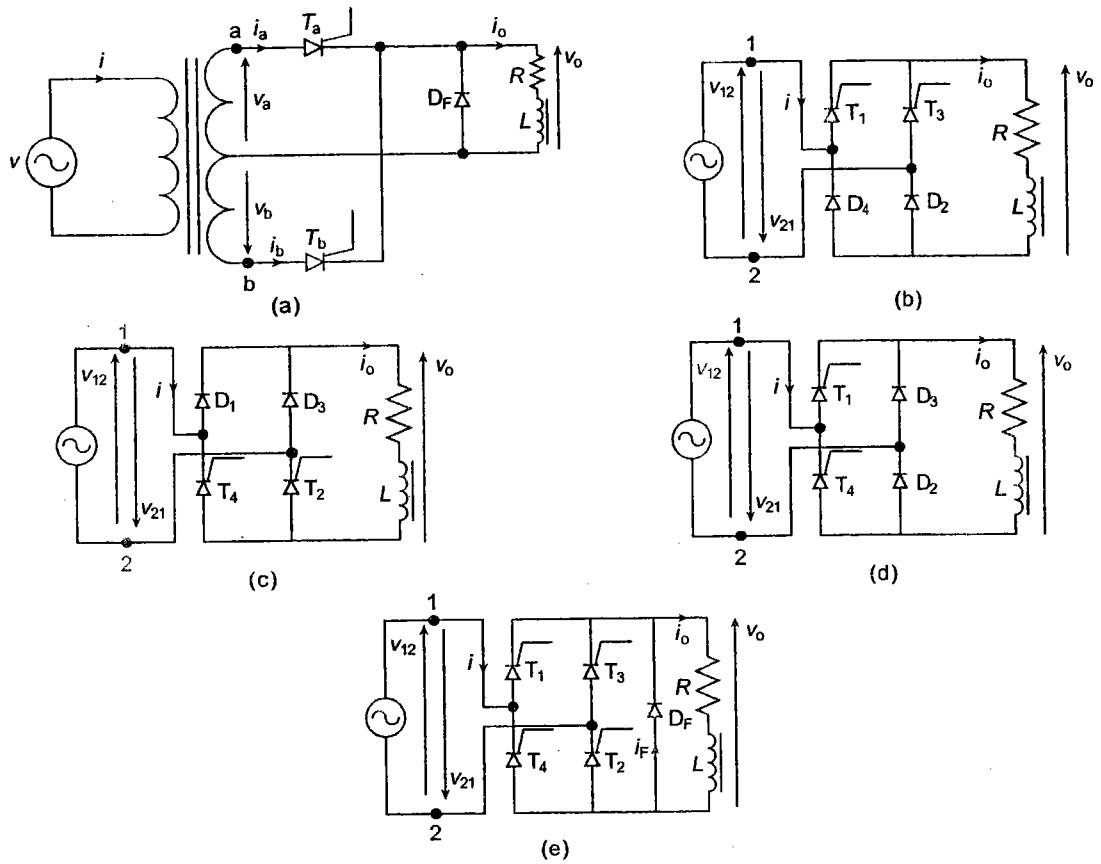


Figure 6.8 Various circuit configurations of semi-converters.

semi-converter. A large number of circuit configurations is available for these converters. Both SCR and diodes are used here. Although an additional transformer is required in the first configuration but the number of devices is minimum, i.e. three only (Fig. 6.8a). Similarly, in the last configuration, there is maximum number of devices. Basically, both these configurations are modified form of a fully-controlled converter by addition of a freewheeling diode (D_F). When the cost of a transformer is less than the cost of a device (SCR), the first configuration will be preferred. Similarly, if a fully-controlled converter is available, by addition of a diode, the converter will work as a semi or half-controlled converter. Figure 6.9 shows the switching mechanism of a centre-tapped transformer based semi-converter with a discontinuous load current.

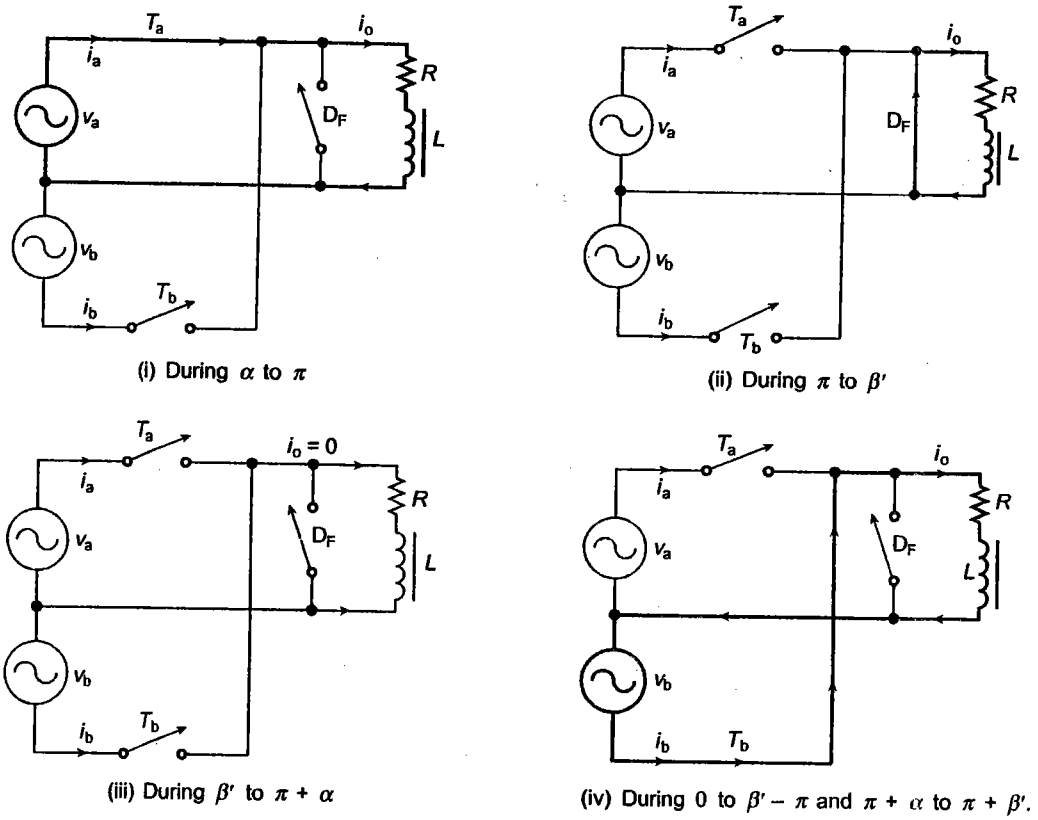


Figure 6.9 Switching mechanism of the semi-converters (with centre-tap transformer) for a discontinuous load current.

When T_a is triggered at $\omega t = \alpha$ and it conducts up to $\omega t = \pi$, it makes cathode of D_F negative and it becomes forward biased and hence conducts. The load current (i_o) now finds a short-circuited path (ideally) and flows through D_F and continues to flow up to β'. Since i_o (or i) ceases to flow through T_a and a negative voltage appears across it ($v_{AK} = v_a$), hence T_a commutates. Now, D_F commutates at β', when the current through it reaches (ideally) zero level. During the second half-cycle, the same process repeats for T_b. The relevant waveforms are shown in Fig. 6.10 for both discontinuous and continuous load current. During the discontinuity of the load current (from β'

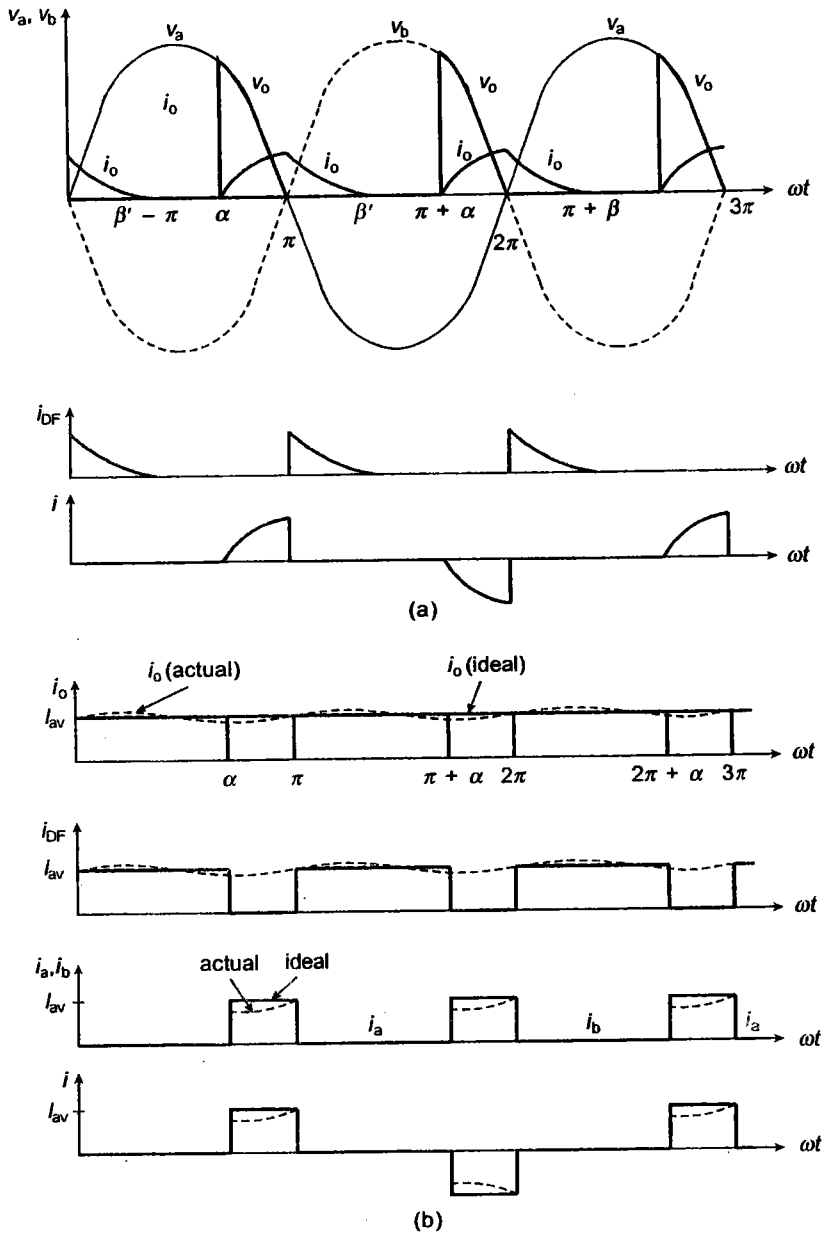


Figure 6.10 Waveforms of semi-converter (a) for discontinuous i_o and (b) for continuous i_o.

to $\pi + \alpha$ and from $\beta' - \pi$ to α), no device conducts (blanking period). For a large value of L ($\omega L >> R$), i_o is continuous and no blanking period exists. However, the input or line current is never continuous.

Table 6.1 shows the conduction period of each device in different configurations of the semi-converter (Fig. 6.8), when the load current is continuous.

Table 6.1 Conducting Devices for Semi-converters

Circuits of Fig. 6.8	0 to α (2π to $2\pi + \alpha$)	α to π	π to ($\pi + \alpha$)	($\pi + \alpha$) to 2π
(a)	D_F	T_1	D_F	T_2
(b)	T_3, D_2	T_1, D_2	T_1, D_4	T_3, D_4
(c)	D_1, T_4	D_1, T_2	T_2, D_3	D_3, T_4
(d)	D_2, D_3	T_1, D_2	D_2, D_3	D_3, T_4
(e)	D_F	T_1, T_2	D_F	T_3, T_4

In all the bridge circuits (Figs. 6.8b–e), whenever the supply voltage becomes negative, the freewheeling diode (D_F) becomes forward biased, and it conduct with the load current. Thus it offers a freewheeling path for the load current and the negative supply voltage does not reach to the load. Figure 6.11 shows the switching mechanism of the bridge circuit configuration shown in the Fig. 6.8b.

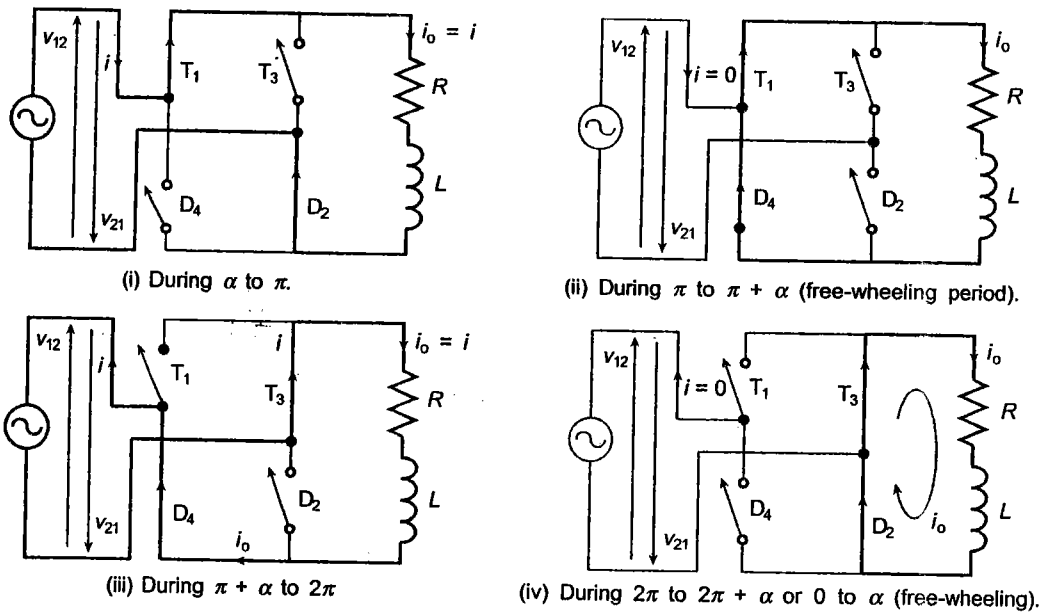


Figure 6.11 Switching mechanism of a semi-converter bridge.

The average value of output voltage for both continuous and discontinuous load current and for R and RL loads, is same, which is given by

$$V_o = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{\pi}(1 + \cos \alpha) \tag{6.11}$$

The maximum output voltage is $V_{o(max)} = 2V_m/\pi$, for $\alpha = 0$. Then the normalized output voltage (V_{on}) is given by

$$V_{on} = \frac{V_o}{V_{o(max)}} = \frac{1}{2}(1 + \cos \alpha) \tag{6.12}$$

Thus, V_o is independent of the load (R or RL) and it can simply be controlled by α (Fig. 6.12).

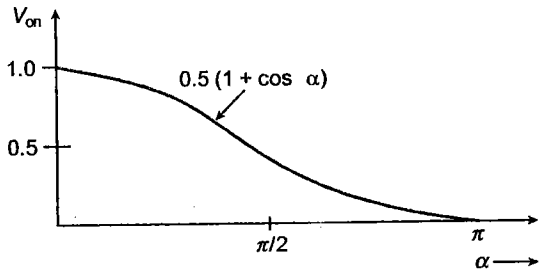
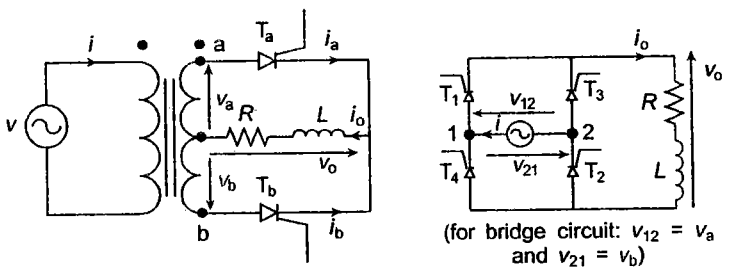


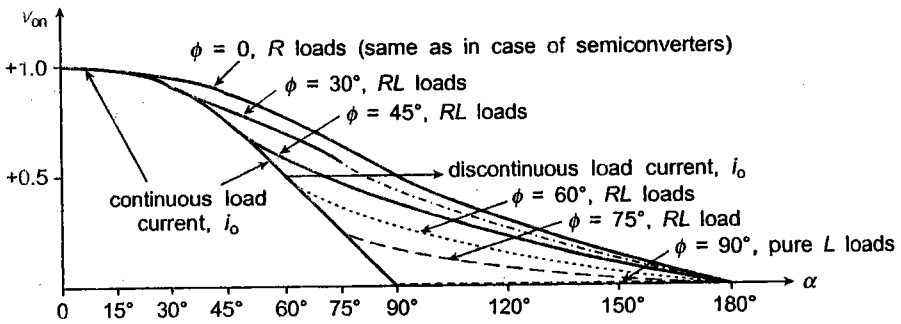
Figure 6.12 Normalized output voltage of semi-converters for *R* and *RL* loads.

6.4.4 Full-wave, Full Converters

The term *full-wave* corresponds to the output voltage control in both the half-cycles. Similarly, the term *fully-controlled* or *full-converter* corresponds to the controllability of converter in the first as well as fourth quadrant of the output (v_o-i_o) characteristics plane. It is also called a *two-pulse, full-wave, fully-controlled* converter. Although the load current flows in one direction only but the output voltage and power input to the converter is bi-directional. Therefore, the converter may operate in the first and the fourth quadrants. There are two circuit configurations of this converter, which are shown in Fig. 6.13. When size, weight and cost due to the presence of a centre-tapped transformer are not important, then the first configuration is simple and attractive. Only two SCRs with a common cathode connection are needed. A simple gate-trigger circuit with

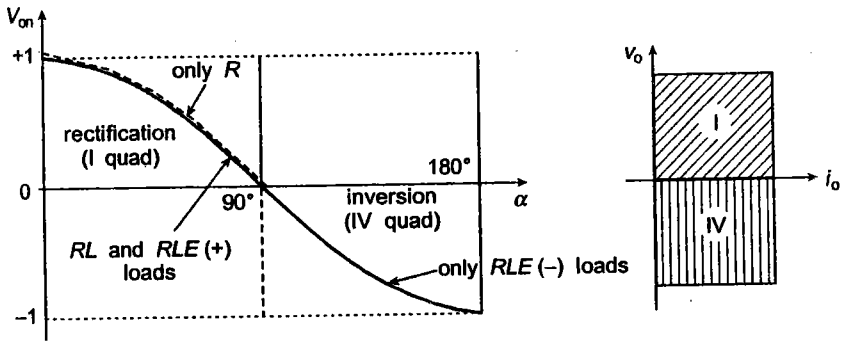


(a)

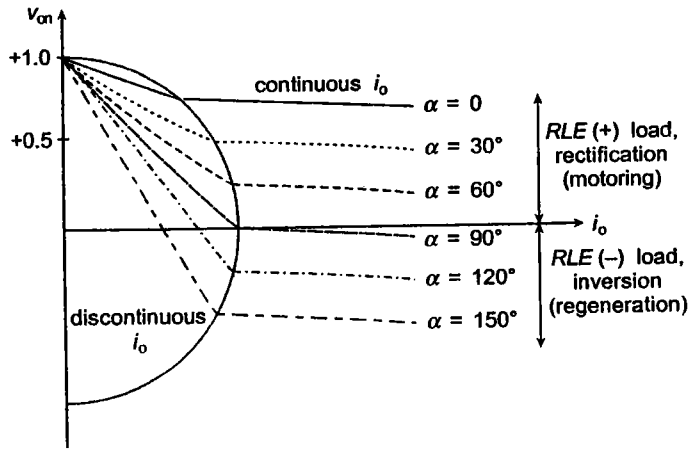


(b) Rectifier operation of full converters with *R* and *RL* loads

Figure 6.13 (*Cont.*)



(c) Output characteristics of full-converters with continuous i_o ($\phi \simeq 90°$)

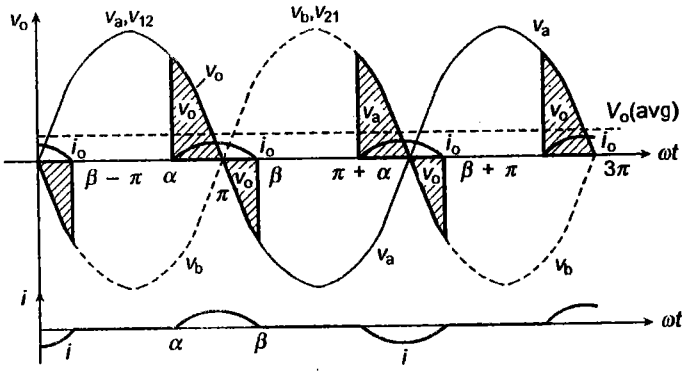


(d) Rectifier/inverter operation of full converters with RLE loads

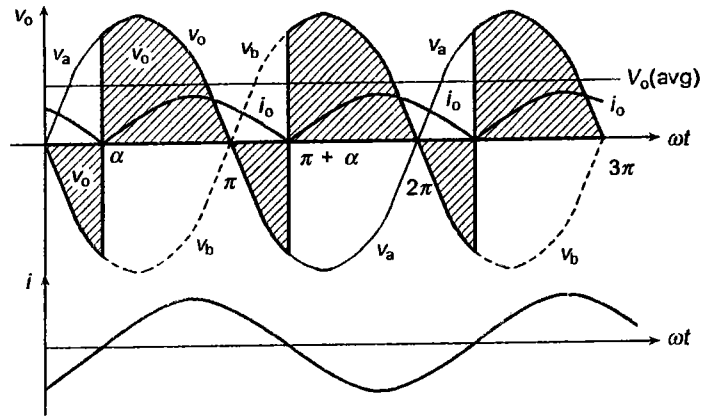
Figure 6.13 Output characteristics of full-converters.

single dc power supply and without buffer or isolation can be used (as cathode of both SCRs are common). However, apart from the requirement of a transformer and ideal-period (half-cycle) of its secondary winding, the thyristors experience twice of the peak supply voltage, $2V_m = 2\sqrt{2}\,V$. In the second circuit configuration, no transformer is needed but four thyristors are required. The size and weight of this circuit are less. However, if the cost of a transformer is less than the cost of two additional SCRs, then the first configuration may be preferred.

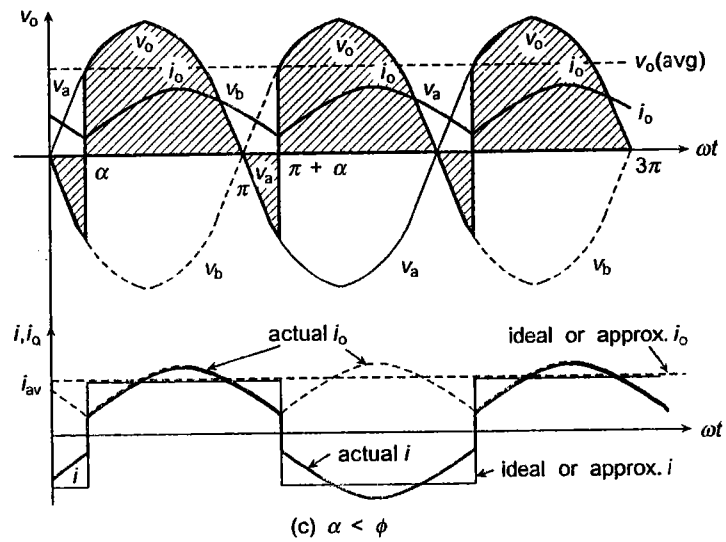
The performance of the converter depends upon the switching angle (α), and the impedance angle (ϕ). Since an SCR is a unidirectional device, the direction of the current through it (i_A) always remains same. However, due to an RL load, the conduction continues even in the next half-cycle. Therefore, in case of a full-converter, the instantaneous value of v_o may be positive or negative but the average value of output voltage (V_o) will be only positive for RL loads (Fig. 6.14). However, for an active or R-L-E negative load, the converter may operate in the fourth quadrant of v_o-i_o plane and V_o becomes negative. The load current may be discontinuous, just continuous (or sinusoidal) or continuous. It depends upon α and ϕ of RL loads, as discussed as follows:



(a) $\alpha > \phi$



(b) $\alpha = \phi$



(c) $\alpha < \phi$

Figure 6.14 Circuits and waveforms of full-converters.

Discontinuous I_o ($\alpha > \phi$)

Figure 6.14 a shows the load current waveform which is similar to that of the half-wave (1-pulse) configuration (Fig. 6.7b). The same equation of the current (6.8) holds good. However, due to switching of another SCR, there are two pulses in each cycle. Therefore, the average or the mean output voltage for this full-wave circuit will be twice that of the half-wave case (Eq. 6.9), which is given by

$$V_o = \frac{1}{\pi}\int_{\alpha}^{\beta} V_m \sin \omega t \, d(\omega t) = \frac{V_m}{\pi}(\cos\alpha - \cos\beta) \tag{6.13}$$

It is evident from equation (6.13) that the output voltage is load dependent due to β. The value of β depends upon the inductance (L) of the load as it was shown in Fig. 5.7. For R and RL loads, V_o is always positive and converters operate in the first quadrant of v_o-i_o plane.

Just Continuous i_o ($\alpha = \phi$)

Under this condition, T_a is triggered at α and it commutates at $\omega t = \beta = \pi + \alpha$ (Fig. 6.14b). Immediately thereafter, T_b is triggered. It is evident from equation (6.8), the load and the line current become sinusoidal as the transient term vanishes for $\alpha = \phi$. Therefore, THD becomes zero and PF is equal to cos ϕ. The expression of the load current, given by equation (6.8) reduces to

$$i = i_o = \frac{V_m}{Z}\sin(\omega t - \phi), \qquad \alpha \le \omega t \le \beta = \pi + \alpha \tag{6.14}$$

The average output voltage can be obtained from Eq. (6.13), which is given by

$$V_o = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin \omega t \, d(\omega t) = \frac{2V_m}{\pi}\cos\alpha, \quad \text{for } \alpha = \phi \text{ and } \alpha \le \omega t \le \pi + \alpha \tag{6.15}$$

The maximum and the normalized values of V_o are given by

$$V_{o(max)} = \frac{2V_m}{\pi} \quad \text{and} \quad V_{on} = \frac{V_o}{V_{o(max)}} = \cos\alpha \tag{6.16}$$

Continuous i_o ($\alpha < \phi$)

Under this condition, the load current never reduces to zero. Therefore, either T_a or T_b will always be conducting (Fig. 6.14c). At $\omega t = \pi + \alpha$, T_a is still conducting because i_a is still flowing through it and both v_a and v_o are negative and v_b is now positive. When T_b is triggered, it applies a positive voltage at the cathode of T_a and provides an alternative path for i_o through itself. The current through T_a ceases and it commutates at $\omega t = \pi + \alpha$ (as anode is negative and cathode is positive due to v_b). At this condition,

$$v_{AK} = v_a - v_b = -2|v_b| = -2v_a \tag{6.17}$$

Thus, the maximum voltage during commutation of T_a (or T_b) is $2V_m$ and that appears at $\alpha = \pi/2$. Therefore, the voltage rating of the SCR should be double that of the bridge configuration. The instantaneous value of v_o is positive for R loads and both positive and negative for RL loads.

However, the average value is always positive. It is same as given in (6.15) except $\alpha \leq \phi$. The maximum and normalized values are same, as given in (6.16). Since ϕ (hence α) cannot be more than 90° (for highly inductive loads), V_{on} varies from +1.0 to 0 (Fig. 6.13).

In this case, the load current is same at $\omega t = \alpha$ and $\omega t = \pi + \alpha$. Therefore, by substituting these conditions in (6.7), the load current is given by

$$i_o = \frac{V_m}{Z}\left[\sin(\omega t - \phi) + \frac{2\sin(\alpha - \phi)}{1 - \exp(-\pi/\tan\phi)} \exp\frac{\alpha - \omega t}{\tan\phi}\right], \qquad \alpha \leq \omega t \leq \pi + \alpha \quad (6.18)$$

Under all delay or switching angle conditions, the average or the mean output current, $I_o = V_o/R$.

In case of a bridge configuration (Fig. 6.13a), while T_1–T_2 pair was conducting, T_3–T_4 pair is triggered at $\omega t = \pi + \alpha$. T_3 applies a positive voltage (v_{21}) at the cathode of T_1 and T_4 applies a negative voltage (v_{12}) at the anode of T_2. Moreover, both these devices (T_3 and T_4) provide an alternative path for the inductive load current (i_o). Thus, the current through T_1 and T_2 ceases and commutation of these devices take place at $\omega t = \pi + \alpha$. The same phenomenon repeats for T_3–T_4 pair in the next half-cycle.

6.4.5 Full-converters with *RLE* Load

Often a converter is required to control the speed and torque in a dc motor drive. A resistance, an inductance and a back emf (E) are used to represent an armature circuit of a dc motor. Both continuous and discontinuous load current flows in the armature circuit.

Discontinuous Load Current

The waveform of this circuit is shown in Fig. 6.15 with a discontinuous load current. In this case, T_a cannot be triggered unless its anode voltage (v_{12}) is greater than E. Therefore, conduction of T_a cannot start conduction before α_{min} and after α_o. Here, α_{min} is less than $\pi/2$ and $\alpha_o = \pi - \alpha_{min}$. The value of α_{min} is given by

$$\alpha_{min} = \sin^{-1} m \quad (6.19)$$

where $m = E/V_m$. The line or the load current can be found by solving the voltage equation:

$$V_m \sin\omega t = L\frac{di}{dt} + Ri + E, \qquad \alpha \leq \omega t \leq \beta' \quad (6.20)$$

It gives,

$$i_o = i = \frac{V_m}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)\exp\frac{\alpha - \omega t}{\tan\phi}\right] - \frac{E}{R}\left(1 - \exp\frac{\alpha - \omega t}{\tan\phi}\right)$$

$$= \frac{V_m}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)\exp\frac{\alpha - \omega t}{\tan\phi} - \frac{m}{\cos\phi}\left(1 - \exp\frac{\alpha - \omega t}{\tan\phi}\right)\right], \qquad \alpha \leq \omega t \leq \beta' \quad (6.21)$$

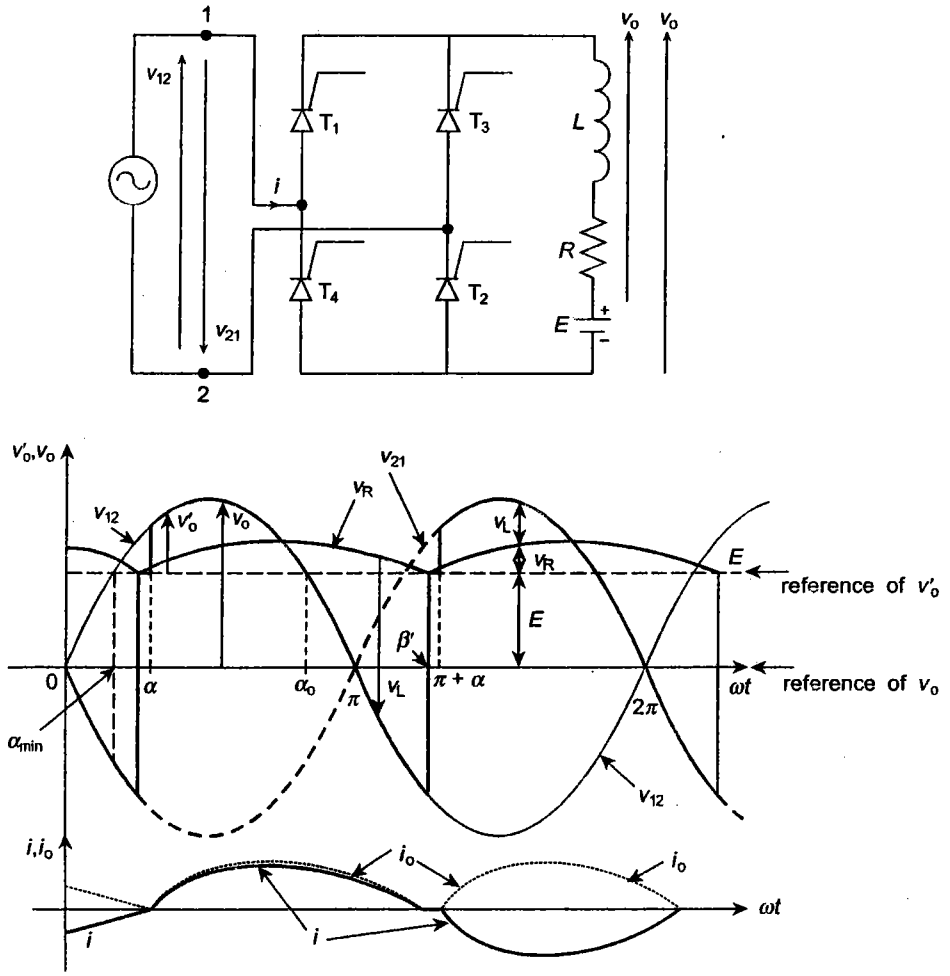


Figure 6.15 A full-converter with an *RLE* (+) load.

The value of β' can be obtained by iteration method (as discussed in Chapter 5), using the above equation for $i(\beta') = 0$. The average value of output voltage is given by

$$V_o = \frac{1}{\pi}\left[\int_{\alpha}^{\beta'} V_m(\sin\omega t)\, d(\omega t) + \int_{\beta'}^{\pi+\alpha} E\, d(\omega t)\right] \tag{6.22}$$

$$= \frac{V_m}{\pi}\left[(\cos\alpha - \cos\beta') + m(\pi - \beta' + \alpha)\right], \qquad \alpha < \beta' < \pi + \alpha \tag{6.23}$$

and

$$I_o = \frac{V_m}{\pi R}\left[(\cos\alpha - \cos\beta') - m(\beta' - \alpha)\right] \tag{6.24}$$

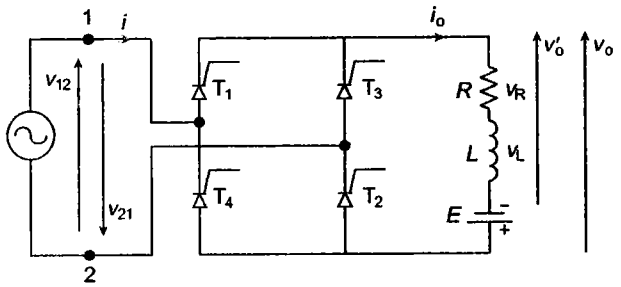
Continuous Load Current

For a continuous current, $\beta' = \pi + \alpha$, and accordingly the above equations will be modified. The average output voltage is same as that of a full-wave, fully controlled converter, as given in (6.15). It is positive and depends only on α where $\alpha \leq \phi$. The average value of the load current is given by

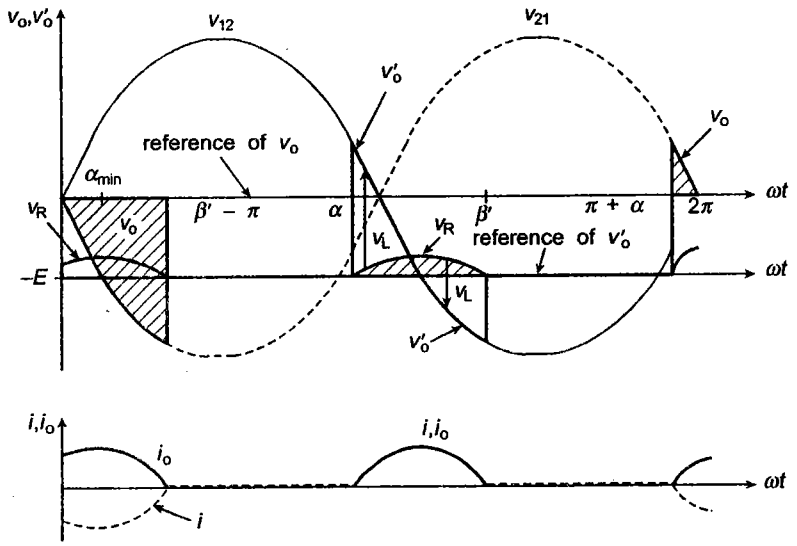
$$I_o = \frac{V_m}{R}\left(\frac{2}{\pi}\cos\alpha - m\right) \tag{6.25}$$

RLE Load (Inverter Mode)

If the polarity of E is reversed, the above converter (Fig. 6.15), can act as a line-commutated inverter as shown in Fig. 6.16. A line-commutated dc-to-ac inverter is basically a phase-controlled

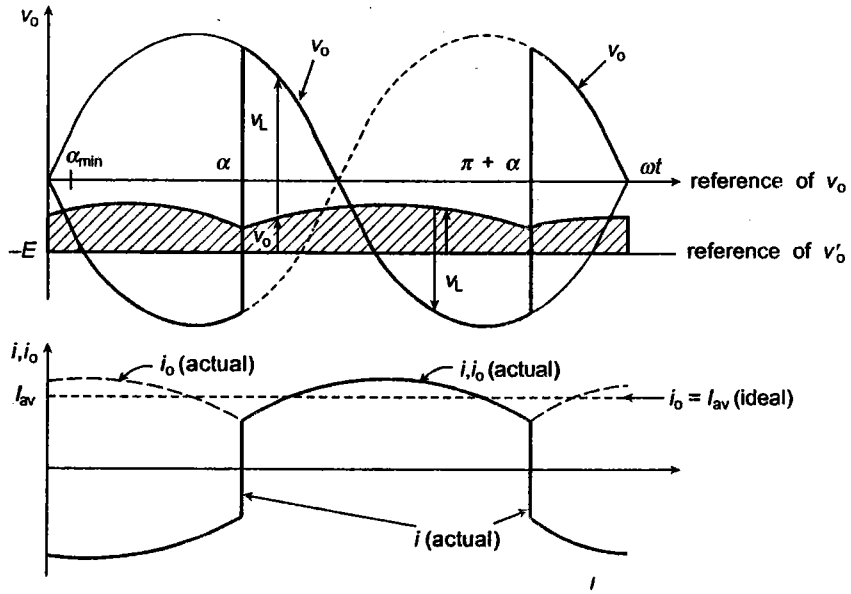


(a) Circuit configuration



(b) Waveforms for discontinuous load current (i_o)

Figure 6.16 (*Cont.*)



(c) Waveforms for continuous load current (i_o)

Figure 6.16 A full-converter with an *RLE* (–) load.

converter with an *RLE* (–) load (i.e. an *RL* load with a negative voltage source, *E*). In some part of the voltage cycle, the power flow is from the ac source to the dc source and in some part of the cycle it is from the dc source to the ac source. However, the average value of the power flow is negative (inversion) for $\alpha > 90°$. In case of a dc motor, if α is increased beyond 90° (with reverse *E*) for forward breaking, the motor operates in the fourth quadrant of v_o-i_o plane. Now, V_{on} may vary from +1.0 to –1.0. While an independent dc source (e.g. storage battery, solar photovoltaic (PV) cell or array, etc.), may be used to convert a dc power into an ac power, using this configuration. Figure 6.16 shows the inversion operation for a continuous and a discontinuous current. Here α may be increased beyond π, i.e. $\omega t = \pi + \alpha_{min}$. The power inversion can be computed with the help of Eqs. (6.21), and (6.22). The converter operates in inversion mode only when $\alpha > 90°$ and there is an inductive *RL* load in the output circuit. Normally, α is varied up to 165° for inversion operation (to facilitate the line-commutation voltage for SCR otherwise it becomes very small near $\omega t \cong 180°$).

Example 6.2 An armature (*RLE* load) of a separately excited dc motor is fed from single-phase, full-wave, fully controlled converter. The supply ac voltage $V = 220$ V, $R_a = 0.06\ \Omega$, $L_a = 0.85$ mH, I_a (rated) = 150 A, speed (rated) = 875 rpm, V_a (rated) = 200 V. Find the output voltage and α for a rated load when

(a) E = 160 V (speed = 733 rpm, first quadrant)

(b) E = –109 V (speed = –500 rpm, fourth quadrant)

Solution (a) The rated load current, $I_a = 150$ A. The dc voltage of the armature circuit is given by

$$V_a = E + I_a R_a = 160 + 150 \times 0.06 = 169 \text{ V}$$

Assuming continuous conduction, the output voltage of the converter,

$$V_o = \frac{2V_m}{\pi}\cos\alpha = V_a$$

or

$$\cos\alpha = \frac{169\pi}{2\sqrt{2} \times 220} = 0.853 \quad \text{and} \quad \alpha = 31.43°$$

(b) $V_a = -109 + 150 \times 0.06 = -100$ V. Then

$$\cos\alpha = \frac{-100\pi}{2\sqrt{2} \times 220} = -0.505 \quad \text{and} \quad \alpha = 120.3°$$

Example 6.3 Find the output voltage of a full-converter for different R and RL loads ($\phi = 0°$, 30°, 60° and 85°).

Solution The output voltage of a full-converter is given by

$$V_o = \frac{V_m}{\pi}(\cos\alpha - \cos\beta)$$

The maximum and the normalized values of V_o are given by

$$V_{o(max)} = \frac{V_m}{\pi}(2\cos\alpha), \qquad \text{for } \beta = \pi + \alpha$$

$$V_{on} = \frac{V_o}{V_{o(max)}} = \frac{1}{2\cos\alpha}(\cos\alpha - \cos\beta)$$

The value of β is available from Table 5.2, for different values of ϕ. For $\alpha \le \phi$, the load current is continuous (otherwise discontinuous), and therefore, $V_{on} = \cos\alpha$. The tabulated values are shown in Table 6.2.

Table 6.2 V_{on} for Full Converters

α (in degree)	$\phi = 0°$ (R load)	$\phi = 30°$ (RL load)	$\phi = 60°$ (RL load)	$\phi = 85°$ (RL load)
0°	1.0	1.0	1.0	1.0
30°	0.93	0.87	0.87	0.87
60°	0.75	0.68	0.5	0.68
90°	0.5	0.43	0.29	0.07
120°	0.25	0.4	0.24	0.04
150°	0.07	0.074	0.02	0
180°	0	0	0	0

6.5 ANALYSIS OF CONVERTERS

The analysis of different types of ac regulators is discussed in detail in Chapter 5 (Section 5.5). The same analysis is applicable to ac-to-dc converters. In case of a purely resistive load, the

output voltage is a discontinuous rectified sinusoidal voltage. However, the line current is same as the line current of an ac regulator for a resistive load. Therefore, the performance of the converters is same (which is shown in Fig. 6.7). For an *RL* load, depending upon α and ϕ of the load, the nature of the load current varies. Therefore, for an accurate analysis, numerical techniques (as discussed in Chapter 5) may be employed. However, in general, for the sake of simplicity, it is assumed that the load impedance is highly inductive ($\omega L >> R$), therefore, the load current is ripple free and it has a constant instantaneous magnitude.

6.5.1 Analysis of Semi-converters

Figure 6.10 shows the input line current of semi-converters. Since the instantaneous value of the load current is assumed to be constant, from α to π, it is equal to I_a and from $\pi + \alpha$ to 2π, it is equal to $-I_a$. It can be expressed in Fourier series as

$$i(\omega t) = I_{dc} + \sum_{n=1,2,\ldots}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t)$$

Due to symmetry of waveform

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i(\omega t)\, d(\omega t) = 0$$

with

$$a_n = \frac{1}{\pi} \int_0^{2\pi} i(\omega t)(\cos n\omega t)\, d(\omega t)$$

$$= \frac{1}{\pi} \left[\int_{\alpha}^{\pi} I_{av} (\cos n\omega t)\, d(\omega t) + \int_{\pi+\alpha}^{2\pi} (-I_{av})(\cos n\omega t)\, d(\omega t) \right]$$

$$= -\frac{2I_{av}}{n\pi} \sin n\alpha, \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.26}$$

$$= 0 \qquad \text{for } n = 2, 4, 6, \ldots$$

and

$$b_n = \frac{1}{\pi} \int_0^{2\pi} i(\omega t)(\sin n\omega t)\, d(\omega t)$$

$$= \frac{1}{\pi} \left[\int_{\alpha}^{\pi} I_{av} (\sin n\omega t)\, d(\omega t) + \int_{\pi+\alpha}^{2\pi} -I_{av} (\sin n\omega t)\, d(\omega t) \right]$$

$$= \frac{2I_{av}}{n\pi} (1 + \cos n\alpha), \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.27}$$

$$= 0 \qquad \text{for } n = 2, 4, 6, \ldots$$

Also,

$$\phi_n = \tan^{-1}\frac{a_n}{b_n} = -\frac{n\alpha}{2} \tag{6.28}$$

The rms value of the nth harmonic component of the input or line current is given by

$$I_n = \sqrt{\frac{a_n^2 + b_n^2}{2}} = \frac{2\sqrt{2}I_{av}}{n\pi}\cos\frac{n\alpha}{2}, \qquad n = 1, 3, 5, \ldots \tag{6.29}$$

Thus, $n = 1$ gives the rms value of the fundamental component of the input current, i.e.

$$I_1 = 2\frac{\sqrt{2}I_{av}}{\pi}\cos\frac{\alpha}{2} \tag{6.30}$$

Also, the rms value of the input current is given by

$$I = \left[\frac{1}{2\pi}\int_0^{2\pi} i^2(\omega t)\, d(\omega t)\right]^{1/2}$$

$$= \left[\frac{2}{2\pi}\int_\alpha^{\pi} I_{av}^2\, d(\omega t)\right]^{1/2}$$

$$= I_{av}\left(\frac{\pi - \alpha}{\pi}\right)^{1/2} \tag{6.31}$$

Therefore,

$$\text{THD} = \sqrt{\frac{I^2}{I_1^2} - 1} = \sqrt{\frac{\pi(\pi - \alpha)}{8\cos^2(\alpha/2)} - 1} = \sqrt{\frac{\pi(\pi - \alpha)}{4(1 + \cos\alpha)} - 1} \tag{6.32}$$

Also

$$\text{Displacement factor} = \cos\phi_1 = \cos\left(-\frac{\alpha}{2}\right) \tag{6.33}$$

Then

$$\text{PF} = \frac{I_1}{I}\cos\frac{\alpha}{2} = \frac{2(1 + \cos\alpha)}{\sqrt{2\pi(\pi - \alpha)}} \tag{6.34}$$

6.5.2 Full Converters

Figure 6.13 shows the input line current of full converters. Since the instantaneous value of the load current is assumed to be constant, from α to π, $i = I_{av}$ and from $\pi + \alpha$ to 2π, $i = -I_{av}$. It can be expressed in Fourier series as

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\, d(\omega t) = 0, \qquad \text{(due to symmetry of waveform)}$$

with

$$a_n = \frac{1}{\pi}\int_{\alpha}^{2\pi+\alpha} i(\omega t)(\cos n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\int_{\alpha}^{\pi+\alpha} I_{av}\,(\cos n\omega t)\, d(\omega t)$$

$$= -\frac{4I_{av}}{n\pi}\sin n\alpha, \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.35}$$

and

$$b_n = \frac{1}{\pi}\int_{\alpha}^{2\pi+\alpha} i(\omega t)(\sin n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\int_{\alpha}^{\pi+\alpha} I_{av}(\sin n\omega t)\, d(\omega t)$$

$$= \frac{4I_{av}}{n\pi}\cos n\alpha, \qquad \text{for } n = 1, 3, 5, \ldots \tag{6.36}$$

Then

$$I_n = \sqrt{\frac{a_n^2 + b_n^2}{2}} = \frac{4I_{av}}{\sqrt{2}n\pi} = \frac{2\sqrt{2}I_{av}}{n\pi} \tag{6.37}$$

Therefore, the fundamental component the current is given by

$$I_1 = \frac{2\sqrt{2}I_{av}}{\pi} \tag{6.38}$$

The instantaneous value of i is constant, hence the rms value is also same (i.e. $I = I_{av}$). Therefore,

$$\text{THD} = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.4834 = 48.34\%$$

Also,

$$\phi_n = \tan^{-1}\frac{a_n}{b_n} = \tan^{-1}[\tan(-n\alpha)] = -n\alpha \tag{6.39}$$

$$\text{Displacement factor} = \cos\phi_1 = \cos(-\alpha) \tag{6.40}$$

$$\text{PF} = \frac{I_1}{I}\cos(-\alpha) = \frac{2\sqrt{2}}{\pi}\cos(-\alpha) = 0.9003\cos(-\alpha) \tag{6.41}$$

Example 6.4 For a highly inductive *RL* load, find THD and PF of a single-phase, semi-converter.

Solution Let the load current (i_o) is ripple-free. Then, I_{av}, the average value of i_o is equal to the rms value of the line current (i). For equations (6.28)–(6.32), the computed values are given in Table 6.3.

Table 6.3 Performance of a Semi-converter for a Highly Inductive *RL* Load (in %)

α in deg.	I_1	I	THD	PF
0°	90.03163	100	48.34259	90.03163
22.5°	88.3017	93.54144	34.957	92.58464
45°	83.17838	86.60254	28.98754	88.73504
67.5°	74.85857	79.05695	33.95788	78.73138
90°	63.66198	70.71068	48.34259	63.66198
112.5°	50.01889	61.23725	70.63053	45.37926
135°	34.45361	50	105.1693	26.36965
157.5°	17.5643	35.35535	174.6941	9.691959

Example 6.5 Compare the output voltage of a semi-converter and a full converter with highly inductive *RL* loads.

Solution The output voltage of a semi-converter is independent of ϕ (i.e. same for R as well as *RL* loads). The normalized value is given by

$$V_{on} = \frac{1}{2}(1 + \cos\alpha)$$

For a highly inductive *RL* load, let $\phi \cong 90°$. Then the load current will be continuous for $\alpha \leq \phi$. The output voltage (V_o) is given by

$$V_o = \frac{V_m}{\pi}(\cos\alpha - \cos\beta)$$

$$= \frac{2V_m}{\pi}\cos\alpha, \qquad \text{(for a continuous load current, } \beta = \pi + \alpha)$$

and $V_{on} = \cos\alpha$. Table 6.4 shows V_{on} of both converters:

Table 6.4 Comparison of Performance of Full and Semi-converters

α (in degrees)	V_{on} (semi-converter)	V_{on} (full-converter)
0°	1.0	1.0
30°	0.93	0.87
60°	0.75	0.5
90°	0.5	0.0
120°	0.25	0.0
150°	0.067	0.0
180°	0.0	0.0

6.6 THREE-PHASE CONVERTERS

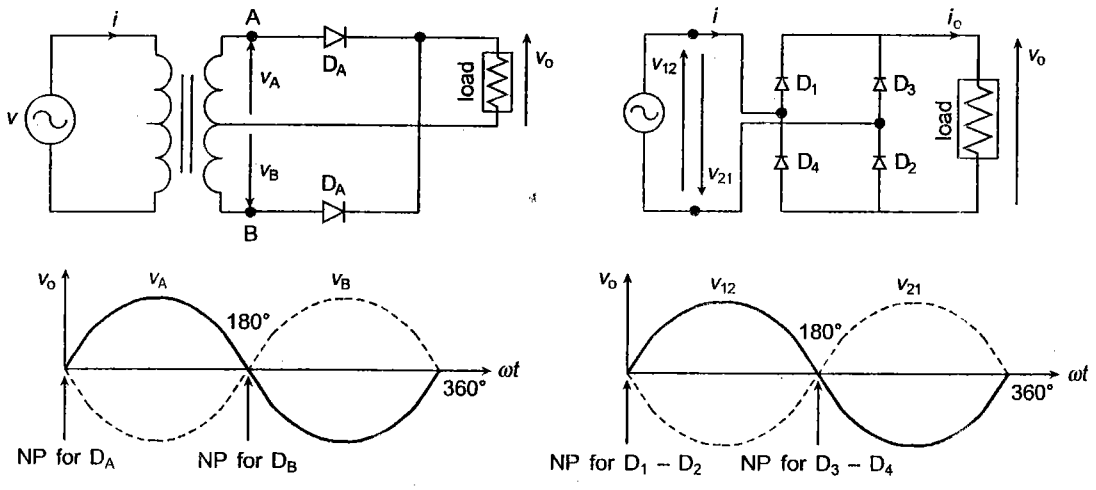
At a higher-power level, above a few kW, normally a three-phase system is employed. It reduces the harmonics of the line current and load voltage, and causes balanced loading on the utility system (distribution line of the power system). Since the voltage and current ripples reduce

drastically, the EMI reduces and the requirement of the harmonic filters also becomes nominal. Among all types of the three-phase converters, three-phase six-pulse bridge type converters are most common. However, for the sake of understanding, first of all three-phase, three-pulse type converters are discussed.

It becomes easy to draw waveforms for three-phase systems using the waveform exercise sheet, given in Appendix (Fig. A13).

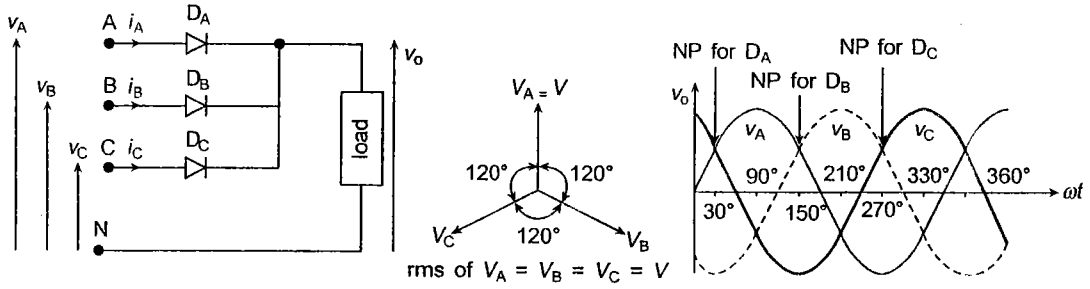
6.6.1 Rectifier Operation

As discussed in the Section 6.1, when a diode is in forward-biased condition, it conducts. However, a thyristor requires a triggering signal, too. For a single-phase system, there is only one positive voltage pulse in a cycle. During the entire period of the half-cycle, a diode (or thyristor) is in forward-biased condition (Fig. 6.17). Therefore, a thyristor can be switched on during this period. While in case of a poly-phase system, there are several such pulses, which overlap each other (Fig. 6.17c). In case of diodes in a poly-phase system, a particular diode conducts for a period during which its anode voltage is higher than all the other voltages (this voltage appears at its cathode and prevents the conduction of any other diode). This period is 180° or half-period in a single-phase



(a) Single-phase, full-wave with transformer

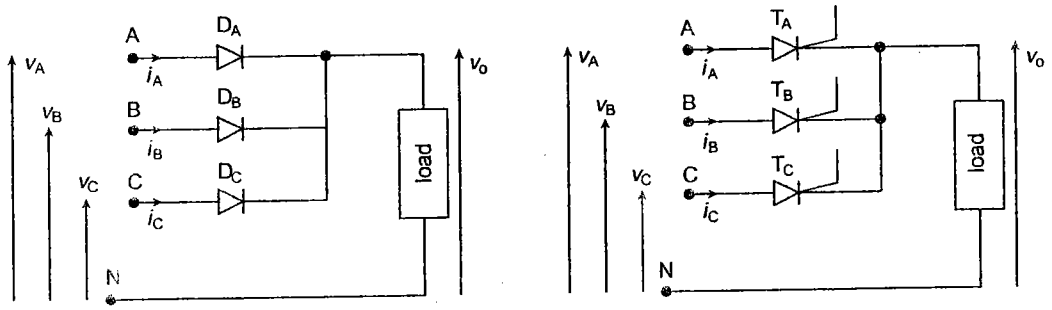
(b) Single-phase, full-wave without transformer



(c) Three-phase, three-pulse, half-wave rectifier

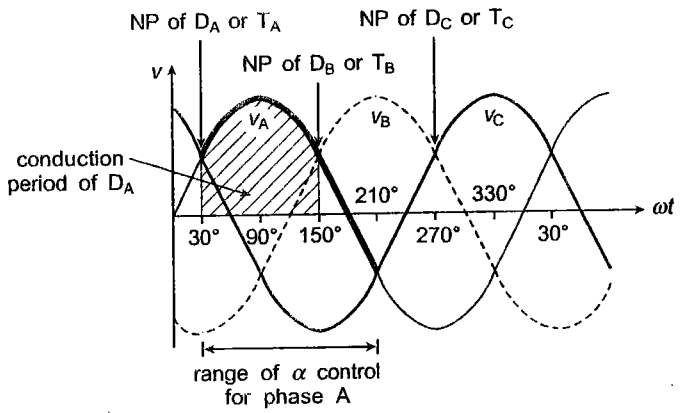
Figure 6.17 NP of Rectifier circuits.

system (Figs. 6.17a and b) and 120° for a three-phase, half-wave, diode bridge converter (Fig. 6.17c). The anode voltage of the diode where it just becomes higher than all the other voltages, is the reference point of switching or delay angle for thyristors in a bridge circuit. This point is also called *natural switching point* (NP) for naturally commutated or line-commutated converters. For a three-phase system, the possible range for triggering (switching) a thyristor starts where the anode voltage just becomes highest and continues till it just becomes lowest, as shown in Fig. 6.18. Thus the switching delay angle varies from 0° to 180°. The time interval between the switching pulses for each thyristor depends upon the type of converter (bridge) connection. In case of three-pulse converters, the controller generates three equidistant gate trigger pulses per cycle of the supply voltage. Thus these pulses appear at an interval of 120°. Similarly for six-pulse, half- or full-converters, six-gate trigger pulses appear at an interval of 60° only.



(a) Uncontrolled converter

(b) Controlled converter



(c) Waveforms

Figure 6.18 NP and range of α control in a three-phase, half-wave system.

For resistive loads, the current waveforms of the converters are same as the voltage. However, for other loads (e.g. *RL* loads), the current waveforms depend upon various factors including voltage switching angle, *R/X* ratio or ϕ, etc. For the sake of simplicity of study and analysis of converters, in general, here all the loads of ac-to-dc uncontrolled or controlled converters are considered to be highly inductive *RL* load. Therefore, the magnitude of the load current is assumed to be constant (free from ripples).

6.6.2 THREE-PHASE, UNCONTROLLED CONVERTERS

Only diodes are used in such converter circuits (bridges). Thus both turn-on and the conduction period of diodes depend upon the configuration or the type of bridge. Since the input voltage is constant, the average dc or value of the output voltages also remains constant. In general, for an n-phase system, the average output voltage is given by

$$V_o = \frac{V_m}{(2\pi/n)} \int_{-\pi/n}^{\pi/n} \cos \omega t \, d(\omega t) = \frac{V_m \sin(\pi/n)}{\pi/n} \tag{6.42}$$

For highly inductive circuits, the load current may be considered as ripple free. The current through each diode depends upon the number of the current pulses through it. For example, for a single-phase system, there are two pulses in each cycle ($n = 2$), the average current through each diode is given by

$$I_{D(av)} = \frac{I_o}{n} = \frac{I_{av}}{n} \tag{6.43}$$

and the rms current in each diode is given by

$$I_{D(rms)} = \frac{I_o}{\sqrt{n}} = \frac{I_{av}}{\sqrt{n}} \tag{6.44}$$

The ratio of the rms value to the mean value (form factor) is given by

$$K_f = \frac{I_{D(rms)}}{I_{D(av)}} = \sqrt{n} \tag{6.45}$$

THREE-PULSE, HALF-WAVE, UNCONTROLLED CONVERTERS

Three-diodes and a three-phase transformer with star-connected secondary windings are required for this type of converters (Fig. 6.19). However, if neutral is available with the supply (three-phase, four-wire system), the transformer is not required. As discussed earlier, the diode with the highest potential at its anode with respect to the neutral conducts. When the anode voltage of another diode becomes highest, the load current transfers to that diode. The incoming diode (with the highest anode voltage) applies to a higher voltage at the cathode of the outgoing diode and natural commutation (NC) takes place due to reverse-bias condition. The diode conducts from 30° to 150° or (1/3)rd period of the cycle. The load voltage (v_o) becomes equal to v_A. At the end of this period, the anode potential of another diode (D_B) becomes the highest and therefore it conducts and load current transfers from the previous device (D_A) to it. When $\omega t > 150°$, due to the conduction of D_B, v_B reaches the common cathode side ($v_o = v_B$), and therefore, the voltage at the cathode of D_A becomes higher than its anode voltage. Thus it naturally commutates the device (D_A). The average output dc voltage is given by (6.42). Therefore,

$$V_o = \frac{V_m \sin(\pi/3)}{\pi/3} = \frac{3\sqrt{3}}{2\pi} V_m = \frac{3\sqrt{6}}{2\pi} V \tag{6.46}$$

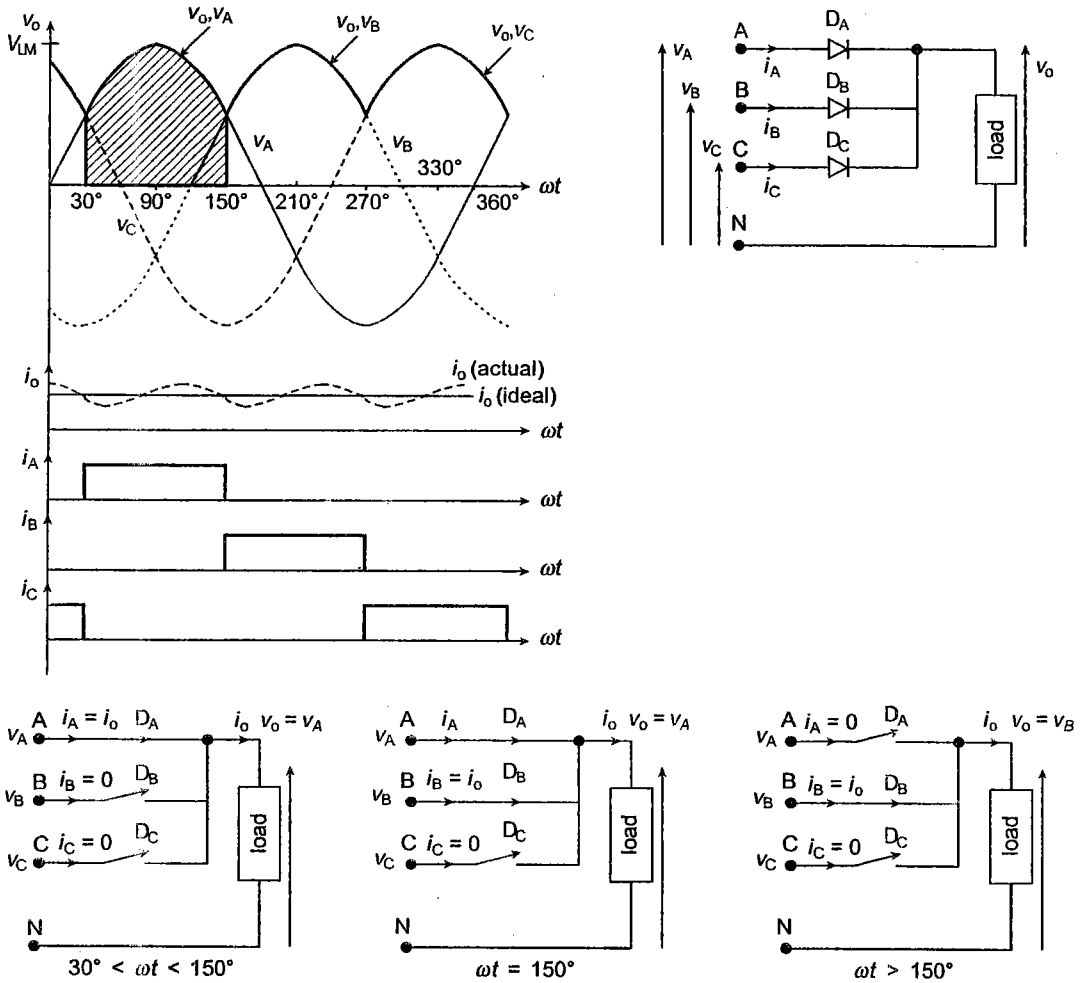


Figure 6.19 Three-phase, three-pulse, half-wave uncontrolled rectifiers.

Each non-conducting diode experiences a maximum voltage that is maximum of two phase-voltage (maximum of line voltage, that is equal to $\sqrt{2}\ \sqrt{3}\ V$ or 2.45 V). It gives the required voltage rating, i.e. the peak inverse voltage (PIV) of the diode. Also, the current through the diode is given by

$$I_{D(av)} = \frac{I_o}{3}, \quad I_{D(rms)} = \frac{I_o}{\sqrt{3}} \quad \text{and} \quad K_f = \sqrt{3} \tag{6.47}$$

Uncontrolled Converters with a Zig Zag Winding Transformer

Although, no transformer is needed for the above configuration but it has several demerits. Since full load current flows in the neutral and only unidirectional current flows in each phase (from the

supply or distribution transformer), therefore this configuration is of theoretical interest only. However with the help of a special zig zag transformer (with double secondary windings), the above-mentioned demerits are removed and the cost of system increases due to special transformer. There are two secondary windings for each phase (Fig. 6.20). These windings are connected such that

$$\bar{V}_A = \bar{V}_{A1} + \bar{V}_{C2}, \quad \bar{V}_B = \bar{V}_{B1} + \bar{V}_{A2}, \quad \bar{V}_C = \bar{V}_{C1} + \bar{V}_{B2} \tag{6.48}$$

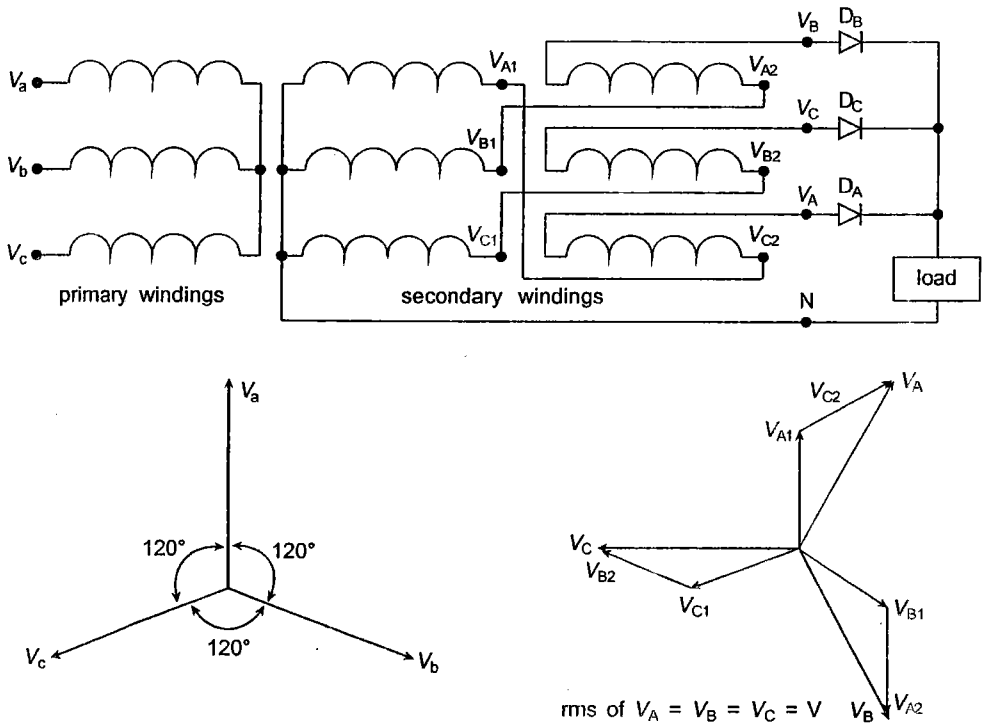


Figure 6.20 A three-phase, three-pulse, uncontrolled converter using a zig-zag winding transformer.

As discussed in the previous case, the diode with of highest anode voltage conducts for a period of 120°. However in this case, at the secondary terminal A, the current flows in both A_1 and C_2 windings. Therefore, the current flows in both primary windings of phase *a* as well as phase *c*. Since one of the secondary winding (C_2), is connected in reverse direction, the corresponding current in primary winding of phase *c* will be negative. Each phase current has an equal magnitude of positive-half and negative-half current in each cycle. Thus dc magnetization of the core of transformer is avoided. The average dc output voltage is given by

$$V_o = \frac{\sqrt{2}V_A \sin(\pi/3)}{\pi/3} = \frac{3\sqrt{3}}{\sqrt{2}\pi} V_A = \frac{9}{\sqrt{2}\pi} V_{A1} \tag{6.49}$$

where

$$\bar{V}_A = \bar{V}_{A1} + \bar{V}_{C2} \quad \text{and} \quad |V_A| = 2V_{A1}\cos\frac{\pi}{6} = \sqrt{3}\,V_{A1}$$

Six-pulse, Mid-point, Uncontrolled Converters

If all the six secondary windings of the zig zag transformer are connected with a common neutral, as shown in Fig. 6.21, the output will have six voltage pulses. The average value of the output voltage is given by

$$V_o = \frac{\sqrt{2}V_{A1}\sin(\pi/6)}{\pi/6} = \frac{3\sqrt{2}}{\pi}V_{A1} \tag{6.50}$$

where $V_{A1} = V_{A2} = V_{B1} = V_{B2} = V_{C1} = V_{C2} = V$. In this case, the output dc voltage reduces, because the ac voltage of each secondary winding is equal to V_{A1} only (where $V_{A1} < V_A$).

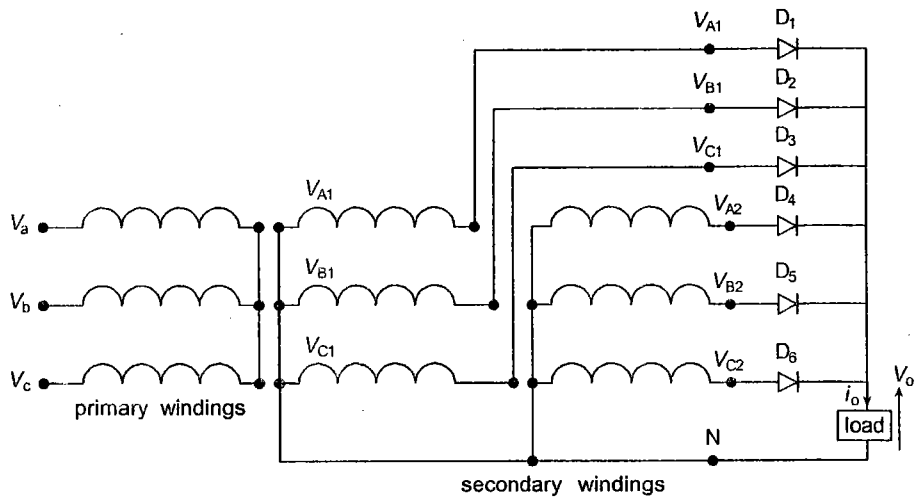
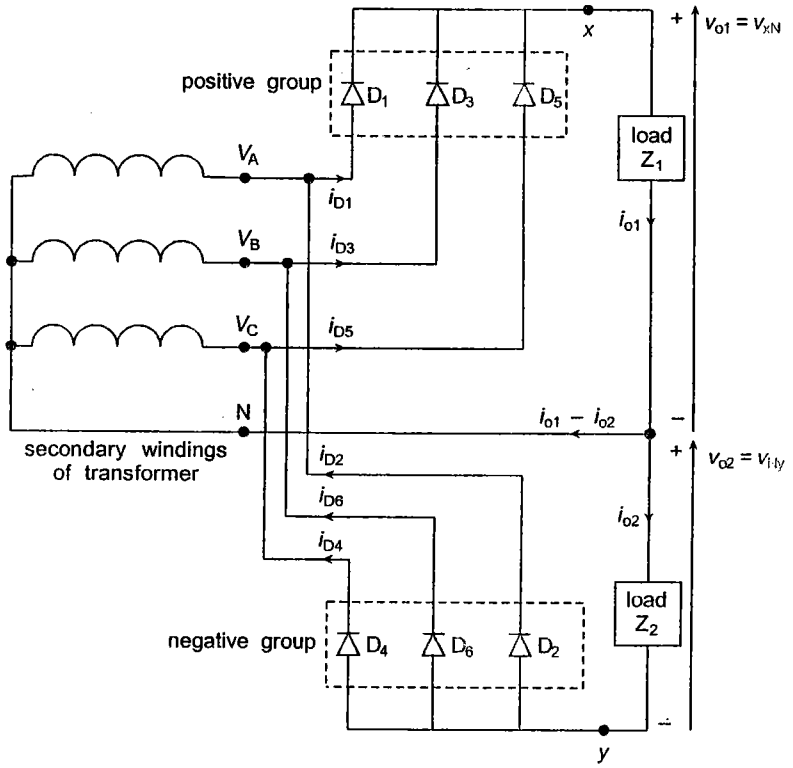


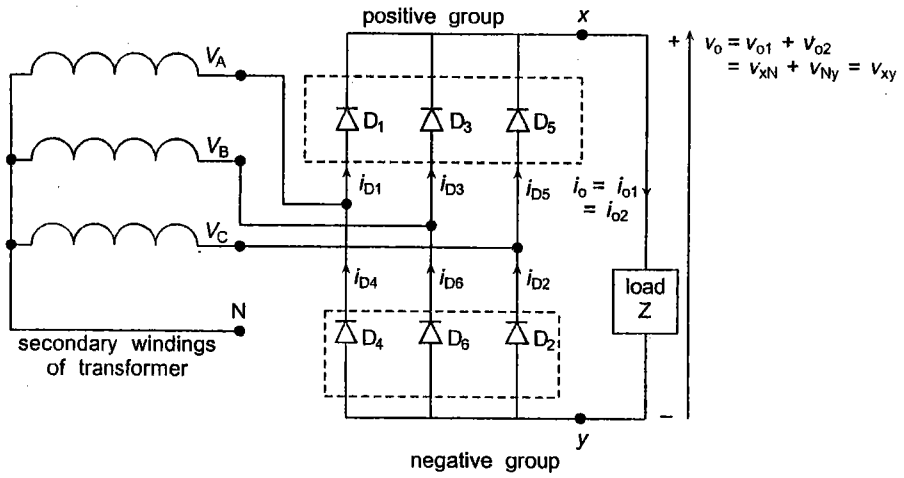
Figure 6.21 A three-phase, six-pulse, uncontrolled converter using a zig-zag winding transformer.

Six-pulse, Full-wave, Uncontrolled Converters

In the previous six-pulse converter, a six-winding transformer with a neutral connection is a must. In this case, the use of transformer can be avoided altogether. If two three-pulse converters are connected in forward and reverse modes (Fig. 6.22) and if the load impedances (Z_1 and Z_2) are same, then the neutral current (I_{o1}–I_{o2}) becomes zero. Therefore, there is no need of the neutral connection. Thus if the neutral wire is removed, the performance of the circuit does not change. Or in other words, with different values of the load impedances ($Z_1 \neq Z_2$) and removed neutral wire, both converters groups shall share the same dc current, as shown in Fig. 6.22b (it works even with one impedance). Since the output of each converter group has three pulses, the total number of pulses will be six. While three pulses of the positive-group correspond to the positive peaks of three-phase supply and three pulses of the negative group correspond to the negative peaks of the three-phase supply, as shown in Fig. 6.22c respectively. The output voltage (v_o) is the sum of v_{xN}

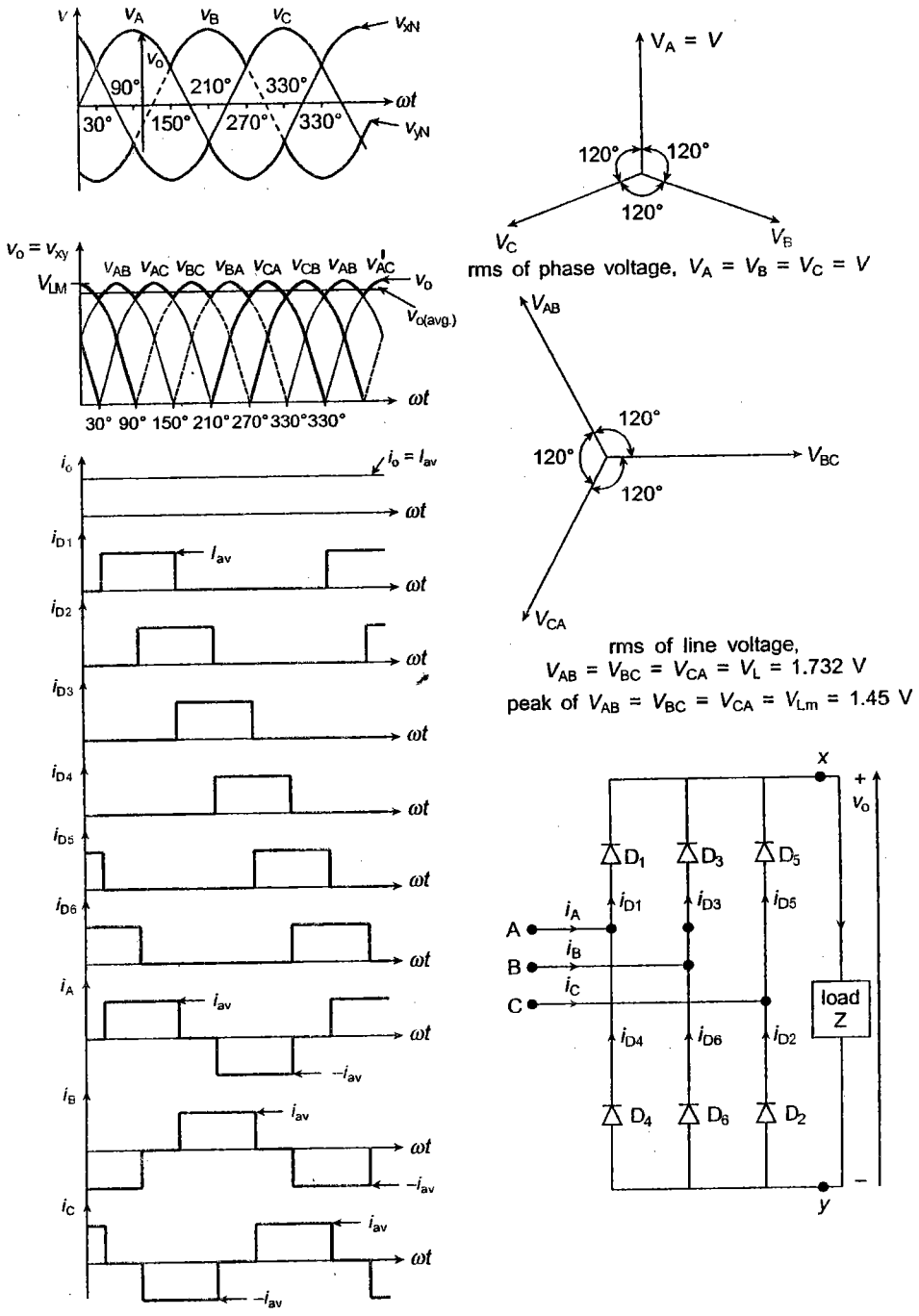


(a) Two three-pulse, half-bridge, uncontrolled converters form a full converter



(b) A three-phase, six-phase, full-bridge, uncontrolled converter

Figure 6.22 (*Cont.*)



(c) Waveform of a three-phase, six-pulse, uncontrolled converter

Figure 6.22 Two three-pulse converters connected in forward and reverse modes.

and v_{yN} due to the positive and negative groups, which corresponds to the rectified line voltage. Therefore,

$$v_o = v_{xN} - v_{yN} = v_{xN} + v_{Ny} = v_{xy} \tag{6.51}$$

The output voltage (v_o) is a floating voltage and it is with reference to y (not with reference to N). Both positive and negative half-cycles of each phase contribute the output voltage. There are six voltage pulses and NP (or switching points of diodes from which they start conduction). NP is the crossover point of the six line-voltage pulses. Now, NP is at 30° of each phase voltage and at 60° of each line voltage (as a line voltage is leading by 30° with respect to its phase voltage).

The average output voltage is twice of the three-pulse, uncontrolled converter, as given in (6.46). Therefore,

$$V_o = \frac{3\sqrt{6}}{\pi} V = \frac{3\sqrt{2}}{\pi} V_L = 1.36\, V_L = 2.34V \tag{6.52}$$

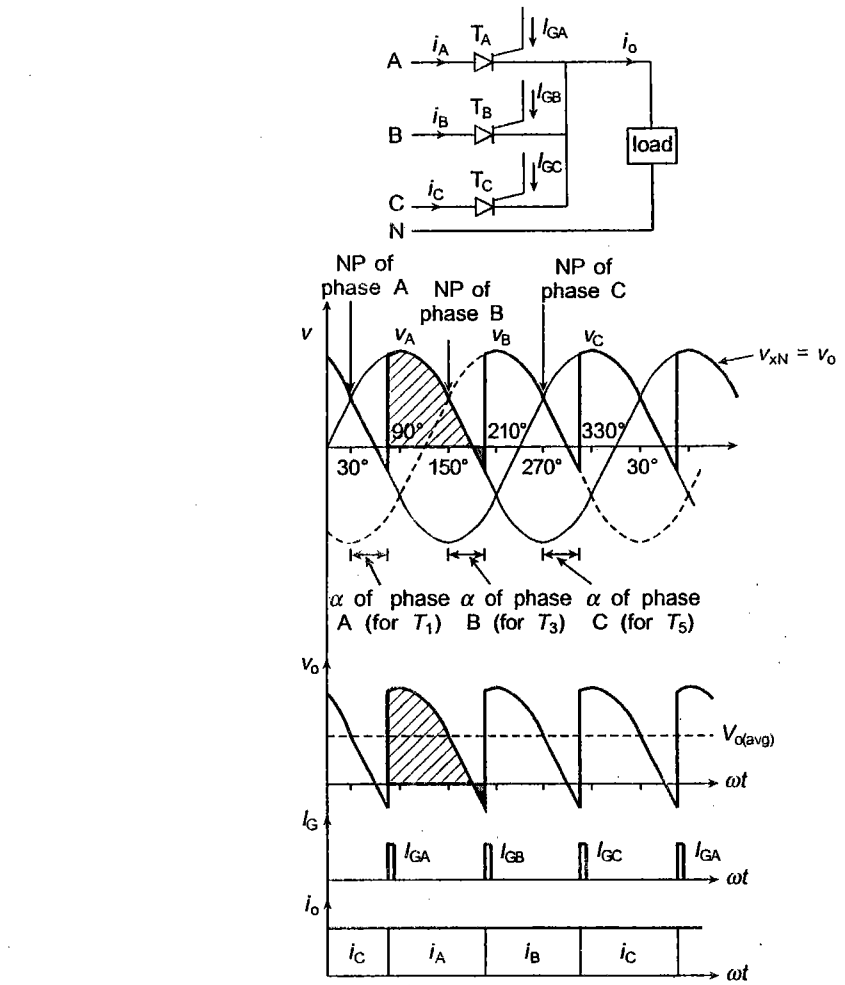
where V_L is line voltage. In this case, no neutral wire connection is necessary and two diodes always conduct. There are six ripples in each cycle and the line voltage appears across the load. Its frequency is six times of the mains frequency. Therefore, the requirement of components of filter circuit reduces and the ripples become minimum. Each diode conducts for 120° and experiences the peak of the line voltage, $V_{Lm} = \sqrt{6}$ V.

6.6.3 Three-phase, Controlled Converters

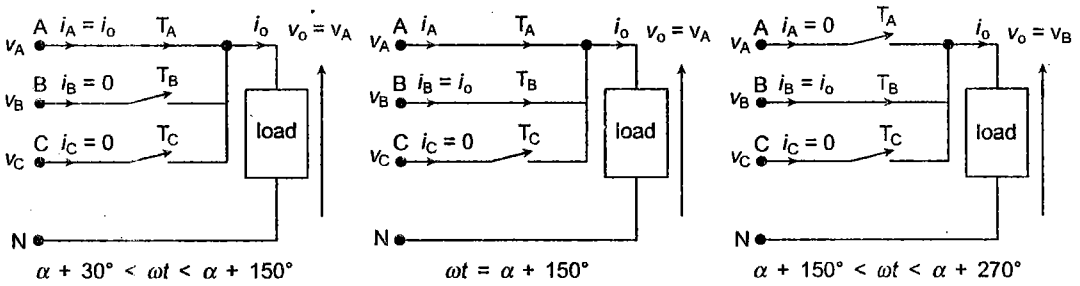
The applications of uncontrolled converters are limited due to lack of output voltage controllability. For high-power applications, three-phase controlled converters are extensively used. The performance resembles with their single-phase counterparts. Three-phase, semi-converters operate in the first quadrant of $v_o - i_o$ plane. While full-converters are able to be operated in the fourth quadrant, too, but only for active or *RLE* (–) loads. There are three and six voltage pulses (peak) in half-wave and full-wave converters, respectively. The use of three-phase, half-wave, controlled converters is limited. Because it introduces dc component in the input supply current which may result in core saturation of the distribution transformer. In comparison to single-phase system, here due to increased pulses (hence frequency of the output voltage pulses), the requirement of filter-circuit components reduces.

Three-pulse, Half-wave Converters

When all the diodes of a three-pulse, half-wave, uncontrolled converter (shown in Fig. 6.19), are replaced by thyristors (SCR), the converter becomes a half-wave, fully-controlled converter, as shown in Fig. 6.23a. The average output voltage is controllable with the help of switching angle (α), from positive maximum to zero [or up to negative maximum for active or *RLE* (–) loads]. Unlike the reference point of α, being the zero-crossover instant for single-phase systems, here the reference or natural point of α is the crossover point of voltage wave of two phases as shown in Fig. 6.17. Therefore, the NP for phase A, B and C are at ωt = 30°, 150° and 270°, respectively. Since there are three voltage pulses, NP for each phase is displaced by 120°. In case of uncontrolled converters, transfer of current takes place at each NP or crossover point of phase voltages. However, in this case, the conduction of a thyristor continues until the load current continues to flow or the other thyristor commutates it. When T_1 is triggered at $\omega t = \alpha + 30°$, the



(a) Waveforms of a three-phase, three-pulse, uncontrolled converter.



(b) Switching mechanism of a three-pulse, uncontrolled converter.

Figure 6.23 Three-pulse, half-wave converters.

phase voltage v_A reaches to the load (Fig. 6.23b). The thyristor acts as a mechanical switch and v_o is same as v_A. Since the conduction of thyristor continues up to $\alpha + 150°$, even negative voltage reaches to the load (as commutation does not take place at $\omega t = 180°$ due to inductive current). At $\omega t = \alpha + 150°$, current transfers from T_1 to T_3 and T_3 applies a positive voltage at the cathode of T_1 to commutate it. In fact this voltage is a negative line voltage ($v_A - v_B = v_{AB}$) which appears across T_1.

The average output voltages for an n-phase, half-wave, controlled converter with continuous load current is given by

$$V_o = \frac{\sqrt{2}\,V}{2\pi/n} \int_{\alpha-(\pi/n)}^{\alpha+(\pi/n)} \cos \omega t \, d(\omega t)$$

$$= \frac{\sqrt{2}V \sin(\pi/n)}{\pi/n} \cos \alpha$$

$$= \sqrt{2}V \frac{3\sqrt{3}}{2\pi} \cos \alpha$$

$$= 1.17V \cos \alpha \qquad (6.53)$$

The maximum and the normalized values are given by

$$V_{o(max)} = \frac{3\sqrt{6}}{2\pi} V = 1.17V \quad \text{and} \quad V_{on} = \cos \alpha \qquad (6.54)$$

For $0 < \alpha < 30°$, the instantaneous value of the output is always positive (hence $V_o > 0$) and the load current is continuous for passive R and RL loads. For highly inductive load, $V_o = 0$ at $\alpha = 90°$. Therefore, for $\alpha > \pi/2$, the load current falls to zero and it becomes discontinuous (because the impedance angle, $\phi > \alpha$, and a continuous load does not flow). The average value of the output voltage is given by

$$V_o = \frac{1}{2\pi/3} \int_{\alpha+(\pi/6)}^{\pi} \sqrt{2}V \sin \omega t \, d(\omega t)$$

$$= \frac{\sqrt{2}V}{2\pi/3}\left[1 + \cos\left(\alpha + \frac{\pi}{6}\right)\right], \qquad \frac{\pi}{6} \le \alpha \le \frac{5\pi}{6} \qquad (6.55)$$

For a resistive load, when $\alpha > 30°$, the load voltage becomes a discontinuous sinusoidal voltage with three pulses. Each thyristor commutates at the negative zero-crossover of the phase-voltage (when the load current becomes ideally zero or less than the holding current of the thyristor).

Three-pulse, Half-wave Converters with a Freewheeling Diode

Just like a single-phase system, the freewheeling diode prevents the instantaneous value of the load voltage to become negative. Therefore, V_o is always positive and power inversion is not possible for active or RLE (–) loads. For $0 \le \alpha \le 30$, no freewheeling action takes place, as output voltage (v_o) is always positive. Therefore, V_o is same as in the previous case given in (6.53). A discontinuous output voltage, due to freewheeling action, appears when $\alpha > 30°$. The commutation of each thyristor takes place at negative zero-crossing of each phase (e.g. $\omega t = 180°$

for phase A). V_o is same as given in (6.55). The maximum value of α is 150° because at that condition $\omega t = \alpha + 30° = 180°$. At this instant, $v_A(\omega t) = 0$ and beyond this, v_A becomes negative. Therefore, triggering of thyristors is not possible.

SIX-PULSE, FULL-WAVE CONVERTERS

When all the diodes of a six-pulse, full-wave, uncontrolled converter (Fig. 6.22), are replaced by thyristors, it becomes a full-wave, fully-controlled converter, as shown in Fig. 6.24a. It is similar to a single-phase system discussed earlier. Here each thyristor is switched at an interval of 60° sequentially, from T_1, T_2, ..., T_6. (They are purposely numbered properly for a bridge configuration.) When T_1 and T_2 is conducting v_{AN} and v_{BN} voltage with respect to star point of transformer appears at the load, i.e. $v_{AN} = v_{XN}$ and $v_{BN} = v_{YN}$. The load voltage, $v_o = v_{XY} = v_{AN} - v_{BN} = v_{AB}$, which is the line voltage V_L (where $V_L = \sqrt{3}\,V$, $V_{Lm} = \sqrt{2}\,V_L$ and V is the rms value of the phase voltage). When $\omega t = \alpha + 90°$, T_2 is triggered. At this condition, v_C is more negative than v_B, therefore due to conduction of T_2, v_Y (negative bus) becomes equal to v_C (Fig. 6.24b). Thus a more negative voltage appears at the anode of T_6 to make it reverse biased. Then T_6 commutates and the load current transfers from T_6 to T_2. Again, when T_3 is triggered it supplies a positive (higher) voltage ($v_B > v_A$) at the cathode of T_1 to turn it off and the load current transfers from T_1 to T_3. There are six voltage pulses and the instantaneous output voltage (v_o) becomes negative for an inductive *RL* load. However, V_o is always positive except for active or *RLE*(–) loads where the converter is able to operate in the fourth quadrant of $v_o - i_o$ plane. Since each voltage pulse corresponds to the line voltage and it appears with one-sixth period of a cycle ($2\pi/6$). Therefore, the average output voltage, corresponding to the line voltage, v_{AB} for (1/6)th of a cycle, is given by

$$V_o = \frac{1}{2\pi/6}\int_{\alpha+(\pi/6)}^{\alpha+(\pi/2)} \sqrt{2}V_L \sin\left(\omega t + \frac{\pi}{6}\right) d(\omega t)$$

$$= \frac{3\sqrt{6}V}{\pi}\cos\alpha$$

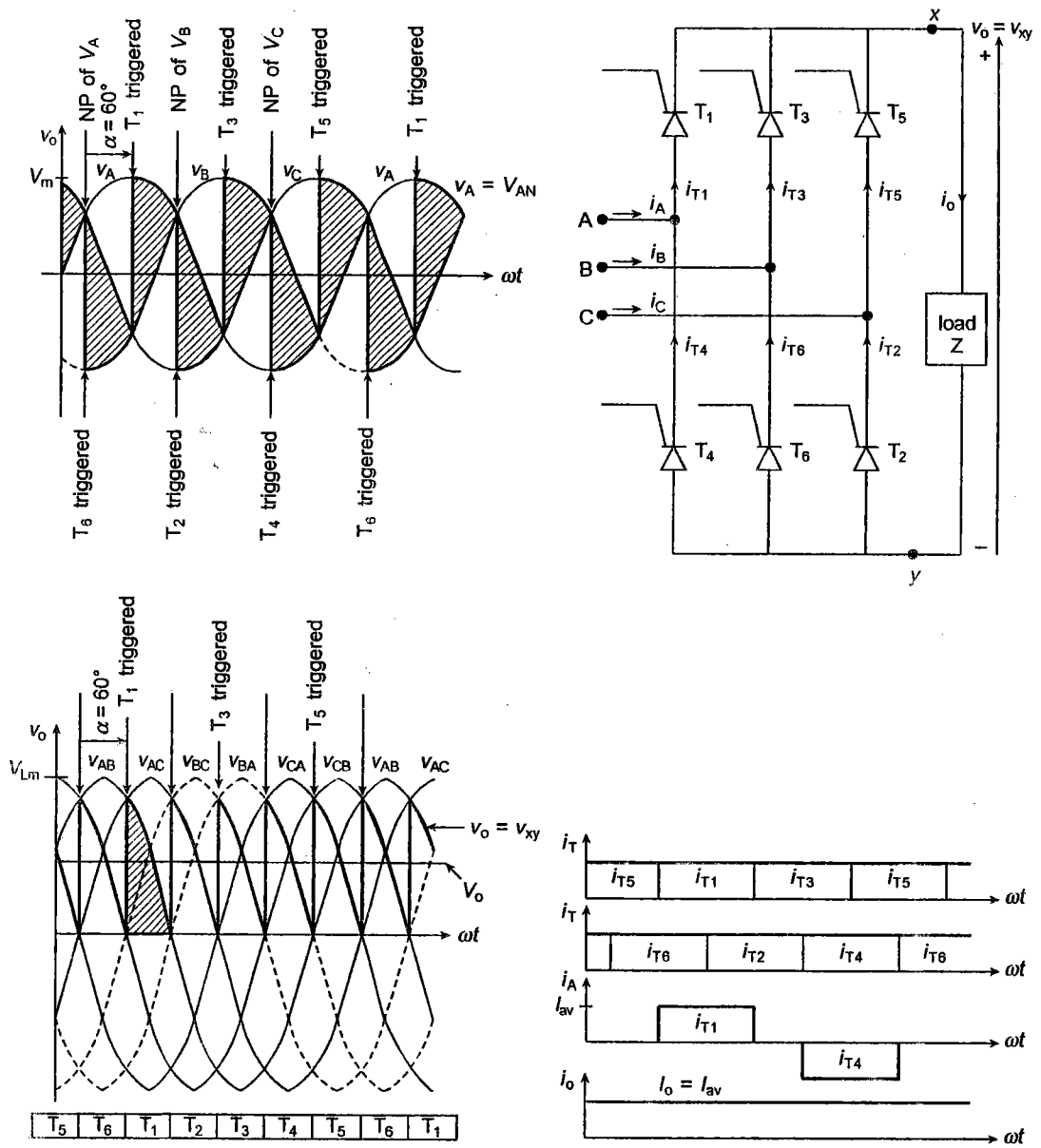
$$= 2.34\cos\alpha \qquad (6.56)$$

The maximum and normalized values are given by

$$V_{o(max)} = \frac{3\sqrt{6}}{\pi}V \quad \text{and} \quad V_{on} = \frac{V_o}{V_{o(max)}}\cos\alpha = \cos\alpha \qquad (6.57)$$

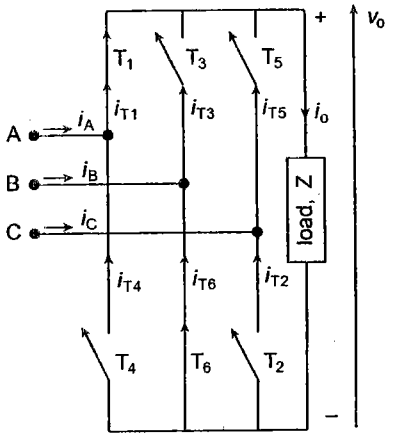
It is evident from Fig. 6.24c that the instantaneous output voltage (v_o) is continuous (non-zero) for $\alpha < 60°$, therefore, for any passive load (*R*, *RL* etc.), the load current is continuous. For $\alpha = 90°$, V_o is zero for a highly-inductive *RL* load. Thereafter, for $\alpha > 90°$, the load current becomes discontinuous and the output voltage (average value) remains positive for passive loads. The performance of converter with different loads and the value of α are given as follows:

For $\alpha \le 60°$: $v_o \neq 0$, i_o continuous for any passive load.
For $60° \le \alpha \le 90°$: continuity of i_o depends on ϕ (discontinuous for *R* load, or $\phi = 0$).
For $\alpha \ge 90°$: i_o always discontinuous for passive loads, $V_o > 0$.
For $\alpha \ge 90°$: Only for active or *RLE*(–) loads, operates in fourth quadrant ($V_o \le 0$, may be continuous).

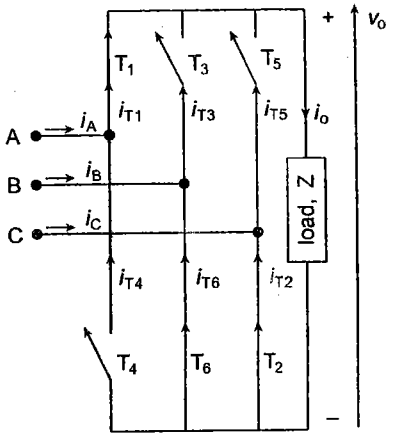


(a) Waveforms of a three-phase, full-wave, six-pulse controlled rectifier for α = 60°

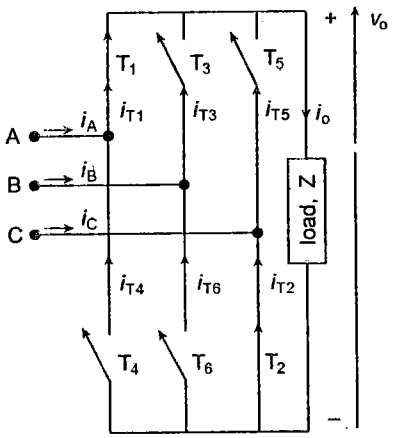
Figure 6.24 (*Cont.*)



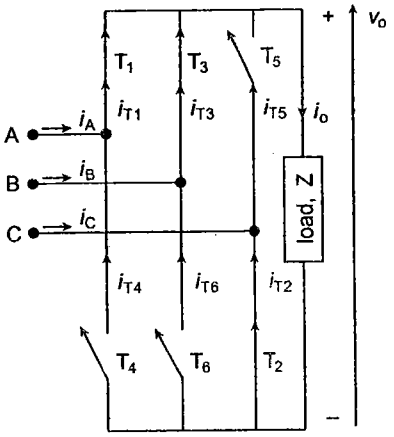
(i) $\omega t > \alpha + 30°$ (T_1 and T_6 conducting)



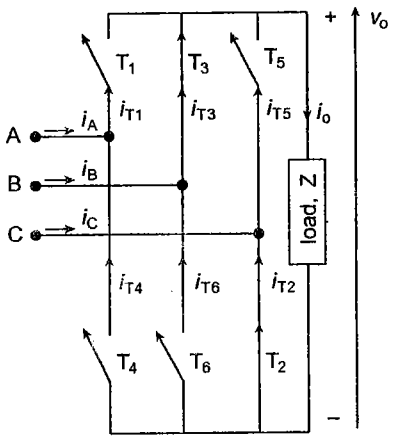
(ii) $\omega t = \alpha + 90°$ (T_2 triggered)



(iii) $\omega t > \alpha + 90°$ (T_1 and T_2 conducting)



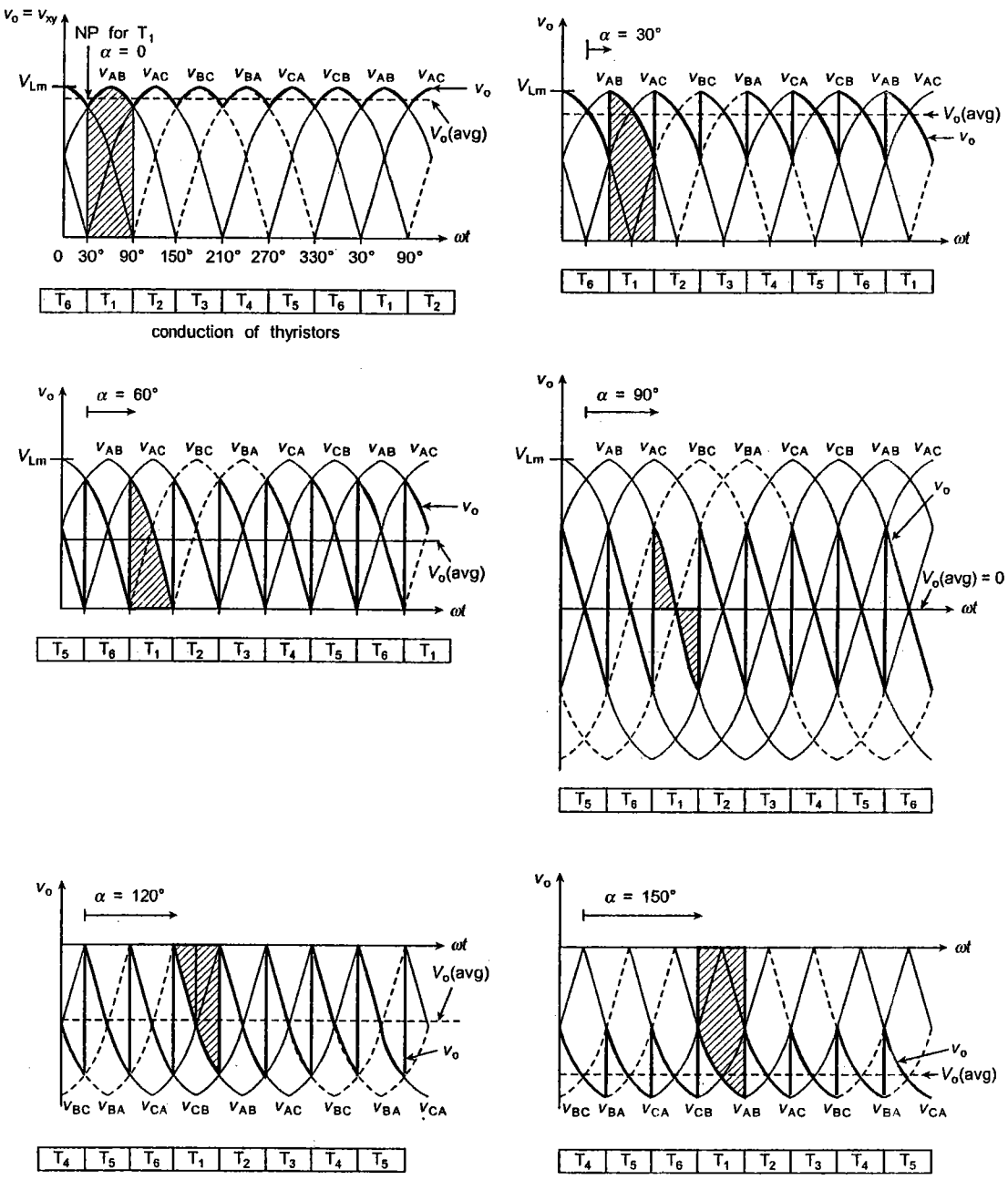
(iv) $\omega t = \alpha + 150°$ (T_3 triggered)



(v) $\omega t > \alpha + 150°$ (T_2 and T_3 triggered)

(b) Switching mechanism of a three-phase, full-wave, six-pulse, controlled converter bridge

Figure 6.24 (*Cont.*)



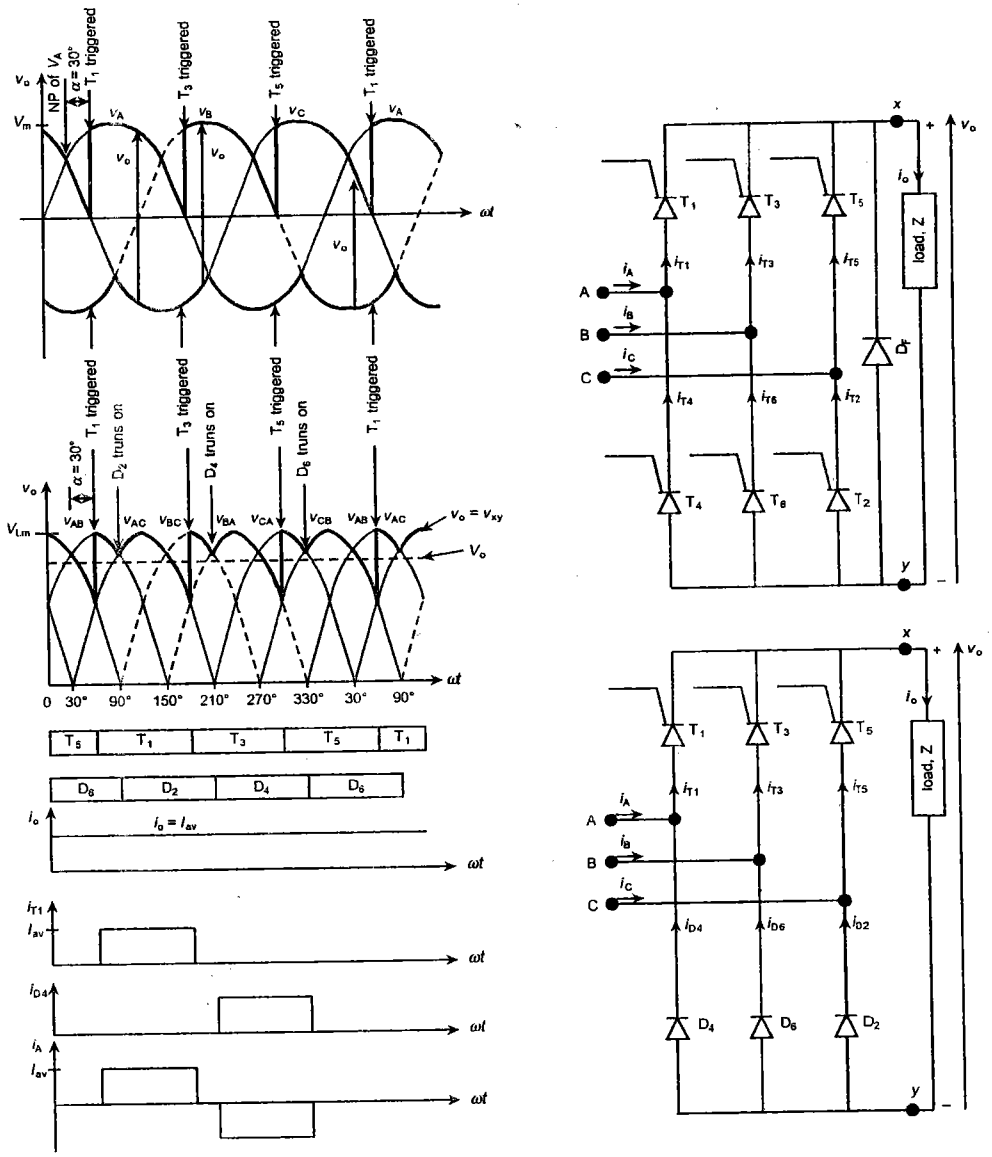
(c) Output voltage of three-phase, six-pulse, full converters

Figure 6.24 Six-pulse, full-wave converters.

The converter operates in the first quadrant of v_o–i_o plane only. However, for an active or *RLE* (–) load, it is able to operate in the forth quadrant of v_o–i_o plane (Fig. 6.24c). Figure 6.24b shows the mechanism of switching of devices for a given value of α.

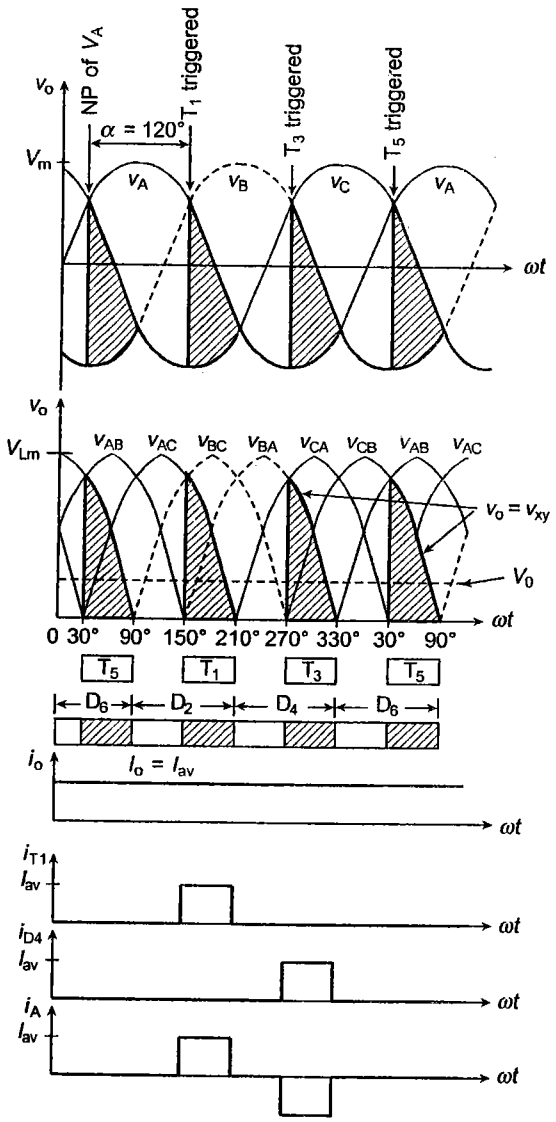
THREE-PHASE, SEMI-CONVERTERS

If a freewheeling diode is connected at the output of the converter (Fig. 6.24), it becomes a semi-converter, as shown in Fig. 6.25. The instantaneous value of the output voltage is always positive



(a) Waveforms of a three-phase, half-controlled rectifier for α = 30°

Figure 6.25 (*Cont.*)



(c) Waveforms of a three-phase, half-controlled rectifier for α = 120°

Figure 6.25 Three phase, semi-converters.

for all passive loads. In this case, the power factor is high as no power inversion from a load to a source takes place. The converter always operates in the first quadrant of the $v_o - i_o$ plane. There are other configurations, where instead of six thyristors and one freewheeling diode, three thyristors and three diodes are used. In this case, freewheeling action takes place when anode of conducting SCR becomes negative. Thus cathode of the diode connected to it, becomes forward biased, then conducts and freewheeling operation takes place with the conducting SCR. The conduction continues till the next thyristor is triggered.

6.7

EFFECT OF SOURCE IMPEDANCE (OR OVERLAP)

Up till now, the effect of the impedance of ac source was neglected and it was assumed that the current transfers immediately from one diode/thyristor to other. However, due to the presence of inductive reactance of the ac source (e.g. distribution transformer leakage reactance), the current takes a finite time to reduce to zero (to commutate the outgoing devices). Similarly, the current takes a finite time to rise in the coming conducting device (during turning on). Let a three-phase, half-wave converter is connected to a three-phase transformer. A highly-inductive load is connected with the converter such that a ripple-free load current flows and $I_o = I_{av}$. The source inductance of each phase are X_A, X_B and X_C, where $X_A = X_B = X_C$. Let T_A is conducting and T_B is turned on at the switching angle, α (Fig. 6.26). The difference of the phase voltage ($v_B - v_A$), appears across the reactances X_A and X_B, and a circulating current flows between the two thyristors. This interval, in which both the thyristors conduct, is called *overlap* period. Neglecting

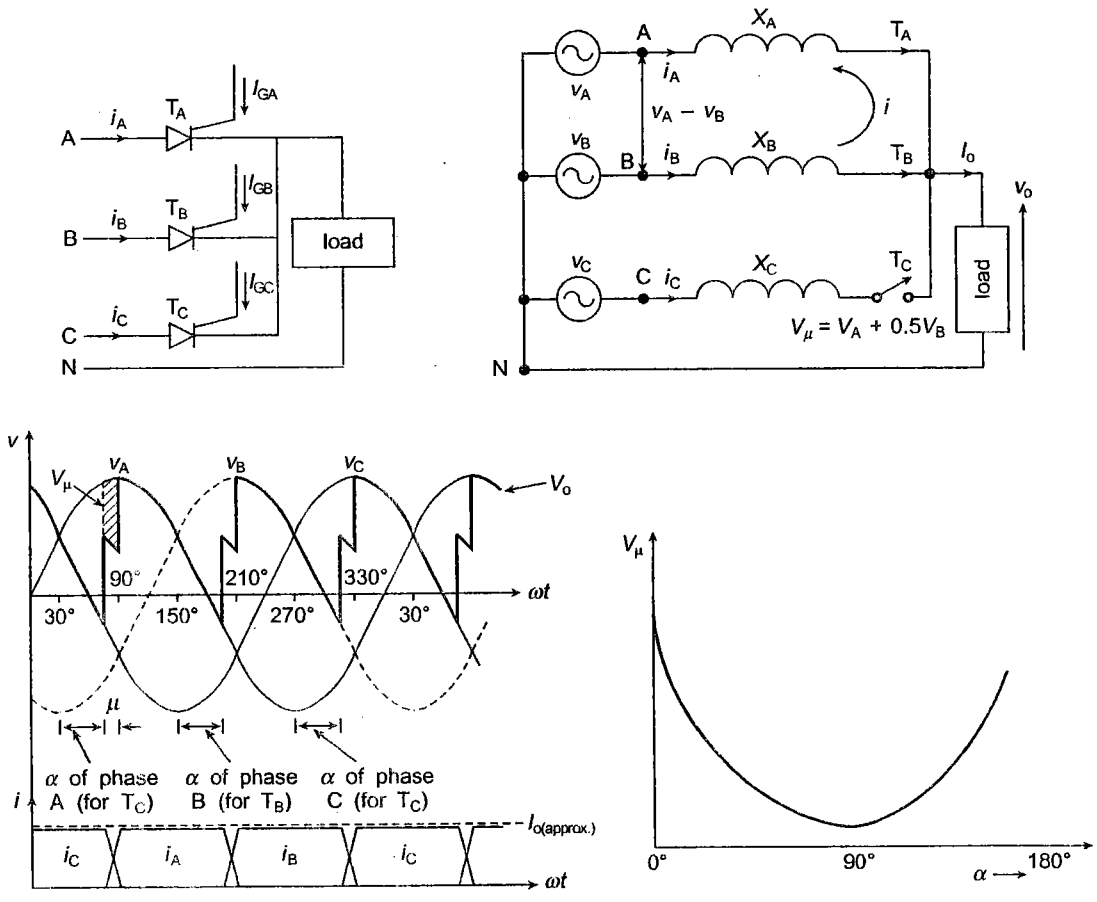


Figure 6.26 Overlap in three-phase system.

the source resistance and the voltage drop across these thyristors, the voltage drop across these inductances is given by

$$\Delta v = 2L_A \frac{di}{dt} \tag{6.58a}$$

where L_A is the leakage inductance and $L_A = L_B$. At the switching instant, the line voltage appears across these reactances. Therefore,

$$\Delta v = \sqrt{3}\sqrt{2}\, V \sin(\omega t + \alpha) \tag{6.58b}$$

Equating these equations (6.58a and b) and integrating for i, yields

$$i = \frac{\sqrt{6}V}{2\omega L_A}[\cos\alpha - \cos(\omega t + \alpha)] \tag{6.59}$$

where at $\omega t = \alpha$, commutation begins and at $\omega t = \alpha + \mu$, commutation completes. Also this instant, $i = i_B = I_{av}$. From (6.59), it gives

$$\cos\alpha - \cos(\mu + \alpha) = \frac{2\omega L_A I_{av}}{\sqrt{6}V}$$

Therefore, the commutation angle,

$$\mu = \cos^{-1}\left(\cos\alpha - \frac{2\omega L_A I_{av}}{\sqrt{6}V}\right) - \alpha \tag{6.60}$$

During the commutation or overlap period (μ), the supply voltage appears across the source inductances. The output voltage is mid-point voltage of the inductance, which is given by

$$v_o = v_2 + \frac{1}{2}(v_1 - v_2) = \frac{1}{2}(v_1 + v_2)$$

V_μ is the average dc voltage loss due to overlap for each output voltage (here three-pulse). Therefore,

$$V_\mu = \frac{3}{2\pi}\int_{\alpha}^{\alpha+\mu} \frac{1}{2}(v_B - v_A)\, d(\omega t)$$

$$= \frac{3}{2\pi}\int_{\alpha}^{\alpha+\mu} \frac{1}{2} v_L\, d(\omega t)$$

$$= \frac{3}{4\pi}\int_{0}^{\mu} \sqrt{3}\sqrt{2}\, V \sin(\omega t + \alpha)\, d(\omega t) \quad \text{(reference is changed by } \alpha\text{)}$$

$$= \frac{-3\sqrt{3}\sqrt{2}V}{4\pi}[\cos(\mu + \alpha) - \cos\alpha]$$

$$= L_A I_{av} \frac{3\omega}{2\pi} \quad \text{(from 6.59)}$$

The loading or reduction in dc output voltage is given by

$$V_{o\mu} = V_o - V_\mu$$

$$\left.\begin{aligned} &= \frac{3\sqrt{6}}{2\pi}\cos\alpha - L_A I_{av}\frac{3\omega}{2\pi} && \text{(for 3-pulse converters)} \\ &= \frac{3\sqrt{6}V}{\pi}\cos\alpha - L_A I_{av}\frac{3\omega}{\pi} && \text{(for 6-pulse converters)} \\ &= \frac{2\sqrt{2}V}{\pi}\cos\alpha - L_A I_{av}\frac{\omega}{\pi} && \text{(for 2-pulse converters)} \end{aligned}\right\} \quad (6.61)$$

The commutation time is inversely proportional to the commutation voltage (Δv). As α increases, Δv increases and μ decreases. However, Δv increases to its maximum and μ reduces to a minimum at $\pi/2$. The maximum value of μ lies at $\alpha = 0$ and near $\alpha = \pi$ (Fig. 6.26). For n-pulse, it is given by

$$\mu_{max} = \cos^{-1}\left[\frac{\omega L_A I_{av}}{\sqrt{2}\,V\sin(\pi/n)} - 1\right]$$

$$= \cos^{-1}\left(\frac{2\omega L_A I_{av}}{\sqrt{2}\sqrt{3}V} - 1\right)$$

$$= \cos^{-1}\frac{2\omega L_A I_{av}}{\sqrt{2}V} \qquad \text{(for 6-pulse converters)} \quad (6.62)$$

The magnitude of μ_{max} also depends upon the load current. The overlap angle is more important in inverter operation. It gives the range of control. The maximum value of α is given by

$$\alpha_{max} = 180° - (\mu_{max} + \gamma) \quad (6.63)$$

where t_q is the thyristor turns-off time and $\gamma = \omega t_q$.

Example 6.6 A three-phase, six-pulse, full converter is connected to a three-phase, 50 Hz, 220 V, Y-connected supply. The load resistance and inductance are 10 Ω and 1 H, respectively. For $\alpha = 30°$, find the following:

(a) the average output voltage, V_o, (b) the average output current, I_o, (c) the output (rms) current , $I_{o(rms)}$, (d) the average output power, P_o, (e) the average thyristor (SCR) current, $I_{T(avg)}$ and (f) the voltage rating of thyristors.

Solution The load impedance,

$$Z = R + j2\pi fL = 10 + j2\pi \times 50 \times 1 = (10 + j314.1)\ \Omega$$

The impedance angle,

$$\phi = \tan^{-1}\frac{314.1}{10} = 88.17°$$

Since the load is highly inductive, we get the average output voltage,

$$V_o = V_{on} \cos \alpha = \frac{3\sqrt{6}\,V}{\pi} \cos \alpha$$

The phase voltage,

$$V = \frac{220}{\sqrt{3}} = 127 \text{ V}$$

(a) $V_{o(av)} = \dfrac{3\sqrt{6} \times 127}{\pi} \cos 30° = 257.45 \text{ V}$

(b) $I_{o(av)} = \dfrac{V_{o(av)}}{R} = \dfrac{257.45}{10} = 25.74 \text{ A}$

(c) Due to a highly-inductive current, the load current is ripple free (constant magnitude). Therefore, $I_{o(rms)} = I_{o(av)} = 25.74$ A.

(d) $P_o = I^2_{o(av)}\, R = I^2_{o(rms)} R = (25.74)^2 \times 10 = 6.625$ kW

(e) $I_{T(av)} = I_{o(av)}/3 = 8.58$ A

(f) $I_{T(rms)} = I_{o(av)}/\sqrt{3} = 25.74/\sqrt{3} = 14.86$ A

(g) The peak inverse voltage (PIV) across the thyristor is the maximum value of the line voltage,

$$V_{Lm} = \sqrt{2} \times V_L = \sqrt{2} \times 220 = 311.1 \text{ V}$$

Example 6.7 An armature circuit (*RLE* load) of a separately excited dc motor is fed from a three-phase, six-pulse, fully-controlled converter. The input ac voltage (line) = 148 V, $R_a = 0.06\ \Omega$, $L_a = 0.85$ mH, I_a (rated) = 150 A, V_a (rated) = 200 V. Find the output voltage and α, when

(a) $E = 160$ V at the rated load torque

(b) $E = 160$ V at 200% of the rated load torque

(c) $E = -109$ V at 200% of the rated load torque.

Solution (a) The voltage equation of dc circuit is given by

$$V_a = E + I_a R_a = 160 + 150 \times 0.06 = 169 \text{ V}$$

For continuous load current, V_o is given by

$$V_o = \frac{3\sqrt{2}V_L}{\pi} \cos \alpha = V_a$$

where

$$\cos \alpha = \frac{169\pi}{3\sqrt{2} \times 148} = 0.845 \quad \text{and} \quad \alpha = 32.3°$$

(b) At this condition, $I_a = 2 \times 150 = 300$ A. Then

$$V_a = E + I_a R_a = 160 + 300 \times 0.06 = 178 \text{ V}$$

where

$$\cos\alpha = \frac{178\pi}{3\sqrt{2} \times 148} = 0.89 \quad \text{and} \quad \alpha = 27.1°$$

(c) $V_a = -109 + 300 \times 0.06 = -91$ V. Then motor operates in fourth quadrant and

$$\cos\alpha = \frac{-91\pi}{3\sqrt{2} \times 148} = -0.455 \quad \text{and} \quad \alpha = 117°$$

Example 6.8 A three-phase, six-pulses full converter is connected with a 400 V, three-phase input voltage supply. A highly inductive *RL* load (10 Ω) is connected at the output. Find PF and THD of the converter for $\alpha = 30°$.

Solution Let the load current be ripple-free continuous current. Then, from the Fourier series, for the input current,

$$a_n = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)(\cos n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\int_0^{\pi} I_{av}(\cos n\omega t)\, d(\omega t) \qquad \text{(due to symmetry of both half cycles)}$$

$$= \frac{2}{\pi}\int_{\alpha+(\pi/6)}^{\alpha+(5\pi/6)} I_{av}(\cos n\omega t)\, d(\omega t)$$

$$= \frac{-4I_{av}}{n\pi}\sin\frac{n\pi}{3}\sin n\alpha \qquad \text{for } n = 1, 3, 5, \ldots$$

$$= 0, \qquad \text{for } n = 2, 4, 6, \ldots$$

and

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)(\sin n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi}\int_0^{\pi} I_{av}(\sin n\omega t)\, d(\omega t)$$

$$= \frac{4I_{av}}{n\pi}\sin\frac{\pi n}{3}\cos n\alpha, \qquad \text{for } n = 1, 3, 5, \ldots$$

$$= 0 \qquad \text{for } n = 2, 4, 6, \ldots$$

The rms value of the nth harmonic is given by

$$I_n = \frac{\sqrt{a_n^2 + b_n^2}}{2} = \frac{2\sqrt{2}}{n\pi} I_{av}\sin\frac{n\pi}{3}$$

Also,

$$\phi_n = \tan^{-1}\frac{a_n}{b_n} = \tan^{-1}(-\tan n\alpha) = -n\alpha$$

The rms value of the input current,

$$I = \left[\frac{1}{\pi}\int_{\alpha+(\pi/6)}^{\alpha+(5\pi/6)} I_{av}^2\, d(\omega t)\right]^{1/2} = \sqrt{\frac{2}{3}}\, I_{av}$$

The rms value of the fundamental component of the input ac current is given by

$$I_1 = \frac{2\sqrt{2}}{n\pi} I_{av} \sin\frac{\pi}{3} = \frac{\sqrt{6}}{\pi} I_{av}$$

Therefore,

$$\text{PF} = \frac{I_1}{I}\cos(-\alpha) = \frac{3}{\pi}\cos 30° = 0.827$$

and

$$\text{THD} = \left[\left(\frac{I}{I_1}\right)^2 - 1\right]^{1/2} = \left[\left(\frac{\pi}{3}\right)^2 - 1\right]^{1/2} = 0.3108 \text{ or } 31.08\%$$

(*Note:* THD is independent of α as in case of single-phase full-converters for a ripple free continuous current.)

6.8 MULTIPLE CONVERTERS

There are limitations of controlled rectifier or converters. A semi-converter operates in the first quadrant of output $v_o - i_o$ characteristics while a full-converter may operate in the fourth quadrant as well for active or *RLE* (–) loads. There are several converters, which are used for special applications. They are basically combinations of half-controlled or fully-controlled converters. For example, when direction of both output voltage and output current is to be reversed, a dual converter (parallel type) is used. For improvement of PF and reducing THD, sequence control or series (dual or multiple) converters are used. Following types of multiple converters are common.

(a) Parallel dual converters
  (i) non-circulating current type
  (ii) circulating-current type

(b) Series multiple-stage converters
  (i) using semi-converter bridges
  (ii) using full-converter bridges

These multiple converters may be a single-phase type or a three-phase type.

6.8.1 Single-phase, Parallel Dual Converters

In case of a half-controlled converter, both load voltage (v_o) and load current (i_o) are non-reversible. Therefore, the operation of converters is restricted to the first quadrant of $v_o - i_o$ plane only. In case of a fully-controlled converter, it is only the output voltage (average value) that is reversible. Thus, the converters may operate in the first and the fourth quadrants only. However, the direction of the load current remains same (as the current through the SCR, i_A is non-reversible). If two fully-controlled converters are connected back-to-back (anti-parallel across the load), this arrangement is called a *dual converter*. Thus, parallel type dual converters are able to operate in all the four quadrants of the $v_o - i_o$ plane, as shown in Fig. 6.27. The converter-1 is able to operate in both I and IV quadrants while the converter-2 may operate in both II and III quadrants. These converters operate in two modes: non-circulating current type and circulating current type.

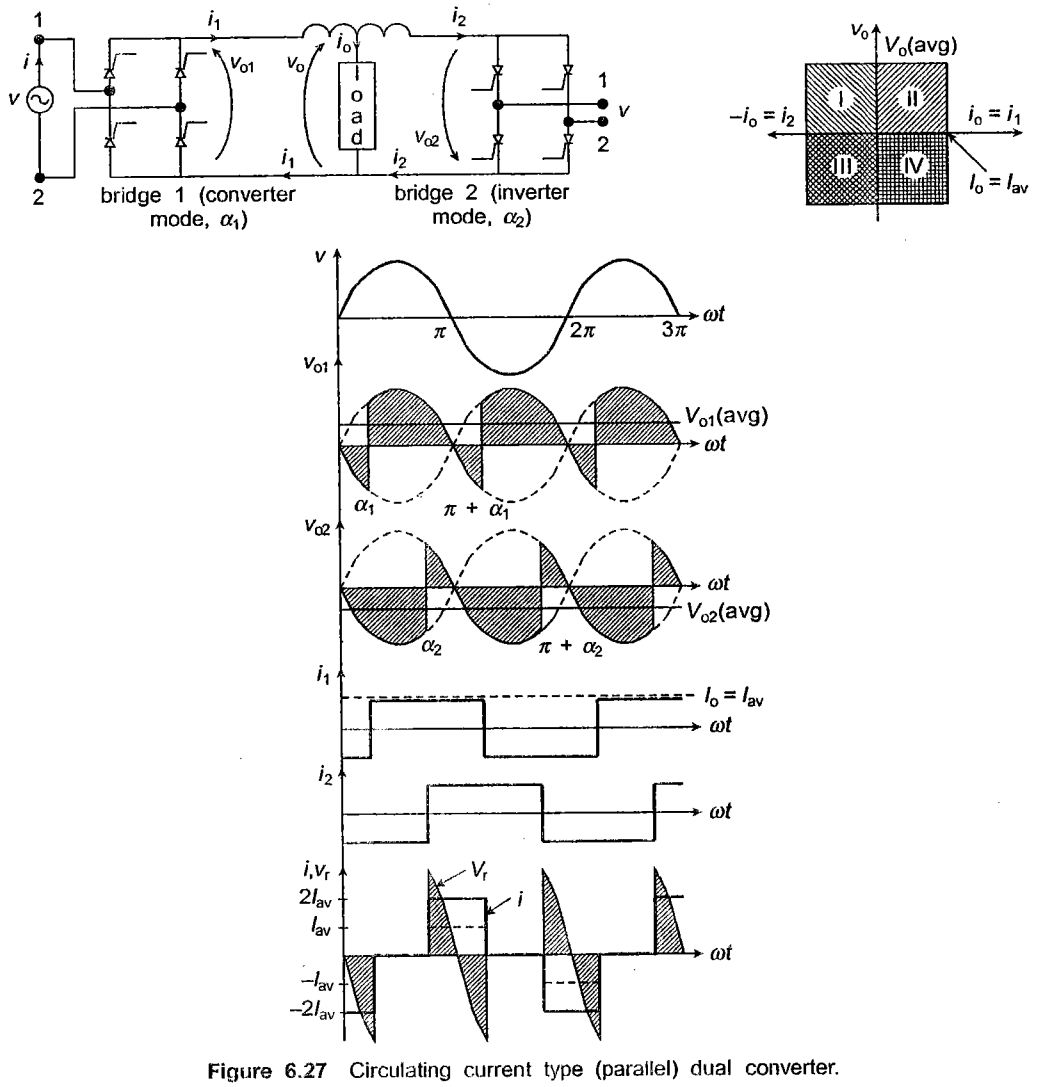


Figure 6.27 Circulating current type (parallel) dual converter.

Non-circulating current type In this case, only one converter operates at a time. Since each bridge is a full-converter, it can operate in the first as well as in the fourth quadrant. Thus, converter-1 operates in I or IV quadrant (with the same direction of load current). When the direction of the load current (i_o) is to be reversed (for II and III quadrant), the thyristors of converters-1 are switched off (by ceasing the gating signals). When the load current, i_o (or i_{o1}), becomes zero, after a blanking or delay period of about 10–20 ms, converter-2 is switched on by supplying the gate signals to its thyristors (otherwise the commutation failure of outgoing converter will cause a high-circulating current). The direction of the load current reverses and now $i_o = i_{o2}$. To avoid the conduction overlapping of the bridges (which may cause a short-circuit condition), a current limiting inductor is used with the load. The average output voltage is same that of the fully-controlled converters, i.e.

$$V_{o1} = \frac{2V_m}{\pi} \cos \alpha_1 \tag{6.64}$$

$$V_{o2} = \frac{2V_m}{\pi} \cos \alpha_2 \tag{6.65}$$

Circulating current type When fast changeover of the output voltage and current is required (without the blanking period), circulating current type control is used. In this mode, both the bridges conduct simultaneously. Since both converters are always on, change of operation from one quadrant to another is quick. The trigger pulses are supplied to all thyristors, whether the load current is present or not. The circulating current maintains the conduction of both converters, independent of the load conditions. Converter-1 operates in rectifier mode ($\alpha_1 < \pi/2$) and converter-2 operates in inversion mode ($\alpha_2 > \pi/2$) such that the average output voltage of each converter across the load remains equal. Therefore,

$$\alpha_1 + \alpha_2 = \pi \quad \text{or} \quad \alpha_2 = \pi - \alpha_1 \tag{6.66}$$

since,

$$V_{o2} = \frac{2V_m}{\pi} \cos \alpha_2 = \frac{2V_m}{\pi} \cos(\pi - \alpha_1) = -\frac{2V_m}{\pi} \cos \alpha_1 \tag{6.67}$$

we get,

$$V_o = V_{o1} = V_{o2}$$

Due to the absence of the blanking period, a quick reversal of the load voltage (average value) and the load current is possible and the control becomes fast. For reversing the direction of current, the first bridge is switched in inverter mode ($\alpha_1 > \pi/2$) and the second bridge in the rectifier mode ($\alpha_2 < \pi/2$). Although the average output voltages of both the converters are always equal but their instantaneous values (voltage) are different. Thus, a circulating current flows between the two converters as shown in Fig. 6.27. A current limiting inductor (reactor) is connected. The magnitude of the circulating current depends on the switching angle. At any time, the power flow from the source to the load (rectifier mode) and from load to source (inversion mode) is possible.

6.8.2 Three-phase Dual Converters

For large power applications, instead of single-phase dual converters, three-phase dual converters are used. Its performance as a dual converter is same as its single-phase counter part. However,

additional benefits of three-phase systems are achieved (e.g. low THD, balanced three-phase input line current, etc.). The same back-to-back parallel configuration is used. In case of non-circulating current type converters, the same control strategy is used, that is only one three-phase, full-converter operates at a time. For circulating-current type converters, each converter operates at α_1 and α_2 respectively such that $\alpha_1 + \alpha_2 = \pi$. As discussed in case of single phase system, the average of the output voltages is equal at load but their instantaneous values (v_{o1} and v_{o2}) are different. To limit the circulating current, an inductor is used. However, the ripple reduces drastically as the ripple-frequency becomes six times the power frequency. Three-phase dual (parallel type) converters are also used to increase number of output voltage pulses. Both converters are connected in parallel (not back-to-back) with the load. It is discussed in detail in the next section of this chapter.

6.8.3 Series Multiple-stage Converters

In this case, two or more converters are connected in series, such that the output voltage is sum of the their individual voltage (series connection). The bridges used in the series converters may be a semi-converter or a full-converter. This method of control is also called *sequence control*. Basically, these converters are used to improve the waveform of the output voltage and the input current. Since the output voltage and the input current waveforms become stepped, THD reduces and PF of the load improves. Normally, such converters are used for high voltage and high power applications, e.g. for speed control of dc traction motors.

Figure 6.28 shows a semi-converter based two-stage series converter. Since secondary windings have equal number of turns, their output voltages (ac) are same. Thus

$$v_1(\omega t) = v_2(\omega t) \quad \text{or} \quad v_1 = V_{m1} \sin \omega t = V_{m2} \sin \omega t$$

For the dc output voltage, from 0 to half of the maximum output voltage, $V_{o(max)}$, the switching angle of only one converter (bridge-1) is controlled. Bridge-2 is kept off and it is bypassed by the freewheeling diode (D_{F2}). Thus, $\alpha_2 = 180°$ and i_2 remains zero. There is no contribution of i_2 to the primary current i. Here, α_1 is controlled from 180° to 0°. The average value of the output dc voltage is given by

$$V_o = V_{o1} = \frac{V_{m1}}{\pi}(1 + \cos\alpha), \qquad \text{for } 0 \le V_o \le \frac{1}{2} V_{o(max)} \quad \text{and} \quad \alpha_2 = 180° \tag{6.68}$$

For the dc output voltage, from a half to the maximum output voltage, $V_{o(max)}$, bridge-2 is used as uncontrolled converter ($\alpha_2 = 0$), and α_1 is controlled from 180° to 0° (wave forms are shown in Fig. 6.28). The average value of the output dc voltage is given by

$$V_o = V_{o1} + V_{o2} = \frac{V_{m1}}{\pi}(1 + \cos\alpha_1) + \frac{V_{m2}}{\pi}(1 + \cos\alpha_2) = \frac{V_{m1}}{\pi}(1 + \cos\alpha_1) + \frac{V_{m1}}{\pi}(2)$$

$$= \frac{V_{m1}}{\pi}(3 + \cos\alpha_1), \quad \text{for } \frac{1}{2} V_{o(max)} \le V_o \le V_{o(max)} \quad \text{and} \quad \alpha_2 = 0° \tag{6.69}$$

The maximum average value of the output voltage is given by

$$V_{o(max)} = \frac{4V_{m1}}{\pi}, \qquad \text{for } \alpha_1 = \alpha_2 = 0° \tag{6.70}$$

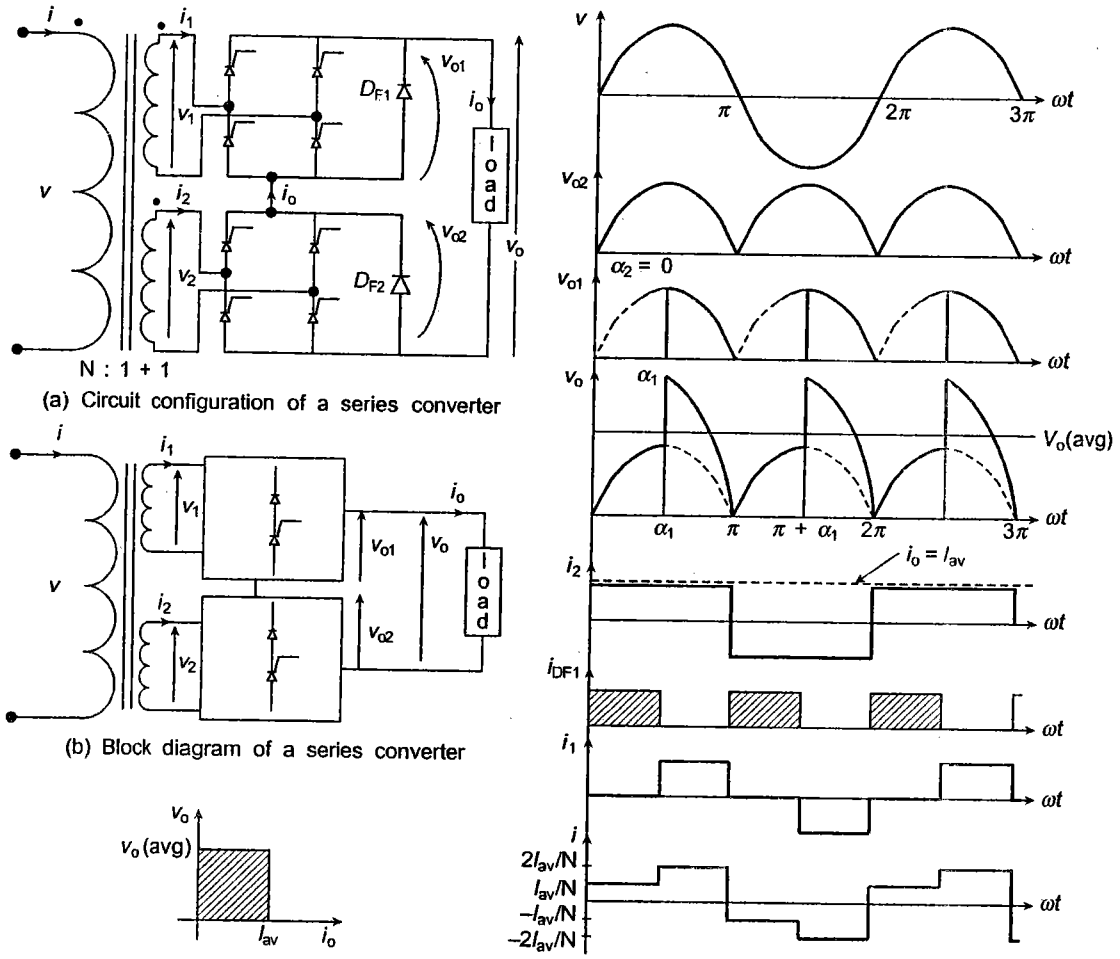


Figure 6.28 A two-stage series converter using semiconverters.

The normalized average output voltage is

$$V_{on} = \frac{V_o}{V_{o(max)}} = \frac{1}{4}(3 + \cos\alpha_1) \tag{6.71}$$

Figure 6.29 shows another series converter with full-converters. Here due to the absence of the free wheeling diodes, any converter (thyristor bridge) cannot be bypassed. Both converters are capable to operate in rectifier and inversion modes. However, the load current should be continuous or, in other words, the load should be highly inductive for successful operation in the IVth quadrant. In both the cases, switching angle of only one converter (say α_1) is controlled. In rectifier mode, one converter bridge is used as uncontrolled rectifier ($\alpha_2 = 0$) and the switching angle of other converter bridge (α_1) is controlled from 180° to 0° (Fig. 6.19). Similarly, in the inversion mode, the second converter bridge is used as an inverter. Here α_2 is kept close to 180° and α_1 is controlled from 0 to 180°. Here the line or input current is modulated single pulse. Therefore, THD reduces and PF improves.

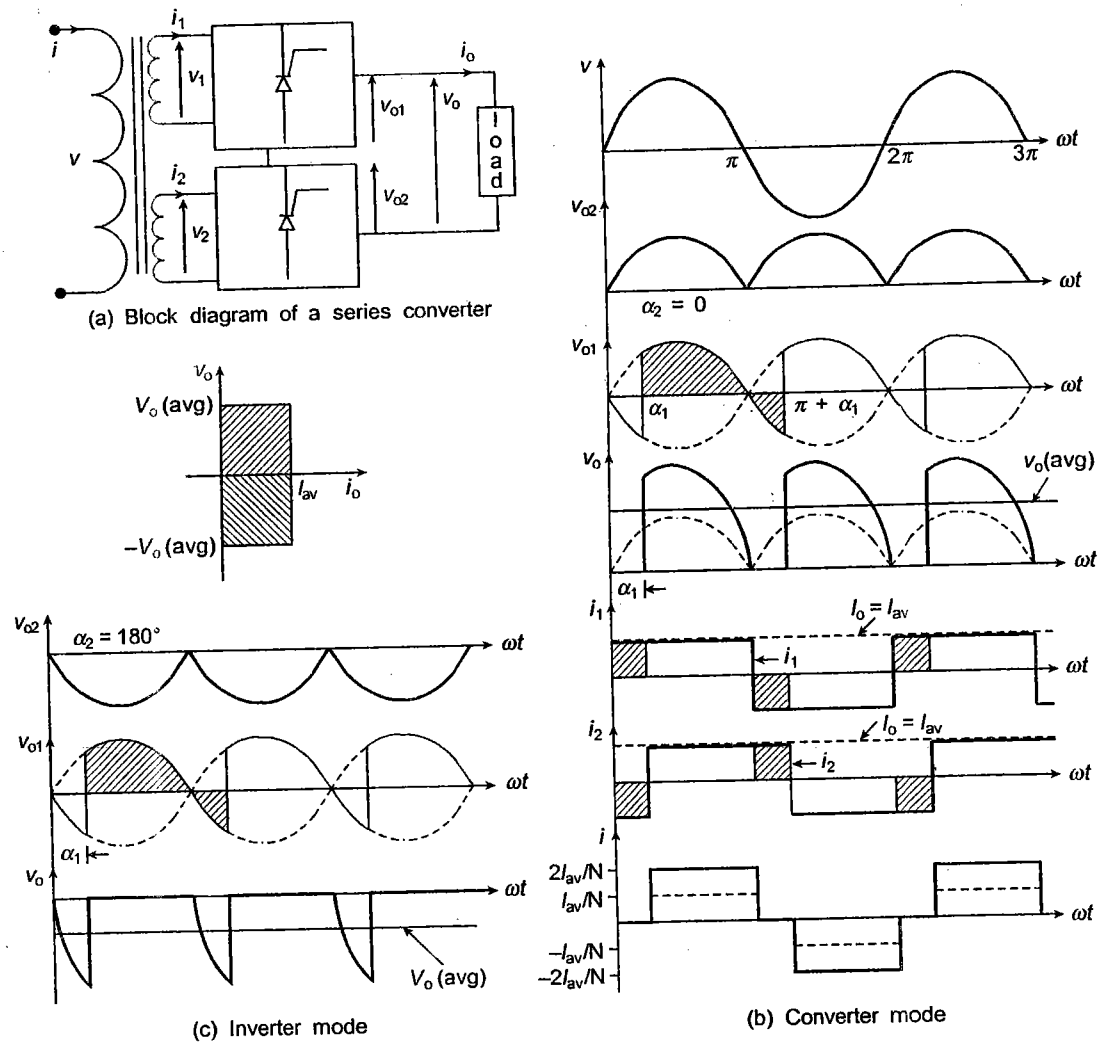


Figure 6.29 A two-stage series converter using full-converters.

6.8.4 Three-phase Converters

The control strategy of a three-phase series or sequence converters are same as its counter part single-phase system. Here, two or more converters are connected in series. They may be a three-phase full- or semi-converter.

6.9

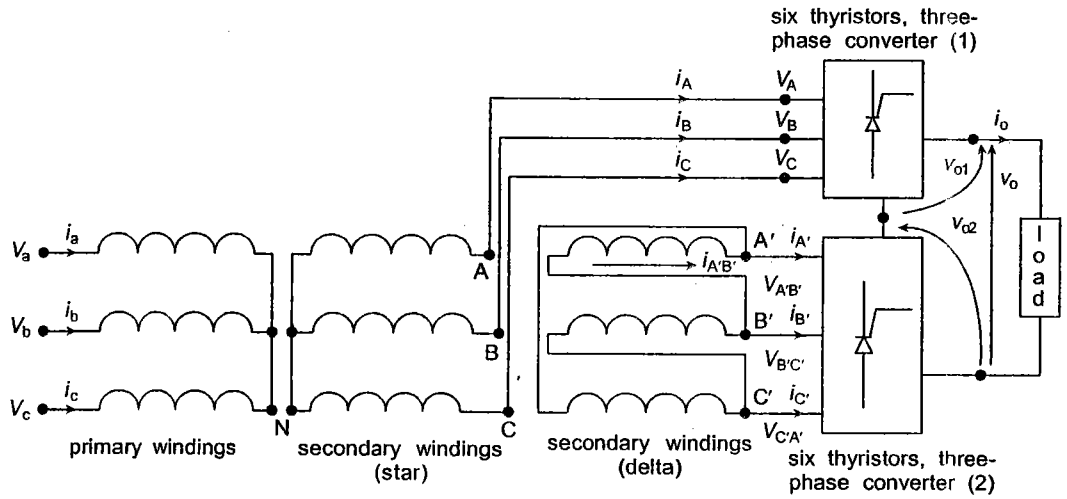
TWELVE-PULSE CONVERTERS

In case of a six-pulse converter, the output voltage and current ripple reduce drastically (in comparison to two-pulse, single-phase converters). Therefore, the requirement of the filter inductor

reduces as the effective inductive reactance increases by three times. Further reduction in ripples is achieved with a twelve-pulse converter. It is realized by connecting two six-pulse converters in series or in parallel. However, the circuit configuration depends upon the connection of secondary windings of transformer connected to each converter. In HVdc transmission, often several such bridges are connected in series to achieve higher operating direct voltage and to reduce the voltage and current ripples. Either two separate three-phase transformers or two set of secondary windings are used as an input supply to each converter. These secondary windings are star and delta connected such that their line voltages are equal and displaced by 30°. The magnitude of load current (thyristor current) of both converters is same due to equal input line voltage.

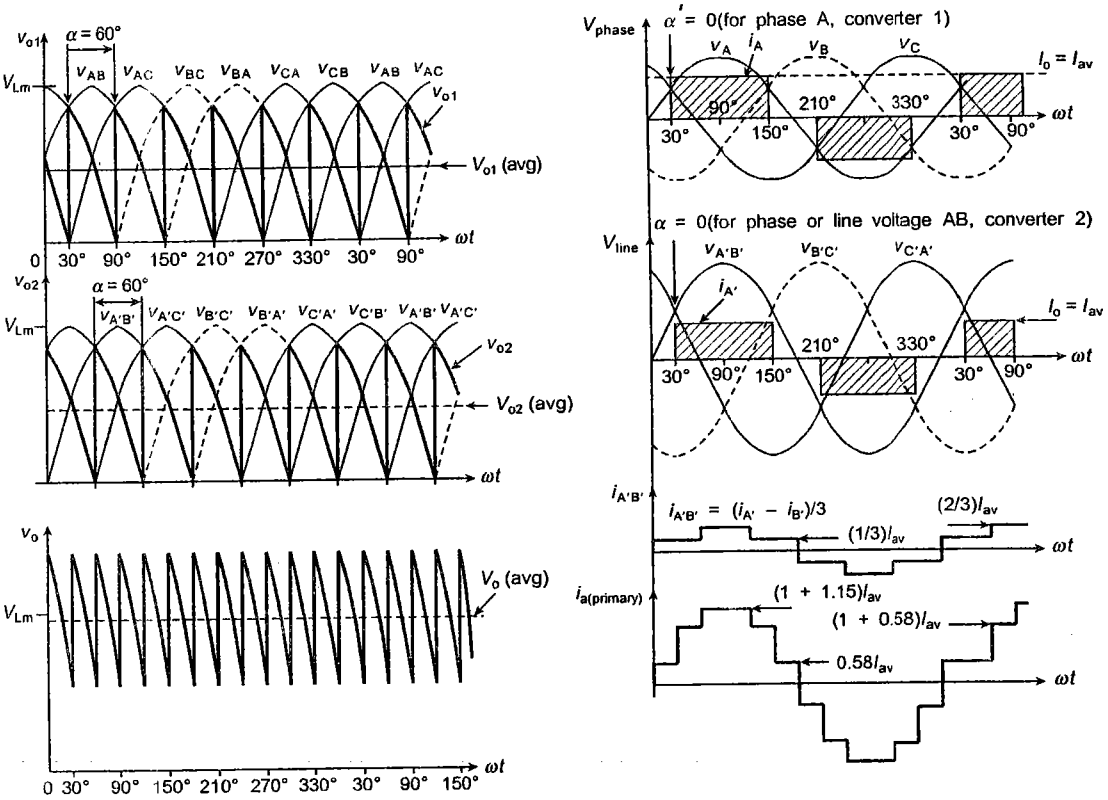
6.9.1 Twelve-pulse Series Converters

Figure 6.30a shows circuit configuration, where converters 1 and 2 are connected with star- and delta-connected secondary windings, respectively. The conduction period of the line current for each converter is 120° and the magnitude of the current is constant (ripple free, i.e. $i_o = I_{av}$). The line current of the star-connected windings (input to converter-1) is same as the phase current. Therefore, the reflected current waveform in the primary winding is also same. For the sake of simplicity, if turns ratio is 1:1, then the magnitude of the primary current is also equal. The number of turns in each phase winding of Δ-connection is $\sqrt{3}$ times of Y-connection. Therefore, the reflected current in the primary winding due to Δ connected winding is $\sqrt{3}\, i_o$. The resultant current in the primary winding is sum of i_o (due to converter-1) and $\sqrt{3}\, i_o$ (due to converter-2). However, the phase current in the delta windings is either $\frac{1}{3} I_{av}$ or $\frac{2}{3} I_{av}$. Therefore, the reflected current in the primary side is stepped (Fig. 6.30b), and the waveform of the total primary current improves drastically. The waveform of the current remains unchanged for different values of α (except its phasor position), which shifts with respect to the input voltage.



(a) Circuit of a twelve-pulse series converter.

Figure 6.30 (*Cont.*)



(b) Waveforms of a twelve-pulse series converter.

Figure 6.30 A three-phase, twelve-pulse, two-stage series converter.

6.9.2 Twelve-pulse Parallel Converters

In this case, two converters are connected in parallel. These converters are energized by two separate Y and Δ-connected windings of a single or two separate three-phase transformers. The converter input ac voltages (line) are displaced by 30° due to Y and Δ-connected secondary windings (Fig. 6.31). The converter operates in the circulating current mode only. The total line

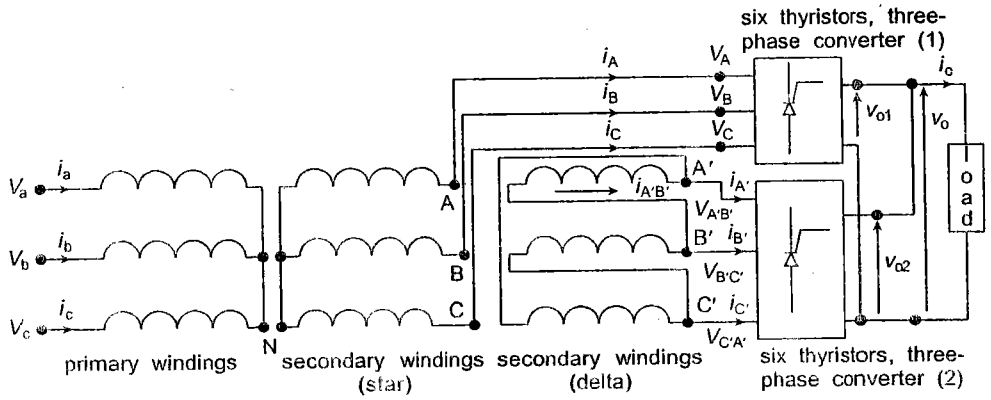


Figure 6.31 A three-phase, twelve-pulse, two-stage parallel converter.

current becomes stepped due to phase shift in the input currents (primary windings of both transformers), as discussed in twelve-pulse series converters. Therefore, THD and requirement of filter circuit parameters reduces. The output voltage for a resistive load is given by

$$V_o = \frac{24\sqrt{3}V}{\pi}\sin\alpha, \qquad 0 < \alpha < \frac{\pi}{12}$$

$$= \frac{12\sqrt{3}V}{\pi}\left[\left(1 - \frac{\sqrt{3}}{2}\right)\sin\alpha + \frac{1}{2}\cos\alpha\right], \qquad \frac{\pi}{12} < \alpha < \frac{\pi}{2}$$

$$= \frac{12\sqrt{3}V}{\pi}\left[1 + \cos\left(\alpha + \frac{\pi}{3}\right)\right], \qquad \frac{\pi}{2} < \alpha < \frac{2\pi}{3} \tag{6.72}$$

For a six-pulse converter at $\alpha = \pi/3$, the output dc voltage is just continuous. Therefore, there is no effect of β and V_o is same for a given value of α ($\alpha \leq 60°$), and for any R or RL load.

6.10 REACTIVE POWER OF CONVERTERS

In case of an ac to dc converter, the reactive power is drawn from the supply even though the load is purely resistive. This happens due to the line or input current, which lags the input sinusoidal voltage because of the delay or switching angle (α). Thus the reactive power required by a converter depends upon α. This is also called *controlled reactive power*. In general, it is lagging for R and RL loads. However it could be leading if capacitors are connected at the ac side of the converter.

The mean (or active) power for a sinusoidal voltage (V) and a non-sinusoidal current (I) is given by

$$P = VI_1 \cos\phi_1 = VI_P \tag{6.73}$$

where I_1 is the fundamental component of I, $\cos\phi_1$ is the displacement factor and I_p is the in-phase component of current I_1.

For reactive power,

$$Q = VI_1 \sin\phi_1 = VI_Q \tag{6.74}$$

where I_Q is quadrature component of current I_1.

The normalized active power for full-wave, full converters is given by

$$P_n = \frac{VI_P}{VI_1} = \frac{V_o I_o}{V_{o(max)} I_o} = V_{on} = \cos\alpha \tag{6.75}$$

or

$$I_P = I_1 \cos\alpha \quad \text{and} \quad \alpha = \phi_1$$

Then

$$I_Q = I_1 \sin\phi_1 = I_1\sqrt{1 - \cos^2\phi_1} = I_1\sqrt{1 - \cos^2\alpha} \tag{6.76}$$

Therefore, the normalized reactive power is given by

$$Q_n = \frac{VI_Q}{VI_1} = \sqrt{1 - \cos^2\alpha} = \sin\alpha \tag{6.77}$$

Similarly, for full-wave, half-converters, the normalized active power is given by

$$P_n = \frac{VI_P}{VI_1} = \frac{V_o I_o}{V_{o(max)} I_o} = V_{on} = \frac{1}{2}(1 + \cos\alpha) \tag{6.78}$$

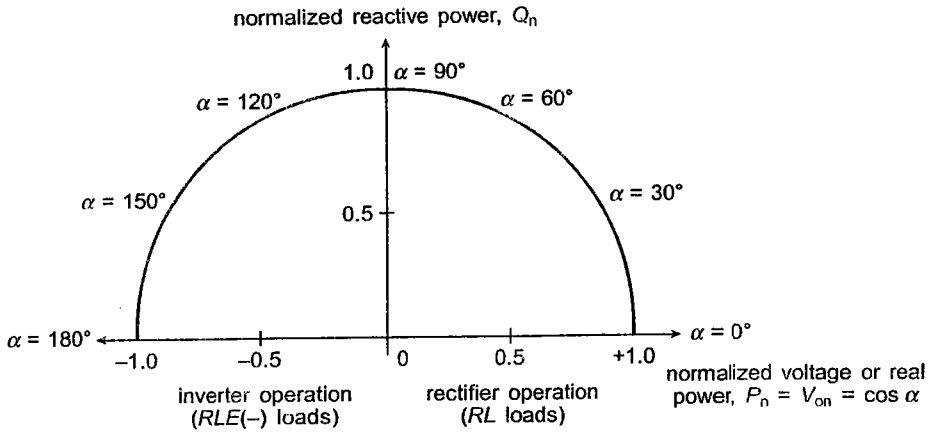
Also

$$I_P = \frac{I_1}{2}(1 + \cos\alpha) \quad \text{and} \quad I_Q = \frac{I_1}{2}\sin\alpha \tag{6.79}$$

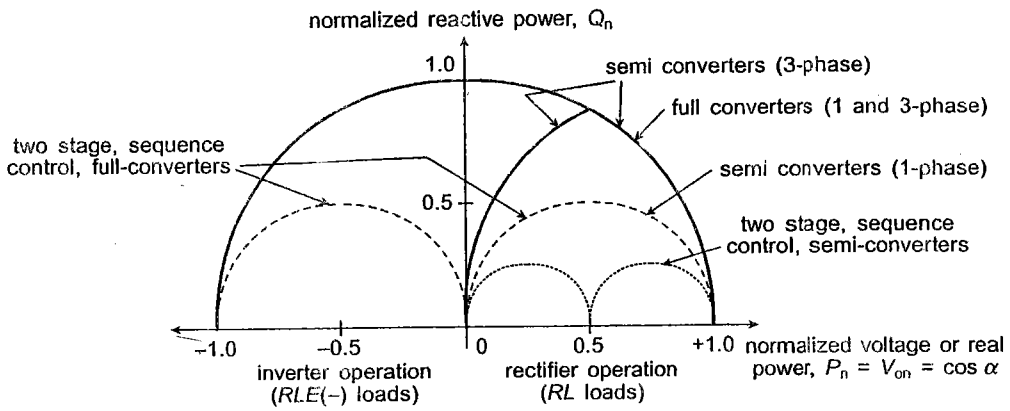
The normalized reactive power is given by

$$Q_n = \frac{VI_Q}{VI_1} = \frac{1}{2}\sin\alpha \tag{6.80}$$

Figure 6.32 shows the variation and the requirements of reactive powers of different types of converters. It is evident that the requirement or introduction of reactive power in the line reduces and input PF improves in case of series converters.



(a) Single and three-phase full-converters



(b) Reactive power requirements of Different converters

Figure 6.32 Variations and requirements of reactive power of different types of converters with a constant load current.

SUMMARY

Phase-controlled converters are used to obtain a fixed or an adjustable dc output voltage from a fixed or an unregulated ac input voltage. In general, thyristors (SCR) and diodes are used in different types of bridge circuits. Both single-phase and three-phase ac inputs are used for this purpose. The control is applied either in half-cycle or in both half-cycles. Accordingly, it is called half-wave or full-wave converters, respectively. Similarly, semi- (half) or full-converters refer to the controllability in the first quadrant or both first and fourth quadrant of the output v_o-i_o plane, respectively. For a semi-converter the average output voltage is always positive. For a full-converter, the output voltage may be negative as well, when an active voltage source is connected at the output. Multiple converters are used for the same purpose. Parallel type dual converters are used for reversing the direction of current and therefore the controllability is achieved in all the four quadrants. Similarly, a series converter improves PF and THD. Thyristor-based converters are able to handle power from a few watts to several hundred MW (e.g. in case of HVdc systems).

REVIEW QUESTIONS AND PROBLEMS

1. Why the performance of a thyristor based ac-to-dc converter rectifier is better than a tap-changing transformer with diode configuration?
2. What is the principal of phase-controlled converters?
3. Why the instantaneous output voltage becomes negative, in case of an *RL* load?
4. Explain free-wheeling action of a diode.
5. Why PF is better in case of a semi-converter than a full-converter?
6. Why, in general, half-wave converter circuits are not used?
7. Find THD and PF of a single-phase, full-converter with a highly-inductive *RL* load for $\alpha = 0$, 22.5°, 45°, 67.5°, 90°, 122.5° and 135°.
8. Why an *RLE* (–) load is necessary for inversion operation?
9. Explain the performance of the converters shown in Fig. 6.33.
10. (a) What happens if the diode in Fig. 6.33d is reversed?

    (b) What happens if T_2 of Fig. 6.33e, is shorted due to fault in the positive half-cycle?
11. For higher power applications, why a three-phase system is preferred over a single-phase ac-to-dc converter rectifier?
12. What is the effect of three-phase system on harmonics? How the performance can be further improved?
13. What are demerits of a three-phase, zig-zag winding transformer based three-phase converter?

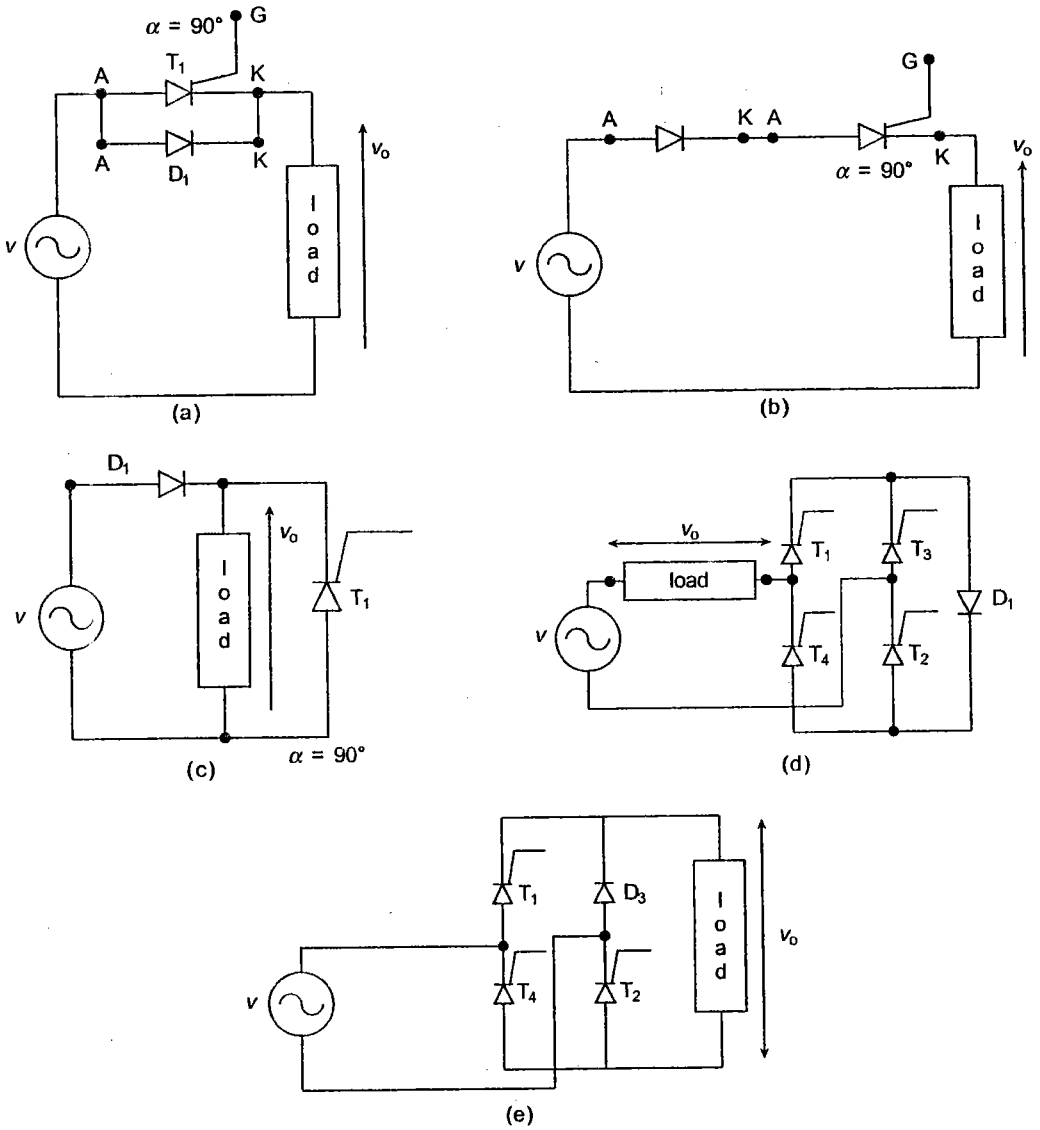


Figure 6.33 For question 9 and 10.

14. Why, for $\alpha \leq \pi/6$, the average output voltage (V_o) for a given α is same for three-phase semi- and full-converters as well as for any R or RL load?

15. An armature circuit (RLE load) of a separately-excited dc motor is fed from a three-phase, six-pulse, fully-controlled converter. The supply ac voltage (line) = 163 V, R_a = 1.0, I (rated) = 25 A, V_a (rated) = 220 V.
For the rated load current, find the output voltage and the switching angle at (i) E = 156 V and (ii) E = −104 V.

16. If the same control is to be achieved by dual (parallel type) converters using the same three-phase, full-converters as mentioned in Question 15. Find α for both non-circulating and circulating current type dual converters.

17. A three-phase, full converter is connected with a 400 V input voltage supply. A highly-inductive *RL* load (20 Ω) is connected at the output. Find PF and THD of the converter for $\alpha = 60°$.

18. Why a circulating-current type dual converter is faster than its counterpart?

19. Why three-phase, twelve-pulse converters are preferred over six-pulse converters?

20. What do you mean by the requirement of reactive power for a converter? Why at all, it is required, even for a purely resistive load?

7

DC-to-DC Converters*

7.1 INTRODUCTION

Different types of dc-to-dc converters are widely used for dc drives in traction (electric trains), electric vehicles (EV), electric cars, trolley cars, golf carts, forklift trucks and switched-mode power supplies (SMPS). Moreover, there are numerous applications in solar photo-voltaic (PV) cell based power generation systems. At present, PV based dc-to-dc converters are extensively used in space applications, lighting applications in remote areas and PV based water pumping systems. In such converters, an adjustable dc voltage is obtained from a fixed voltage dc source. A dc-to-dc converter is also called a *dc-chopper*. The function of a deconverter or dc chopper is similar to the function of an autotransformer in an ac circuit, where an adjustable (variable) output voltage is obtained from a fixed ac voltage. The basic principle of a dc voltage control can be understood with the help of Fig. 7.1. By closing and opening of the switch (i.e. chopping or disconnecting

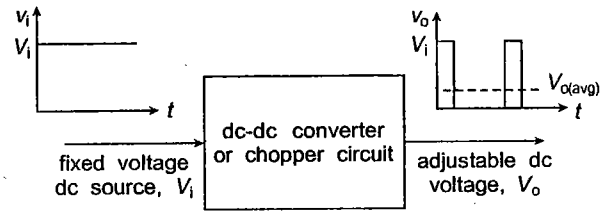


Figure 7.1 Block diagram of a dc-to-dc converter or chopper.

the supply voltage), the dc voltage supply reaches the load in pulse form hence the output dc voltage (average value) is controlled. In comparison to the input dc voltage level, the output dc voltage can be controlled to a lower-voltage level (using a step-down chopper) or to a higher-voltage level (using a step-up chopper). The circuit configurations of these choppers are

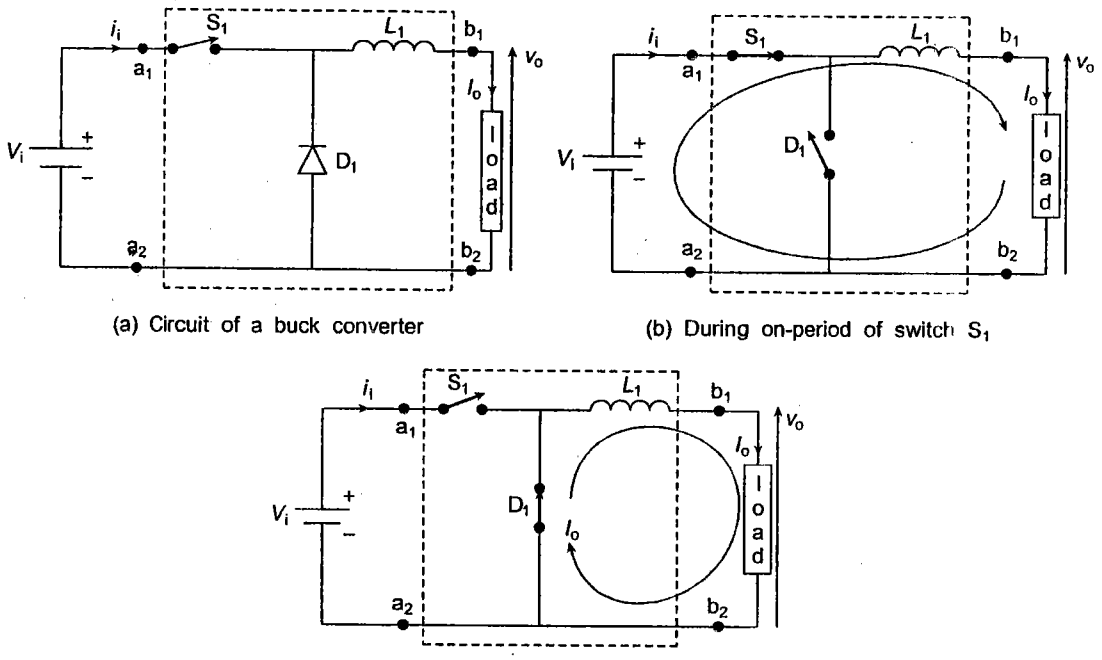
*Contributors: Atif Iqbal and M. Syed Jamil Asghar, Department of Electrical Engineering, Aligarh Muslim University, Aligarh.

different. When a chopper circuit is capable to operate in both step-down and step-up modes, or direction of voltage or current can be reversed, it is called *two-quadrant* chopper. In a two-quadrant chopper, power flows in both the directions, and the transition between the two modes is smooth. This type of chopper finds its application in dc motor speed control with the facility of regenerative braking. Similarly, with the help of four-quadrant choppers, both voltage and current, hence both speed and torque, are reversible.

This chapter is devoted to the basic concepts circuit topology, operation and control of dc-to-dc converters. Thyristor based dc-to-dc converters are used for high power applications. It has limited circuit topologies and it is being discussed here under the head of dc choppers. Linear dc-to-dc converters are used for low power applications only. However, gate-commutation based switch-mode (PWM) dc-to-dc converters are used for low to medium level power applications. There are several thousand circuit topologies of switch mode dc converters.

7.2 PRINCIPLE OF DC CHOPPERS

In general dc choppers consists of power semiconductor devices (thyristor, power BJT, power MOSFET, IGBT, etc., which work as a switch), input dc power supply, circuit elements (R, L, C etc.) and output load (Fig. 7.2). The average output voltage across the load is controlled by varying on period and off period (or duty cycle) of the switch (S). The input voltage (V_i) is a constant dc voltage



(a) Circuit of a buck converter

(b) During on-period of switch S_1

(c) During off-period of S_1

Figure 7.2 A buck dc-to-dc converter or step down chopper.

source connected to the terminals a_1-a_2. The chopper consists of a switch (S_1), a diode (D_1) and an inductor (L_1). The load is connected to the terminals b_1-b_2. A thyristor based chopper lacks the advantage of natural commutation because of a dc input. A commutation circuit is necessary for a thyristor. Therefore, in general, gate-commutation devices based dc-to-dc converters have replaced the thyristor-based choppers. However, for high voltage and high-current applications, thyristor based choppers are still in use. The variation in on and off periods provides an output voltage with an adjustable average value. The power diode (D_1) operates in freewheeling mode to provide a path to load current when S_1 is off. The inductor (L_1) filters out the ripples in load current. It is called the *smoothing inductor*. The operation of this chopper circuit can be divided into two distinct modes:

Mode I (switch S_1 closed) The switching diagram for this mode is shown in Fig. 7.2(b). When S_1 is turned-on by applying a gate signal, the input current (i_i) and the output or load current (i_o) start building up exponentially due to the presence of the inductor (L_1).

Mode II (switch S_1 open) The switching diagram for this mode is shown in Fig. 7.2(c). When the switch S_1 is turned off, the decaying i_o results in a negative or reverse voltage [$L_1(di_o/dt)$] to appear across the inductor. The cathode of D_1 becomes negative and D_1 turns on. It provides a free-wheeling path to i_o. The waveforms of the output voltage and current are shown in Fig. 7.3. The average output voltage is given by

$$V_o = \frac{T_{on}}{T_{on} + T_{off}} V_i = \frac{T_{on}}{T} V_i = DV_i \tag{7.1}$$

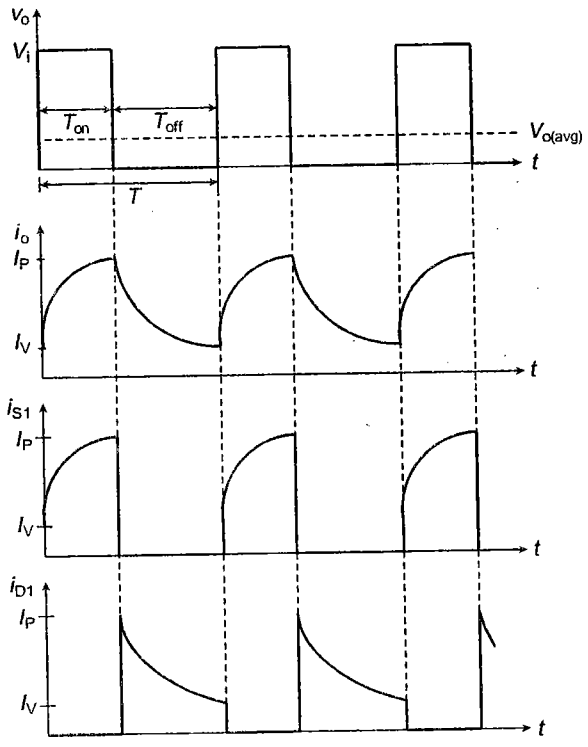


Figure 7.3 Waveforms of a buck converter.

Also,

$$V_o = \frac{T_{on}}{T} V_i = T_{on} f V_i \tag{7.2}$$

where,

T_{on} = On period of the switch (S_1)

T_{off} = Off period of the switch

T = Time period of control

f = $1/T$ = Chopping frequency

D = T_{on}/T, is called duty-cycle or duty-ratio.

Ideally, D can acquire any value between 0 and 1. However, the time delay in turning-on and turning-off operations of the switch imposes a restriction on the variation of the duty-cycle range. It is evident from (7.1), the output voltage (V_o) is directly proportional to the duty-cycle. The output voltage can be controlled by the time-ratio control and current-limit control methods.

Time-ratio control (TRC) In this method, the on period of the switch (T_{on}) is varied keeping the time period (T) fixed. Alternatively, either T_{on} or T_{off} period is kept constant and T (the chopping frequency, f) is controlled. The former technique is called *pulse-width modulation* (PWM) while the later is called *frequency modulation*. Figure 7.4 shows the output voltage waveforms with PWM and frequency modulation techniques.

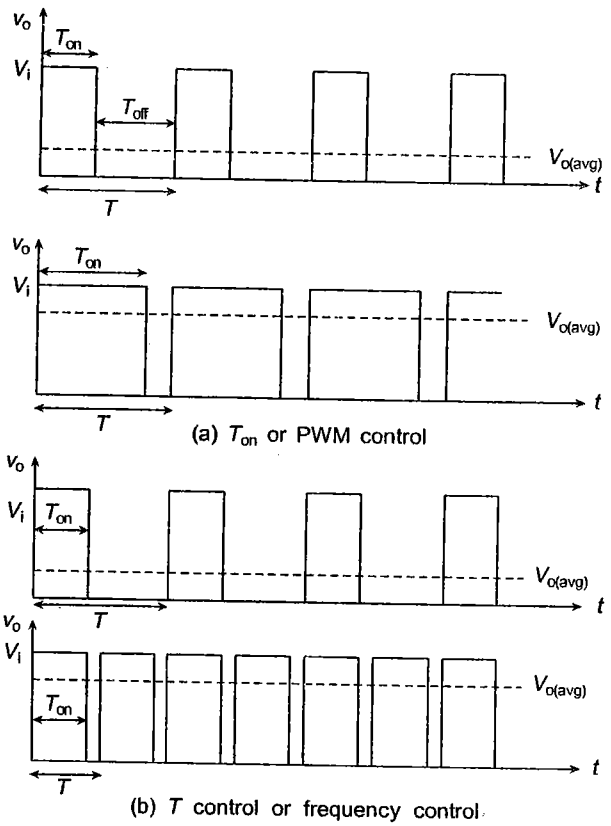


Figure 7.4 Voltage control of a chopper by TRC or PWM.

Current-limit control (CLC) Sometimes it is required to keep the output current constant (e.g. to keep the load current or the output torque constant in a dc motor). In such cases, the switch of the chopper is controlled in such a way that it operates (open and closes) at certain threshold values of the current, as shown in Fig. 7.5. The on-period of the switch and the output voltage (V_o) are self adjusting. These depend upon the load current.

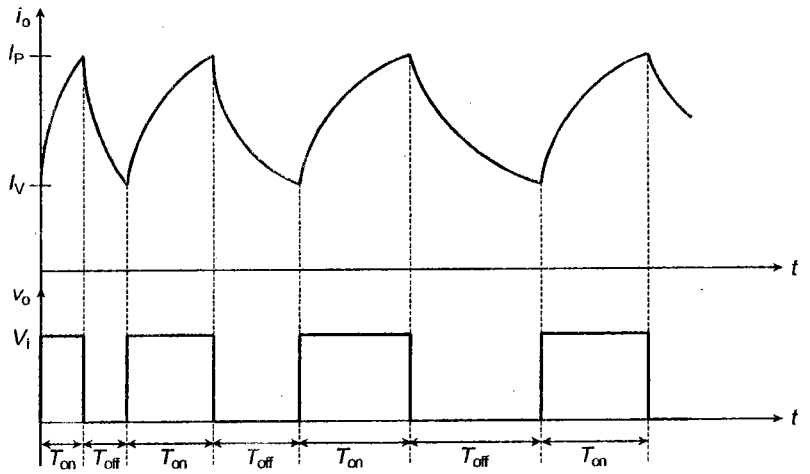


Figure 7.5 Output voltage and current waveforms with CLC.

Example 7.1 A battery powered electric vehicle uses a dc motor drive, controlled by a dc chopper working at 10 kHz. The battery voltage is 220 V. The minimum turn-on and off-time of the chopper switch (an inverter grade SCR) are 2 μsec and 25 μsec, respectively. Determine the minimum and the maximum dc voltage that the chopper can deliver to the motor.

Solution We have

Total time period of chopper, $T = \dfrac{1}{10 \times 10^3} = 100\ \mu s$

Minimum possible on-time = 2 μs

Minimum possible duty-cycle, $D_{min} = \dfrac{T_{on}}{T} = \dfrac{2}{100} = 0.02$

Output voltage, $V_o = DV_i$

Minimum possible output voltage, $V_{o(min)} = D_{min}V_i = 0.02 \times 220 = 4.4$ V

Maximum possible on-time, $T_{on} = T - T_{off} = 100 - 25 = 75$ μsec

Maximum possible duty-cycle, $D_{max} = \dfrac{T_{on}}{T} = \dfrac{75}{100} = 0.75$

Maximum possible output voltage, $V_{o(max)} = D_{max}V_i = 0.75 \times 220 = 165$ V

Output voltage controllability of the chopper circuit is from 4.4 V to 165 V only.

Example 7.2 In a 100-V dc chopper drive using the CLC scheme, the maximum possible value of the accelerating current is 425 A, the lower limit of the current pulsation is 180 A. The length of on and off period is 14 ms and 11 ms, respectively. Determine the limit of current pulsation, the chopping frequency, the duty cycle ratio and the output voltage.

Solution We have I_{max} = 425 A, T_{on} = 14 ms, T_{off} = 11 ms and I_{min} = 180 A. Therefore,

Maximum limit of the current pulsation = 425 − 180 = 245 A

$$\text{Chopping frequency} = \frac{1}{T} = \frac{1}{14\,\text{ms} + 11\,\text{ms}} = 40\ \text{Hz}$$

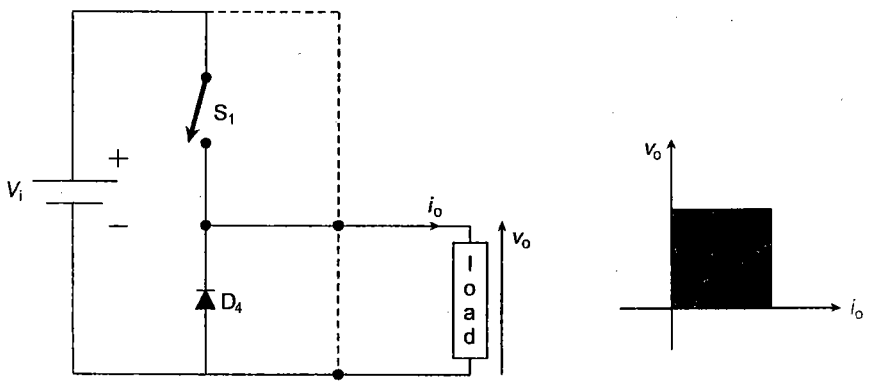
$$\text{Duty ratio, } D = \frac{T_{on}}{T} = \frac{14}{25} = 0.56$$

Output voltage, $V_o = DV_i = 0.56 \times 100 = 56$ V

7.3 CLASSIFICATIONS OF DC CHOPPERS

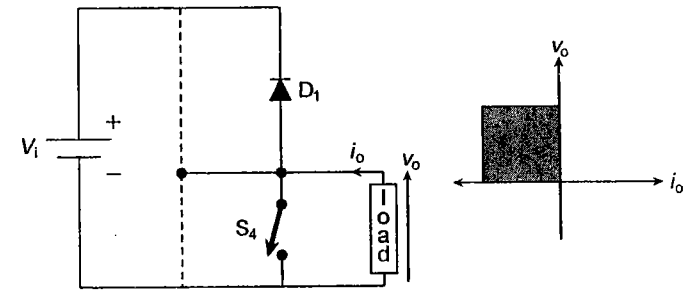
Classification of dc choppers depends upon the direction of the load current and voltage, i.e. whether the current is flowing from the source to the load or vice versa, and whether the output power or the load voltage is positive or negative.

Class A The load current flows from the dc source to the load. Therefore, both load voltage (v_o) and load current (i_o) are positive. The chopper operates in the first quadrant of v_o-i_o plane (Fig. 7.6a). The diode D_4 prevents the output voltage to become negative. Normally, a step-down chopper comes under this category, where the output voltage is less than or equal to the input voltage ($D \leq 1.0$).

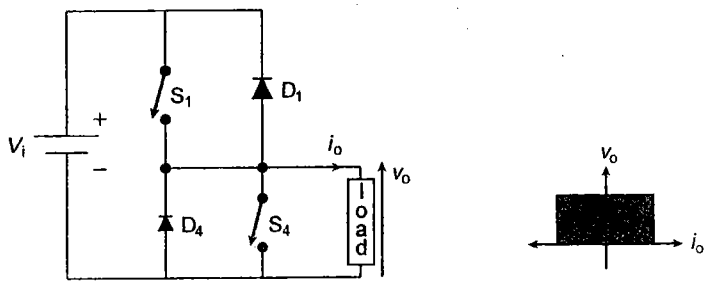


(a) Class-A chopper

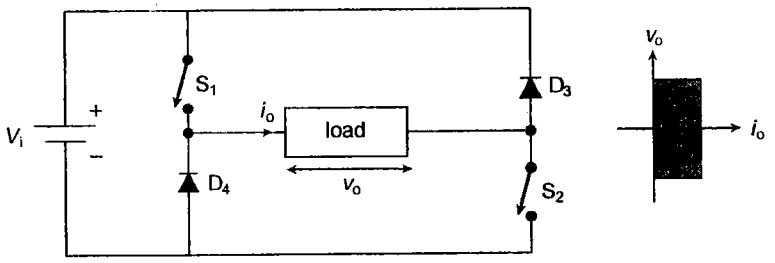
Figure 7.6 (*Cont.*)



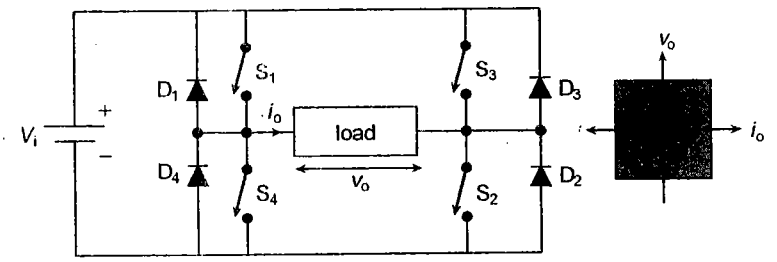
(b) Class-B chopper



(c) Class-C chopper



(d) Class-D chopper



(e) Class-E chopper

Figure 7.6 Classification of choppers.

Class B In this case, the load current is negative and the load voltage is positive (Fig. 7.6b). The load supplies power to the dc source and the chopper operates in regenerative mode and in the second quadrant of v_o-i_o plane. Here either the diode D_1 or the switch S_4 conducts. Normally load circuit contains a charged capacitor, active load or a dc source (e.g. the armature *RLE* circuit of a dc motor).

Class C It is a combination of both class-A and class-B choppers. The load current may be positive or negative but the load voltage is always positive. It is basically a dual chopper and operates in both the first and second quadrants (Fig. 7.6c).

Class D In this case, the load voltage may be positive or negative but the load current is always positive. This is also a dual chopper and operates in both the first and fourth quadrants (Fig. 7.6d). Either S_1 and S_2 or D_3 and D_4 conduct simultaneously.

Class E It is a four-quadrant chopper. The polarity of both the load current and the load voltage are independently reversible. The load is connected in between two back-to-back connected class-C or class-D choppers so that the directions of both current and voltage can be reversed (Fig. 7.6e).

7.4 FORCED-COMMUTATED THYRISTOR-BASED CHOPPERS

When switches are thyristors, they carry up to the full-load current. A chopper using thyristors cannot be line-commutated because of the dc input supply (the supply voltage, hence the load current, does not reduce to the holding current level). Thus, the forced-commutation is mandatory. There are several type of commutation circuits used for dc choppers. However, if the load is an *RC* or *RLC* (underdamped) circuit then the load current reduces to zero and the commutation takes place. It is called *load-commutation* and the performance of the chopper is highly load-dependent (depending upon *R*, *L* and *C* parameters i.e. $R^2 < 4L/C$). Thus, in general, a separate forced commutation circuit is used for independent commutation control of choppers. It is achieved by reducing the anode current of the thyristor below its holding current level for sufficient time. Figure 7.7 shows a circuit configuration for forced commutation of a thyristor used as a switch. There are three basic forced-commutation techniques used for dc choppers:

1. Voltage or impulse commutation
2. Current or resonant-pulse commutation, and
3. Load commutation

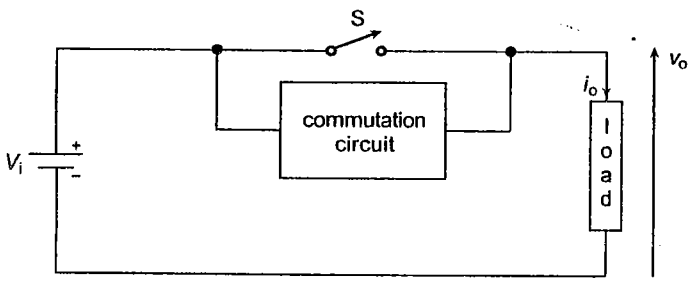


Figure 7.7 Forced-commutation scheme of thyristor based choppers.

7.4.1 Voltage or Impulse Commutation

In this case, a fully charged capacitor is switched across the main thyristor (T_m) to reverse bias it for a certain period. This duration must be more than the recovery-time (t_q) of the thyristor. The circuit topology of a voltage or impulse commutated chopper is shown in Fig. 7.8. When the anode current of the main thyristor (T_m) reduces to the holding current level (due to reverse capacitor current), commutation of the thyristor accomplishes. Here C, D, L and auxiliary thyristor, T_a constitutes the commutation circuit. R_T is the resistance used to trickle charge the capacitor (C). Following assumptions are made to explain the operation of the chopper.

- The load current remains constant during the entire commutation period (commutation period is shorter than the inductive load time constant)
- The switching devices are assumed to be ideal (no loss, no voltage drop)
- The inductor (L) is linear (no saturation takes place).

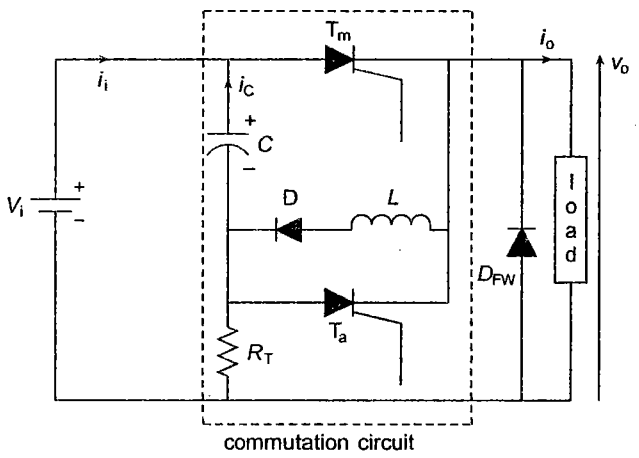
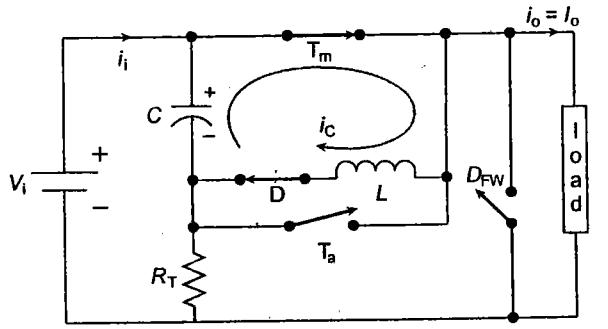


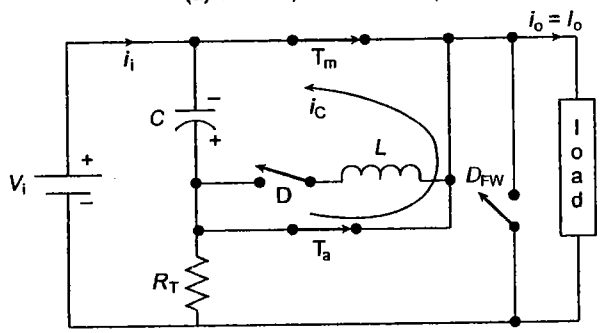
Figure 7.8 Basic circuit topology of voltage commutated chopper.

To start the operation of the chopper, the capacitor C is charged to V_i with the polarity shown in Fig. 7.9a. The sequence of operation of the chopper circuit can be explained as follows:

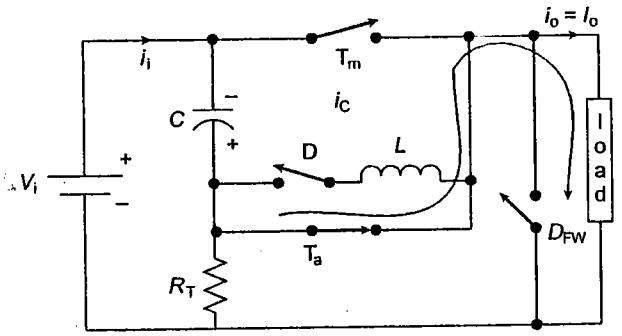
Mode I ***($0 < t < t_1$)*** This mode starts at an instant, $t = 0$, when T_m is turned on to carry the full load current, ($i_o = I_o$) as shown in Fig. 7.9a. The diode, D becomes forward biased and i_C flows. The capacitor discharges through the LC resonating circuit and recharges with the opposite polarity. Now the capacitor acquires a negative polarity of voltage, ready to commutate T_m. At this instant, i_C becomes almost zero. Thereafter, it tends to reverse the direction of flow. Therefore, commutation of diode takes (load commutation) at t_1. The conduction period of T_m continues up to t_2 and i_o remians constant ($i_o = I_o$). The circuit condition does not change between t_1 and t_2. The relevent waveforms are shown in Fig. 7.10.



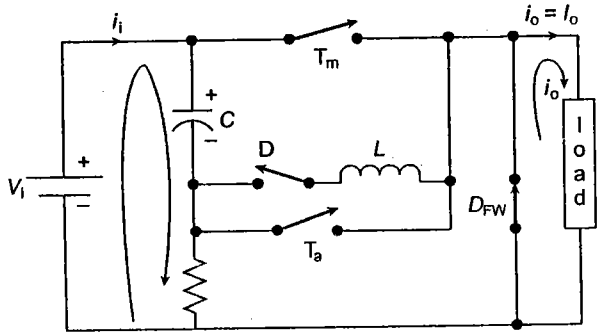
(a) Mode I, for $0 < t < t_1$



(b) Mode II, for $t_2 < t < t_3$



(c) Mode II, at $t = t_3$



(d) Mode III, for $t_3 < t < t_4$

Figure 7.9 Different modes of voltage commutation circuit.

Mode II ($t_2 < t < t_3$) To commutate T_m, T_a is triggered at $t = t_2$ (Fig. 7.9b). Thus, the capacitor voltage applies across T_m to turn it off. The load voltage suddenly takes a jump from V_i to $V_i + V_C$ or $2V_i$ (since C is in series with V_i and $V_C \cong V_i$). Then v_o decreases linearly as C discharges. It reaches zero level at $t = t_3$. The load current remains constant and flows through C and T_a. It recharges the capacitor up to $+V_i$ (with opposite polarity). The switching condition for this mode is shown in Fig. 7.9c.

Mode III ($t_3 < t < t_4$) When the capacitor gets charged to V_i (slightly higher than V_i), the current through it becomes zero. It turns off T_a at $t = t_3$ (due to load commutation). All the switches are off and the load current free-wheels through the free-wheeling diode (D_{FW}). The switching diagram is shown in Fig. 7.9(d). Then T_m is triggered and the same cycle repeats.

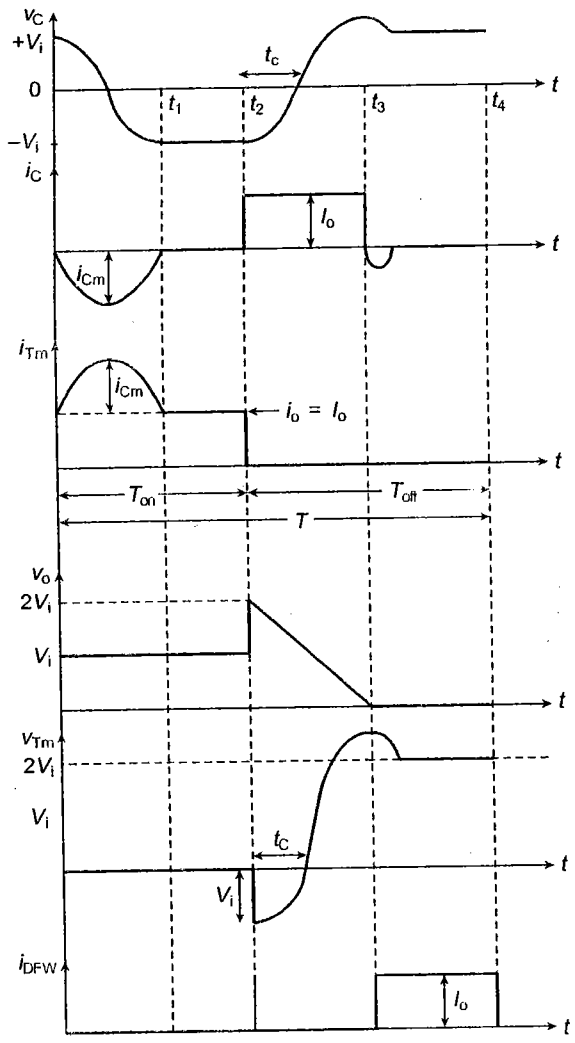


Figure 7.10 Voltage and current waveforms of voltage-impulse commutation.

MATHEMATICAL ANALYSIS

During mode I, the current i_C flows through the inductor only. The loop-voltage equation is given by

$$L\frac{di_C}{dt} + \frac{1}{C}\int i_C\,dt = 0 \tag{7.3}$$

At the initial condition, $t = 0$, $i_C = 0$, $v_C = V_i$. The solution of the voltage equation is given by

$$i_C = \frac{V_i}{\sqrt{L/C}}\sin\omega_o t \tag{7.4}$$

and

$$v_C = V_i \cos\omega_o t, \qquad \text{for } 0 \le \omega_o t \le \pi \tag{7.5}$$

where $\omega_o = 1/\sqrt{LC}$ and the maximum capacitor current, $I_{Cm} = V_i\sqrt{C/L}$. For successful commutation, this current should be greater than or equal to the load current ($I_{Cm} \le I_o$), Therefore,

$$\frac{V_i}{\sqrt{L/C}} \ge I_o$$

or

$$L \le \left(\frac{V_i}{I_o}\right)^2 C \tag{7.6}$$

For a constant-load current (between t_2 and t_3), the value of C can be chosen as,

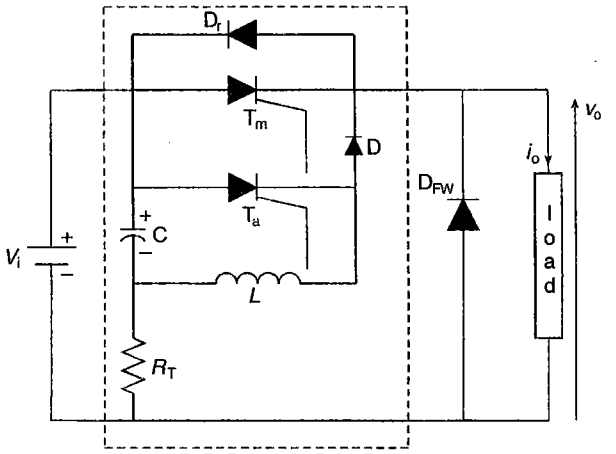
$$I_o = \frac{dQ}{dt} = C\frac{V_i}{t_C}$$

Here, t_C is the turn-off time of commutation circuit and it must be greater than t_q of the main thyristor, T_m. Therefore,

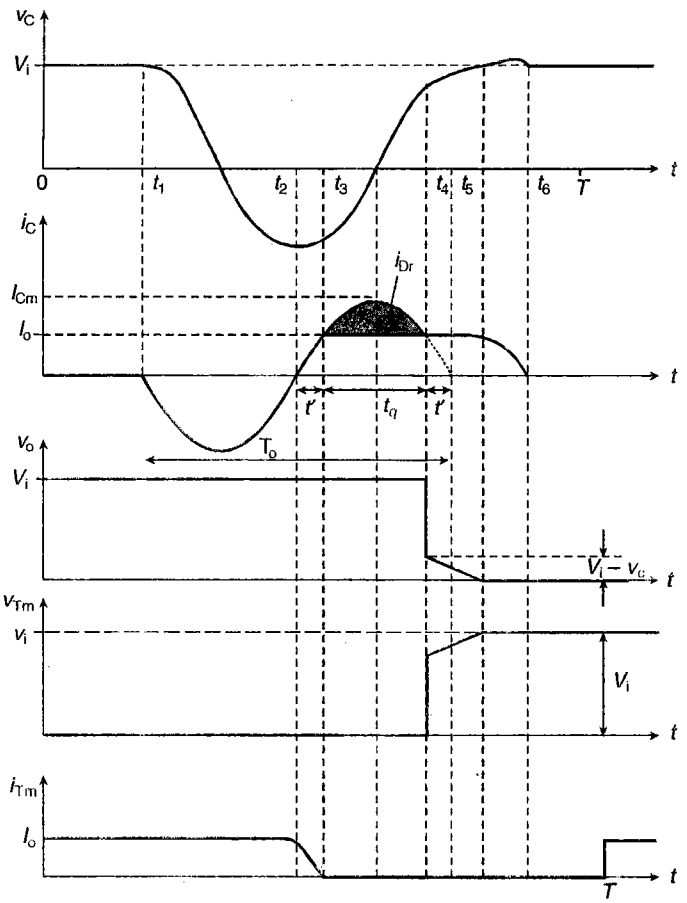
$$C > \frac{t_C I_o}{V_i} \tag{7.7}$$

7.4.2 RESONANT PULSE-COMMUTATED CHOPPER

In this case, the main thyristor (T_m) is commutated by a current-pulse which is generated by a resonating LC commutation circuit (Fig. 7.11). The reverse voltage is applied to T_m by means of a reverse diode (D_r) connected across it. Some assumptions are made such as the switches are ideal and the load current is constant during the commutation period. Initially, the capacitor is charged to $+V_i$ through R_T. The sequence of operation is explained below:



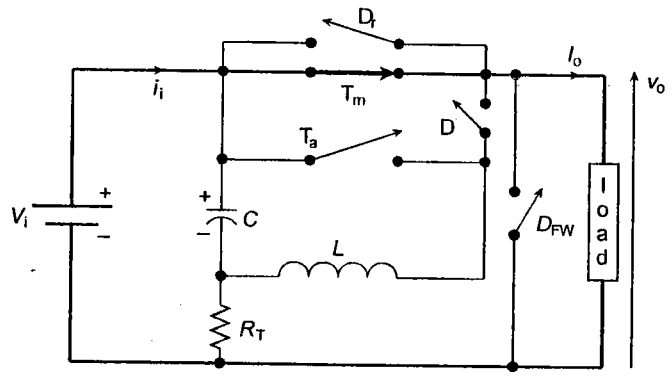
(a) Circuit topology



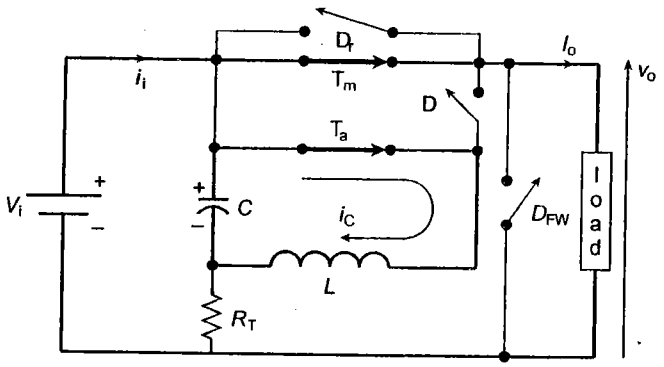
(b) Waveforms of voltage and current

Figure 7.11 A resonant pulse-commutated chopper.

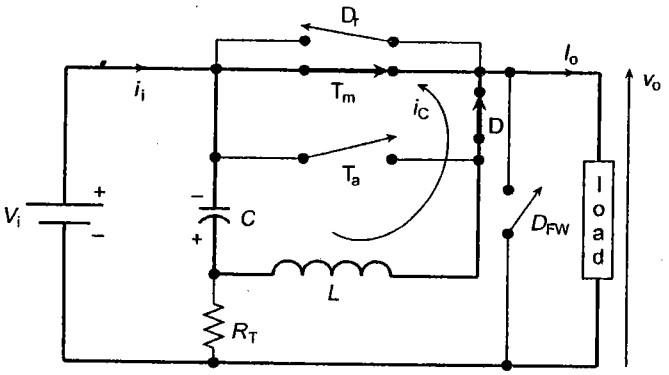
Mode I ***(0 < t < t_1)*** T_m is triggered and the dc supply is connected to the load. The capacitor is already charged through R_T and it retains a voltage, $v_C = V_i$ as shown in Fig. 7.12a.



(a) Mode I, for $0 < t < t_1$

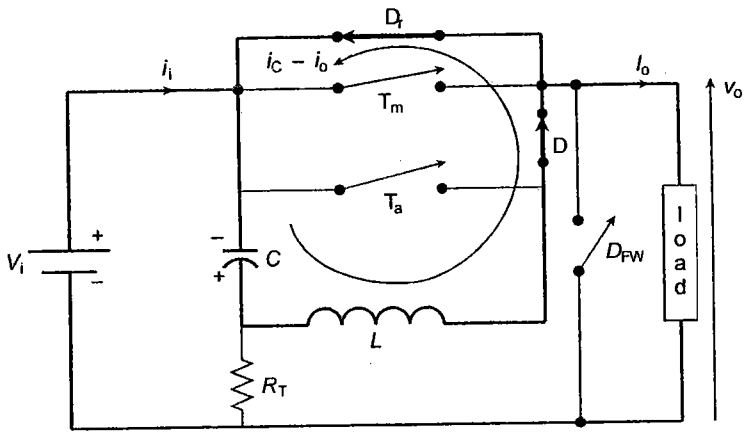


(b) Mode II, for $t_1 < t < t_2$

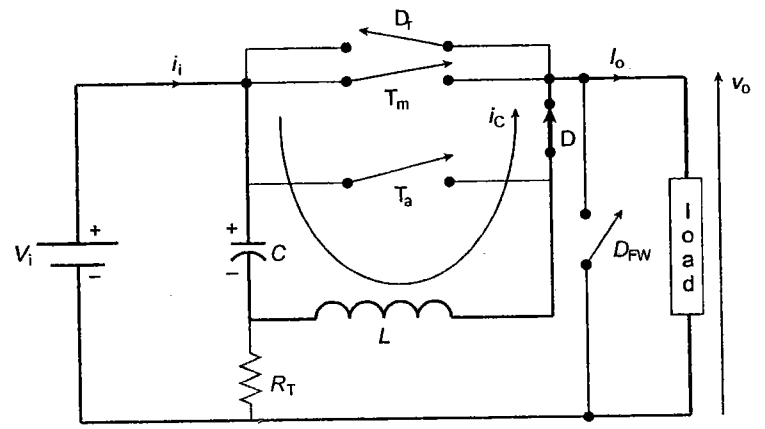


(c) Mode III, for $t_2 < t < t_3$

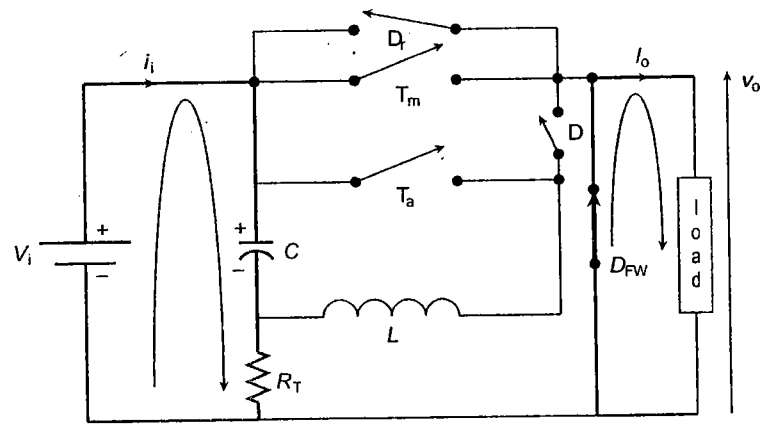
Figure 7.12 *(Cont.)*



(d) Mode IV, for $t_3 < t < t_4$



(e) Mode V, for $t_4 < t < t_5$



(f) Mode VI, for $t_5 < t < t_6$

Figure 7.12 Different modes of current commutation circuit.

Mode II ($t_1 < t < t_2$) The auxiliary thyristor (T_a) is triggered at t_1 to start the process of commutation of the main thyristor (T_m). As the capacitor is already charged, a sinusoidal resonating current (i_C) starts flowing through C, Ta and L (Fig. 7.12b). It reverses the polarity of the capacitor voltage. As soon as i_C becomes zero at t_2, T_a turns off, where the half time-period of oscillation, $t_2-t_1 = \pi\sqrt{(LC)}$.

Mode III ($t_2 < t < t_3$) The direction of the resonating current (i_C) reverses at t_2. It continues to resonate and flows through D and T_m (Fig. 7.12c). The current through T_m is the difference of the load current and i_C, i.e. $i_{Tm} = I_o - i_C$. At $t = t_3$, i_C becomes equal to I_o and commutation of T_m begins.

Mode IV ($t_3 < t < t_4$) The resonating current continues to flow up to t_4. The excess resonating current, i_C-I_o flows through reverse diode D_r (Fig. 7.12d). The maximum value of i_C (I_{Cm}) must be more than the load current for successful commutation of T_m (normally I_{Cm}/I_o varies from 1.4 to 2.5). Moreover, (t_4-t_3) must be higher than the switching turn-off time, t_q of T_m. Also, the voltage drop across Tm during this period is on-state voltage-drop of D_r (about 1V). Therefore, the resonant-pulse auxiliary commutation process is slower than the voltage complementary commutation process.

Mode V ($t_4 < t < t_5$) At $t = t_4$, the current through D_r becomes zero and D_r turns off. At this condition a constant load current flows through C, L, D and load (Fig. 7.12e). During this mode, v_C increases linearly and it becomes equal to V_i at $t = t_5$.

Mode VI ($t_5 < t < t_6$) The charging continues till the capacitor is over charged due to the continuous flow of resonating current through it. This excess voltage makes the lower plate of capacitor more negative and the free-wheeling diode (D_{FW}) becomes forward biased. The current through D_{FW} increases linearly and it becomes equal to I_o at $t = t_6$. As i_C becomes zero at t_6, the diode D turns off and the commutation process completes (Fig. 7.12f). Thus (t_6-t_1) is the complete commutation period. D_{FW} conducts up to the end of the cycle (T) and again T_m is triggered for the next cycle.

Mathematical Analysis

From mode-II of the switching circuit diagram (Fig. 7.12b), the voltage equation is given by

$$\frac{1}{C}\int i_C dt + L\frac{di_C}{dt} = 0$$

Differentiating the above equation, we get

$$L\frac{d^2 i_C}{dt^2} + \frac{1}{C} i_C = 0$$

The solution of the above equation with zero initial conditions ($i_C = 0$, $v_C = 0$) is given in (7.4). The expression for the peak resonating current is given by

$$I_{Cm} = V_i\sqrt{\frac{C}{L}} \tag{7.8}$$

From the waveform of i_C, the half-period of oscillation, $(T_o/2) = t_C + 2t'$. Therefore,

$$\pi = \frac{\omega_o T_o}{2} = \omega_o(t_C + 2t') \tag{7.9}$$

Also, at $t = t'$, $I_o = I_{Cm} \sin \omega_o t'$ and therefore, $t' = (1/\omega_o) \sin^{-1} x$, where $x = I_o/I_{Cm}$. Now, from (7.9)

$$t_C = \frac{1}{\omega_o}(\pi - 2\sin^{-1}x) = \sqrt{LC}(\pi - 2\sin^{-1}x) \tag{7.10}$$

and

$$\sqrt{C} = \frac{t_C}{(\pi - 2\sin^{-1}x)\sqrt{L}} \quad \text{and} \quad \sqrt{L} = \frac{t_C}{(\pi - 2\sin^{-1}x)\sqrt{C}}$$

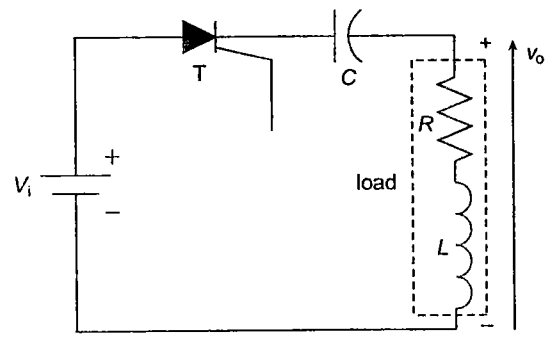
From (7.8), we get

$$L = \frac{V_i t_C}{I_{Cm}(\pi - 2\sin^{-1}x)} \quad \text{and} \quad C = \frac{I_{Cm} t_C}{V_i(\pi - 2\sin^{-1}x)} \tag{7.11}$$

7.5 LOAD COMMUTATED CHOPPERS

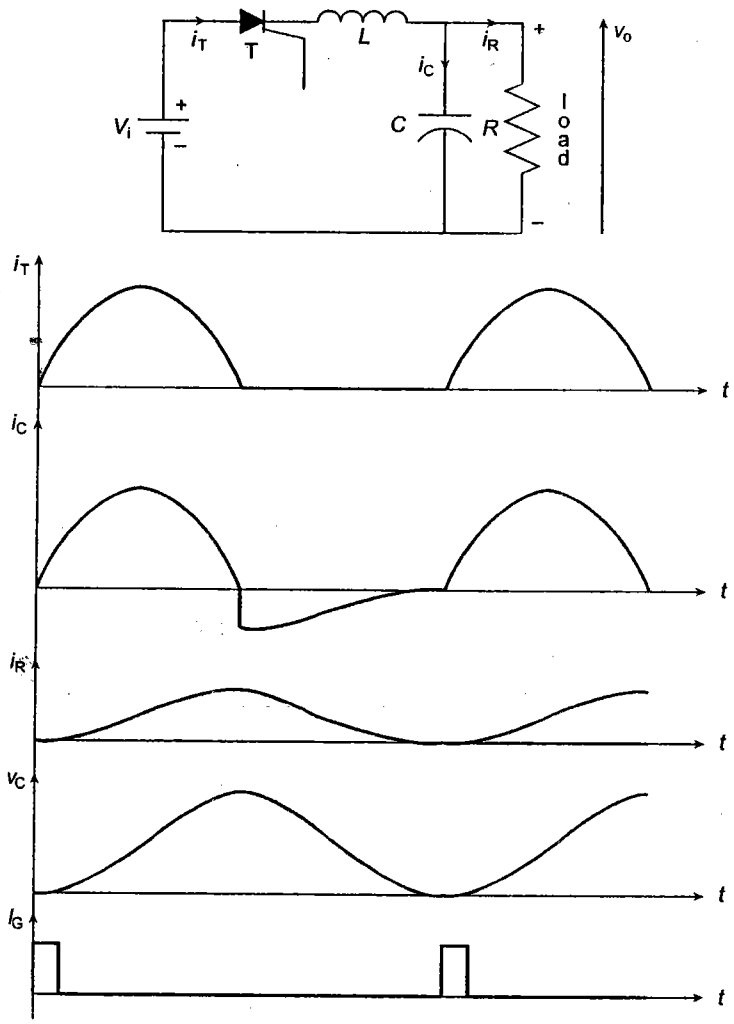
In such choppers, a separate external *LC* resonating circuit is not used to force the thyristor current to zero (below the holding current level). Different circuit topologies of thyristor based choppers are shown in Figs. 7.13 and 7.14. The load circuit current itself is made to oscillate for the commutation of a conducting thyristor. Thus a capacitor is connected with a highly inductive *RL* load circuit which forms an under-damped *RLC* circuit. Alternatively, an *RC* load circuit must be used with an inductor. For a lower value of the load resistance (*R*), an *RLC* series circuit is used (where $R^2 < 4L/C$). Otherwise, for a high value of *R*, the parallel *RC* branch is connected in series with *L*, as shown in Fig. 7.13(b). (A series *RLC* circuit is discussed in detail in Appendix 4). The *RLC* circuit with a parallel *RC* load (Fig. 7.13b), can also be analyzed in the same manner. In this case, during the on period of the thyristor, the capacitor gets charged. The current response in the LC resonating circuit is given by

$$i_C(t) = \frac{V}{\omega_r L} e^{-\xi t} \sin \omega_r t \tag{7.12}$$



(a) A load commutated thyristor based *RLC* series circuit

Figure 7.13 (*Cont.*)



(b) A load commutated thyristor based parallel RC circuit

Figure 7.13 Load commulated (RLC) chopper circuits.

where

$$\omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

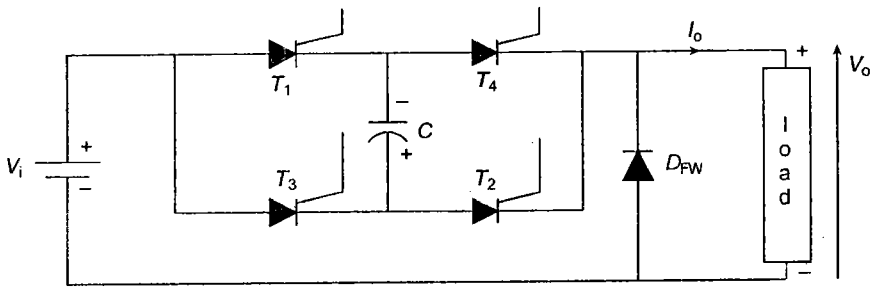
The current response of the resistor circuit is given by

$$i_R(t) = V_i\left(1 - e^{-\xi t}\cos\omega_r t - \frac{\xi}{\omega_r}e^{-\xi t}\sin\omega_r t\right) \tag{7.13}$$

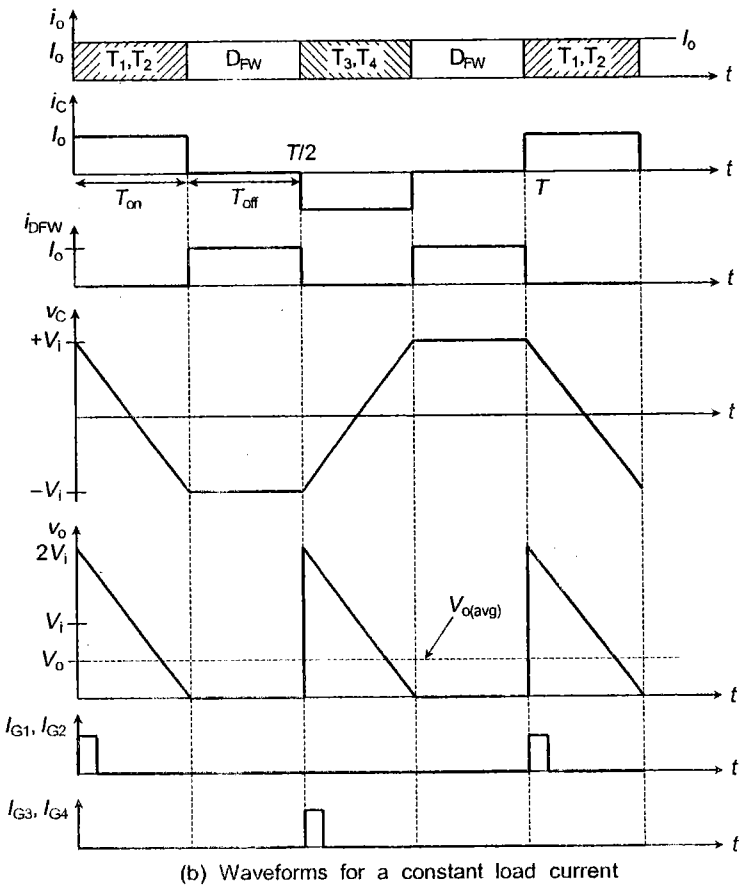
The thyristor current during on-period, $i_T(t) = i_C(t) + i_R(t)$. For successful commutation, R should be high. That is $R >> \sqrt{4L/C}$. The charging current of the capacitor passes through the thyristor

and ultimately reduces to zero; hence commutation takes place. Thereafter, the capacitor discharges through the load resistance before the next cycle starts.

Figure 7.14 shows the impulse commutated chopper circuit. One pair of thyristors, either T_1-T_2 or T_3-T_4, conducts while other pair remains off during that period. Initially, let the capacitor had been charged with $-V_i$ (Fig. 7.14a). At an instant, $t = 0$, T_1 and T_2 are triggered to carry a load current through the capacitor (C). The load voltage (v_o) is equal to $V_i + v_C$ ($\cong 2V_i$). Let the load current is constant, then the capacitor voltage swings linearly from $-V_i$ to $+V_i$. The output voltage



(a) circuit topology



(b) Waveforms for a constant load current

Figure 7.14 A load-commutated thyristor based chopper.

(v_o) decreases linearly to zero at T_{on} because of the capacitor voltage which reverses its polarity and becomes equal to V_i at this instant. When the capacitor acquires full-supply voltage, its current becomes zero leading to turning off of thyristors (T_1 and T_2). In fact, the capacitor is slightly overcharged causing freewheeling diode to conduct and that carries the load current up to $t = (T/2)$. Again T_3 and T_4 are triggered at this instant and the same process follows. The average output voltage is also controlled by keeping T_{on} or T_{off} constant and by varying the chopper frequency (f). Since the capacitor current is equal to Cdv/dt, we have

$$I_o = C\frac{2V_i}{T_{on}} \quad \text{and} \quad T_{on} = C\frac{2V_i}{I_o}$$

Since, $V_o = DV_i = V_i f T_{on}$, the output voltage is given by

$$V_o = \frac{2V_i^2 fC}{I_o}$$

At the maximum chopper frequency, the maximum average output voltage of chopper is given by

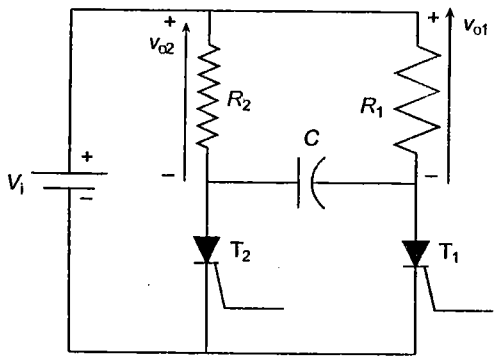
$$V_{o(max)} = \frac{2V_i^2 C}{I_o} f_{max} = V_i \quad \text{or} \quad f_{(max)} = \frac{I_o}{2V_i C}$$

The value of a capacitor chosen for the maximum chopper frequency and the maximum load current is given by

$$C = \frac{I_{o(max)}}{2V_i f_{max}} \tag{7.14}$$

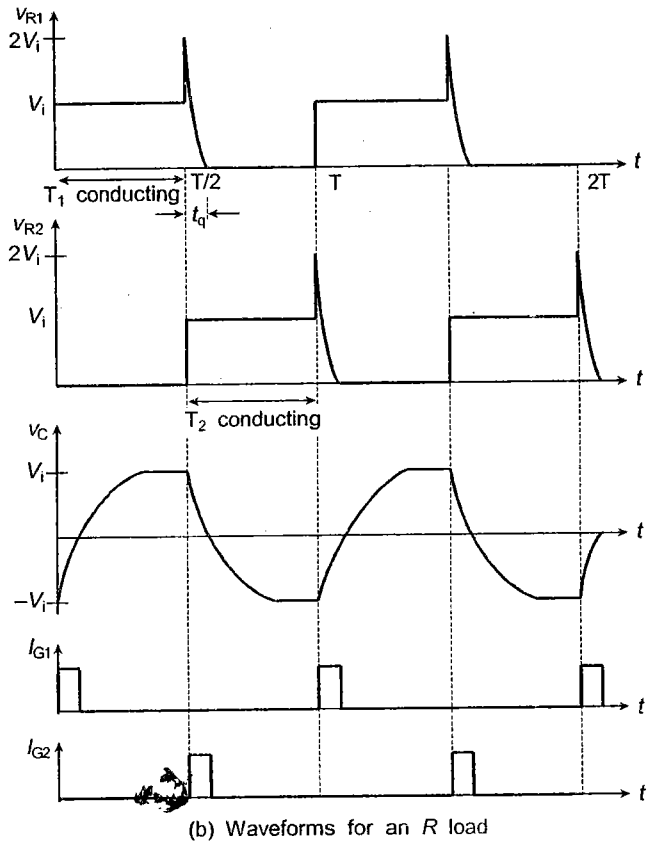
Figure 7.15 shows a complementary load commutation circuit used to transfer a current between two loads. Basically, it is a complementary-impulse commutation. When T_1 conducts, V_i appears at R_1 (load) and the load current is equal to V_i/R. Also, the capacitor gets charged through R_2 up to $+V_i$. The charging current (i_C) flows through (R_2, C and T_1). When T_2 is triggered to turn off T_1, the capacitor voltage ($v_C = V_i$) appears in series with V_i. Therefore, the load voltage becomes $2V_i$. The capacitor discharges through T_1 to turn it off and thereafter it gets charged through R_1 with opposite polarity ($v_C = -V_i$). At this instant, the capacitor or the load current is given by

$$i(t) = \frac{2V_i}{R} e^{-t/RC}$$



(a) Circuit diagram

Figure 7.15 (*Cont.*)



(b) Waveforms for an R load

Figure 7.15 A complimentary impulse-commutation chopper circuit (R load).

and

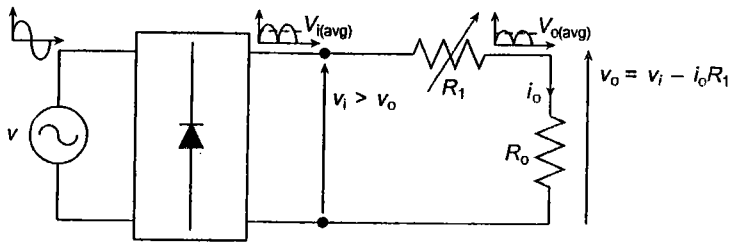
$$v_C(t) = V_i[1 - 2e^{-t/(Rc)}] \tag{7.15}$$

The time required to turn-off the thyristor successfully is equal to the commutation time (t_q) which can be found from the condition, $v_C(t_q) = 0$. It gives the value of t_q equal to $0.693RC$.

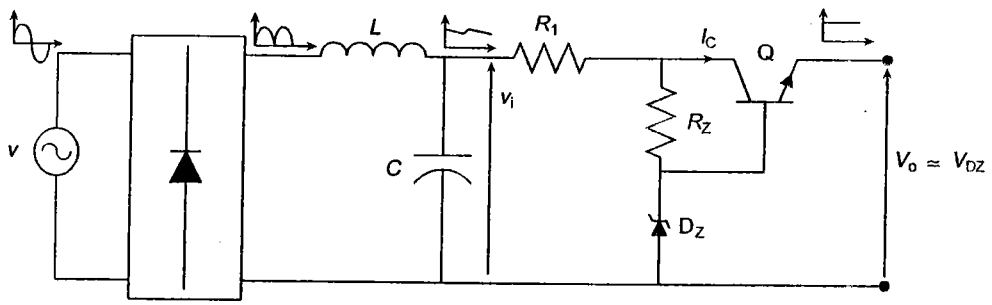
7.6 LINEAR DC POWER SUPPLIES

A dc power supply unit is an integral part of any electronic system. Normally, it is used for biasing of the electronic devices and IC. It is responsible for the reliable operation of the system. The main objective of the power supplies is to provide a constant regulated dc voltage with negligible amount of ripple irrespective of the fluctuation in the input voltage and/or load current. A dc power supply can provide the required biasing voltage levels, such as ±15 V, ±12 V, ±9 V, ±5 V, etc. There are different types of dc power supplies. The output dc voltage may be regulated or unregulated (with and without feedback arrangement). Similarly, the load may or may

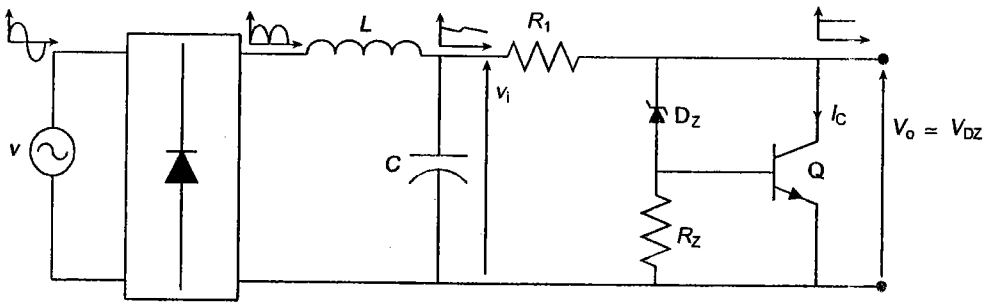
not be electrically isolated from the input voltage source. The basic principle of a linear power supply can be illustrated with the help of Fig. 7.16a. An unregulated input dc voltage (V_i) is obtained from the ac mains through an uncontrolled ac-to-dc converter using a diode bridge. V_o is



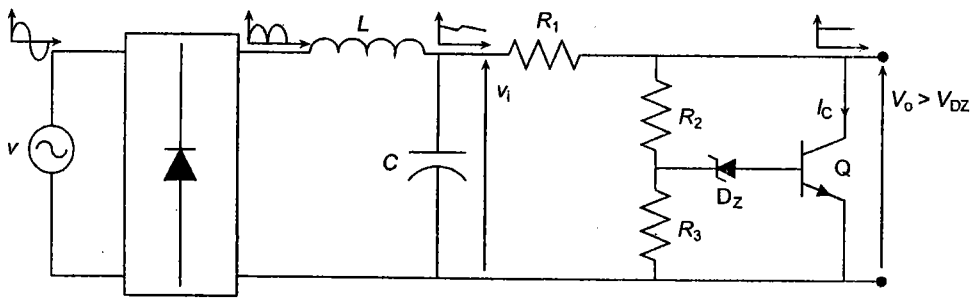
(a) Basic circuit topology of linear dc-dc regulators



(i) A linear dc series regulator



(ii) A linear dc shunt regulator

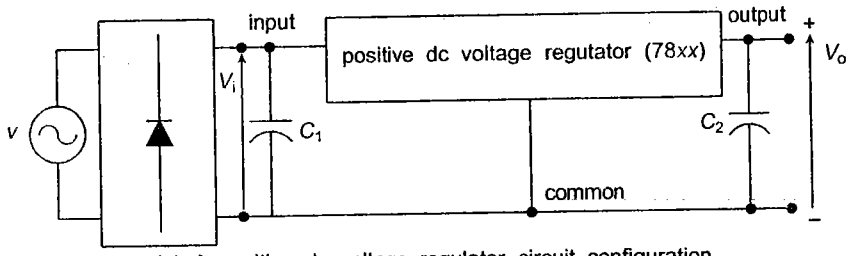


(iii) Another linear dc shunt regulator

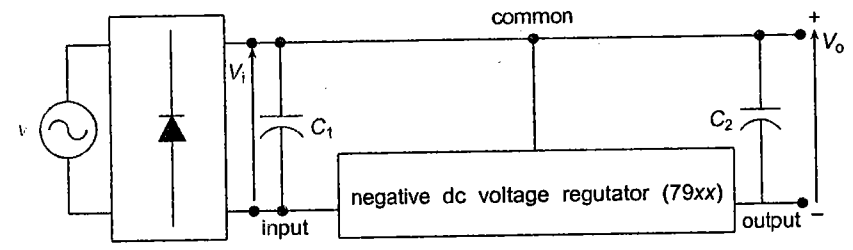
(b) Linear dc voltage regulators

Figure 7.16 Linear dc power supplies.

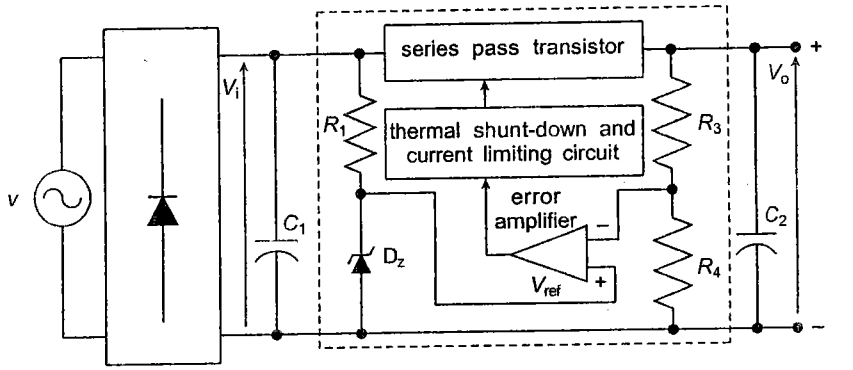
the regulated output dc voltage. The regulated circuit, in fact, acts as a variable resistor (R_1) to control voltage drops across it such that V_o remains constant at the desirable level. Figure 7.16b(i) shows a BJT based series regulator. Here, Q is a bipolar transistor, called series pass transistor. The base signal is provided such that the change in the input voltage appears across Q to keep V_o constant. If the input voltage (V_i) increases, then the base voltage, hence the base current, reduces. It increases v_{CE} voltage drop, hence V_o is maintained. Thus the transistor Q acts as a variable resistor and operates in the linear or active mode. Since all the time, the load current used to flow through the device (Q), the power loss is sufficiently large. It reduces the efficiency of the regulator, which is hardly 50%. This is the major drawback of a linear power supply, which limits its use to low-power applications only. Figure 7.16b(ii) shows a linear shunt voltage regulator circuit. When V_i is less than the desired output voltage, the Zener diode does not conduct. Therefore, no base current is supplied to Q and it remains off. When V_i exceeds the desired V_o level, D_z hence Q conducts. The additional transistor current causes more voltage drop across R_1, hence V_o is maintained to the desired level. Several custom-built ICs are available. The basic arrangements of commercially available three-terminal fixed voltage regulator IC are shown in Fig. 7.17. Fairchild A78*xx*, A78L*xx* and A78M*xx* series and LM340, LM341, LM109, LM117



(a) A positive dc voltage regulator circuit configuration



(b) A negative dc voltage regulator circuit configuration



(c) Block diagram

Figure 7.17 Custom-built fixed voltage dc regulators.

series of National Semiconductors come under this category. Both 78*xx* and 79*xx* series are available for positive- and negative-regulated dc output voltage, respectively. The term *xx* stands for the desired regulated output voltage (e.g. 7805 and 7912 stand for 5 V and −12 V, respectively). The fixed output voltage of the regulator varies from 2.6 to 20 V and current up to 1.5 A. These ICs are in ready-to-use form and require only bypass capacitors C_1 and C_2 to eliminate noise and disturbances. The capacitor C_1 should be either a ceramic disc type (>0.5 μF), a solid tantalum (>2 μF) or an electrolytic type (>25 μF). Similarly the capacitor C_2 should be either a ceramic disc type (>0.22 μF) or a solid tantalum (>1 μF). C_1 acts as a filter of voltage ripple and C_2 improves the transient response of regulator. There should be appropriate voltage ratings of these capacitors. The error signal from error amplifier increases for low value of the voltage across R_4 (hence V_o). Thus v_{CE} of series transistor reduces and V_o increases.

7.7 DC-TO-DC CONVERTERS WITHOUT ISOLATION

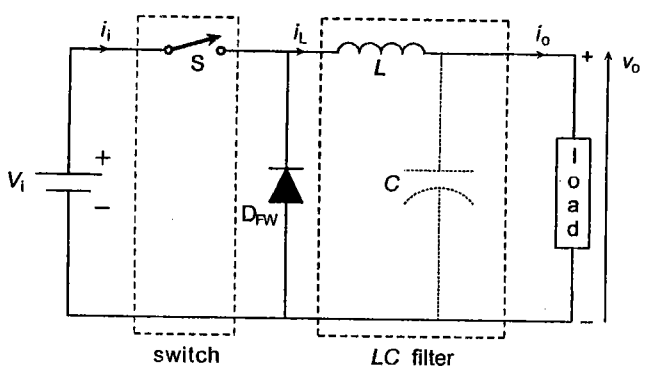
In such converters, the load impedance directly comes into contact with the input dc voltage source or through a circuit element. Therefore, the load is not electrically isolated from the input dc source. There are several thousand circuit topologies available for dc-to-dc converters. These converters are also called switch-mode dc converters. There are four most common and simple dc-to-dc converters without an electrical isolation:

(a) Buck or forward converters
(b) Boost converters
(c) Buck-boost converters
(d) Cuk converters

They are discussed in the following sections.

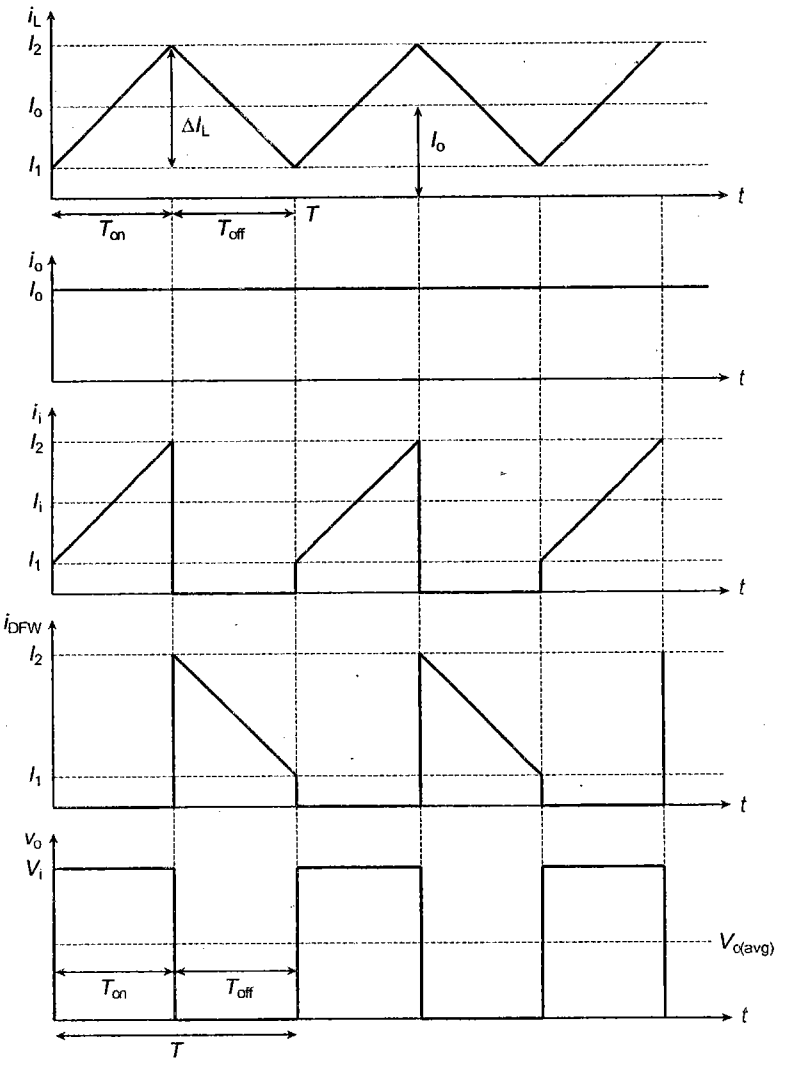
7.7.1 Buck or Forward Type

The buck converter is a dc-to-dc converter, where the output voltage can be controlled from zero to the input voltage level. Therefore, it is called a *step-down* converter. The circuit topology of the converter is shown in Fig. 7.18. The input dc voltage is applied to the load at a high frequency using



(a) Circuit topology of a buck dc-to-dc converter.

Figure 7.18 (*Cont.*)



(b) Waveforms for continuous conduction mode.

Figure 7.18 A buck dc-to-dc converter.

power semiconductor switches. Normally, these switches gate commutation device (e.g. MOSFET, IGBT, etc.). The inductor (L) stores energy during the on-period of switch. The stored energy transfers to capacitor, C through the free-wheeling diode D_{FW} during the off-period. If the switch (S) is turned on before the inductor current reaches zero level, it is called *continuous mode* of operation. If the inductor current reaches zero level before the next on-period, it is called *discontinuous mode* of operation. The relevant voltage and current waveforms for the two modes of operation are shown in Fig. 7.18. It is to be noted that if the switching frequency of the chopper is close to the natural frequency (ω_o) of the LC filter circuit, then the output voltage may be higher than the input voltage. This is discussed in detail in Chapter 9 (resonant converters).

MATHEMATICAL ANALYSIS

Certain assumptions are made to simplify the analysis which are:

- The switching device is ideal, therefore no switching loss takes place.
- The output voltage (V_o) is constant because of the large value of C, and
- The rise and fall of current through the inductor is linear. Therefore di/dt is constant which makes the voltage across $L(v_L = Ldi/dt)$ constant.

Continuous conduction mode During the on-period, the difference of input and output voltage is applied across the inductor. Since, $v_L = Ldi/dt$, the change in inductor current is given by

$$\Delta I_L = I_2 - I_1 = \frac{V_i - V_o}{L} T_{on} \quad \text{and} \quad T_{on} = \frac{L\Delta I_L}{V_i - V_o} \tag{7.16}$$

During the off-period, the free-wheeling diode D_{FW} conducts. The inductor current falls. One terminal of L reaches the negative potential due to conduction of D_{FW} and negative output voltage appears across L. Thus

$$-\Delta I_L = \frac{-V_o}{L} T_{off} \quad \text{or} \quad T_{off} = \frac{L\Delta I_L}{V_o} \tag{7.17}$$

Since, $V_o = DV_i$ and D is less than 1, V_o is also less than V_i. Also, from (7.16) and (7.17), the switching frequency is given by

$$f = \frac{1}{T} = \frac{1}{T_{on} + T_{off}} = \frac{V_o(V_i - V_o)}{V_i L \Delta I_L} \tag{7.18}$$

The ripple current can be found as

$$\Delta I_L = \frac{V_o(V_i - V_o)}{LV_i f}$$

$$= \frac{V_i D(1 - D)}{fL} \tag{7.19}$$

It shows that the current ripples can be reduced by increasing f and L. The maximum and minimum inductor current are given by

$$I_2 = I_o + \frac{\Delta I_L}{2} \tag{7.20}$$

and

$$I_1 = I_o - \frac{\Delta I_L}{2} \tag{7.21}$$

where I_o is the average or mean value of the load current i_o.

Discontinuous conduction mode In this mode of operation, $I_1 = 0$ (Fig. 7.19). Therefore, from (7.21) and (7.16), the average load current is given by

$$I_o = \frac{\Delta I_L}{2} = \frac{V_i - V_o}{2L} T_{on} = \frac{V_i - V_o}{2L} \frac{T_{on}}{T} T = \frac{(V_i - V_o)TD}{2L} = \frac{(V_i - V_o)D}{2Lf} \tag{7.22}$$

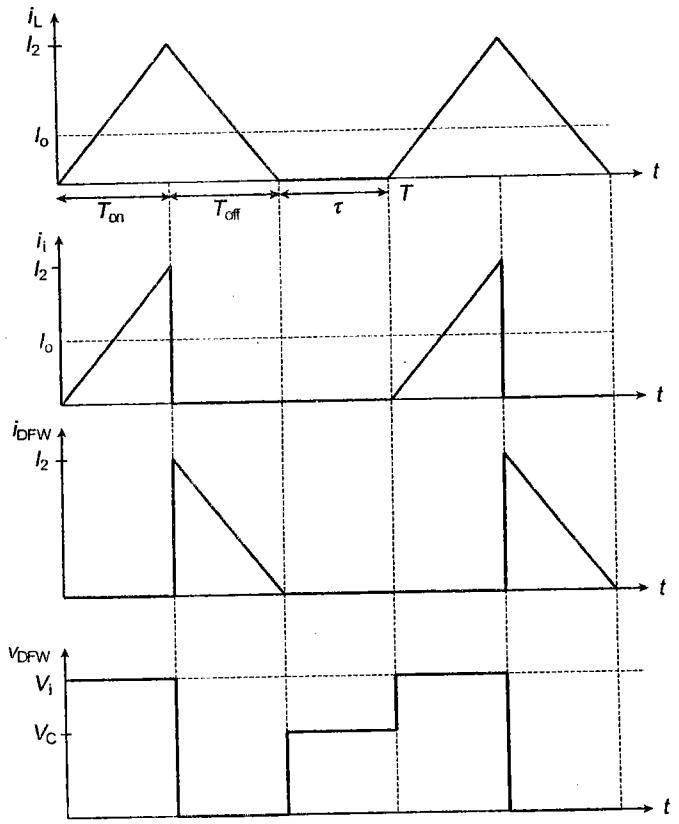


Figure 7.19 Discontinous conduction mode of buck type converter.

Because of a discontinuous current, a term (dead-time), τ is introduced. During τ period, the inductor current does not flow. Equating (7.16) and (7.17), for the rise and fall of the inductor current, gives

$$\Delta I_L = \frac{V_i - V_o}{L} T_{on} = \frac{V_o}{L}(T - T_{on} - \tau) \tag{7.23}$$

Therefore, it gives

$$\frac{V_o}{V_i} = \frac{D}{1 - (\tau/T)} \tag{7.24}$$

When the load current is just continuous (for $\tau = 0$), let the average value of inductor or load current, $I_o = I_{LJ}$. Therefore, for a given set of values of f, V_o, V_i, L and D, if the average load current (V_o/R) becomes less than I_{LJ}, then i_o will be discontinuous. The critical condition can be found by equating V_o/R equal to I_o, as given in (7.22).

Example 7.3 An RL load is connected to a 250 V, 400 Hz step-down (buck) chopper. The average load current is 100 A. The load resistance is 0.5 Ω. Find the minimum value of the inductor to limit the maximum ripple of the inductor current to 15%. Also, find the inductance for the worst-case ripple condition.

Solution The average voltage of load inductor is zero. Therefore the output voltage is given by

$$V_o = RI_o = 0.5 \times 100 = 50 \text{ V}$$

Then

$$D = \frac{V_o}{V_i} = \frac{50}{250} = 0.2$$

The ripple of the inductor current, $\Delta I_L = 0.15 \times 100 = 15$ A. From (7.20), the value of L is given by

$$L = \frac{V_o(V_i - V_o)}{\Delta I_L V_i f} = \frac{50(250 - 50)}{15 \times 250 \times 400} = 6.67 \text{ mH}$$

The worst case ripple condition, corresponds to the maximum ripple with respect to D. Therefore, from (7.20)

$$\frac{d(\Delta I_L)}{dD} = \frac{V_i}{fL}(1 - 2D) = 0$$

Which gives for the worst case, $D_w = 0.5$ and $V_o = D_w V_i = 0.5 \times 250 = 125$. Therefore, the worst-case inductance,

$$L_w = \frac{125 \times 125}{15 \times 250 \times 400} = 10.42 \text{ mH}$$

Example 7.4 For a given buck converter (dc-to-dc converter), find the maximum and minimum load current. It operates at 1 kHz and duty ratio is 0.2. If the operating frequency is increased to 5 kHz, what will be the effect on the load current? The load parameters are given as: R = 10 Ω and L = 10 mH.

Solution We have

$$T = \frac{1}{f} = \frac{1}{1 \times 10^3} = 10^{-3} \text{ s}$$

Therefore duty ratio, $D = T_{on}/T$, we get $T_{on} = DT = 0.2 \times 10^{-3}$ s.
We also have $R = 10$ Ω, $L = 10$ mH $= 0.01$ H. Then, from RLE circuits as given in Appendix (Figs. A13 and A14), the maximum value of the load current,

$$I_2 = \frac{V}{R}\frac{1 - \exp(-RT_{on}/L)}{1 - \exp(-RT/L)} = \frac{100}{10}\frac{1 - \exp(-10 \times 0.2 \times 10^{-3}/0.01)}{1 - \exp(-10 \times 1 \times 10^{-3}/0.01)} = 2.87 \text{ A}$$

Similarly, the minimum value of current is given by

$$I_1 = \frac{V}{R}\frac{\exp(RT_{on}/L) - 1}{\exp(RT/L) - 1} = 10\,\frac{e^{0.2} - 1}{e^1 - 1} = 1.29 \text{ A}$$

Therefore, $\Delta I = I_2 - I_1 = 1.58$ A.

When the frequency is increased to 5 kHz, then

$$T = \frac{1}{f} = \frac{1}{5 \times 10^3} = 0.2 \times 10^{-3} \text{ s}$$

T_{on} can be found as

$$T_{on} = DT = D\frac{1}{f} = \frac{0.2}{5 \times 10^3} = 0.04 \times 10^{-3} \text{ s}$$

The new value of I_2 is given by

$$I_2 = \frac{V}{R}\frac{1 - \exp(-RT_{on}/L)}{1 - \exp(-RT/L)} = \frac{100}{10}\frac{1 - e^{-0.04}}{1 - e^{-0.2}} = 2.1 \text{ A}$$

The new value of I_1 is given by

$$I_1 = \frac{V}{R}\frac{\exp(RT_{on}/L) - 1}{\exp(RT/L) - 1} = 10\frac{e^{0.04} - 1}{e^{0.2} - 1} = 1.84 \text{ A}$$

or

$$\Delta I = 2.1 - 1.84 = 0.26 \text{ A}$$

If operating frequency increases the variation or ripple in load current decreases. Alternatively, the ripple are decreased by increasing the L and C parameters of the filter circuit. It is evident that at high switching frequency, the requirement of L and C parameters of the filter circuit reduces and the converter becomes compact and light weight.

7.7.2 Boost Type Converters

This type of dc-to-dc converter is able to generate a constant output voltage (average value) more than the input voltage. The circuit topology is shown in Fig. 7.20. When the switch, S is turned on at $t = 0$, energy is stored in the inductor L. The current through the inductor is assumed to be rising linearly from a minimum level I_1 to a maximum level I_2. The diode is off as the output voltage V_o appears at the cathode (anode is at zero potential due to the conducting switch). Let the capacitance is very high, therefore V_o is constant and the capacitor supplies a constant load current. The equivalent switching circuit diagram for this period is shown in Fig. 7.21a. When the switch is turned off at $t = T_{on}$, it generates a negative voltage across it ($v_L = Ldi/dt$). Thus, a voltage $V_i + v_L$

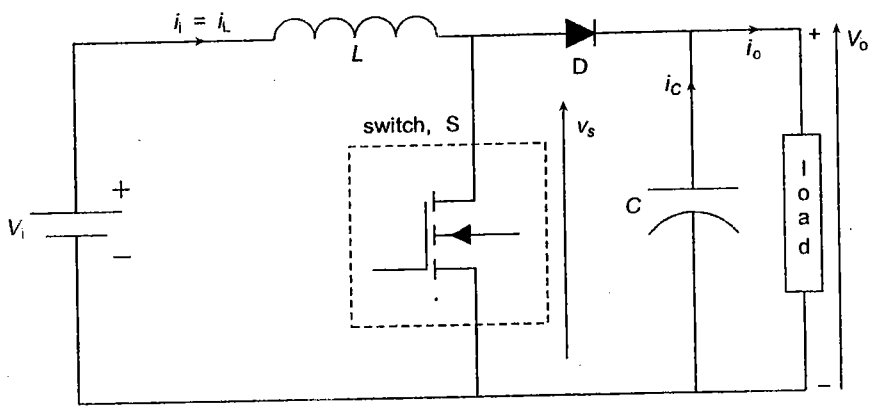
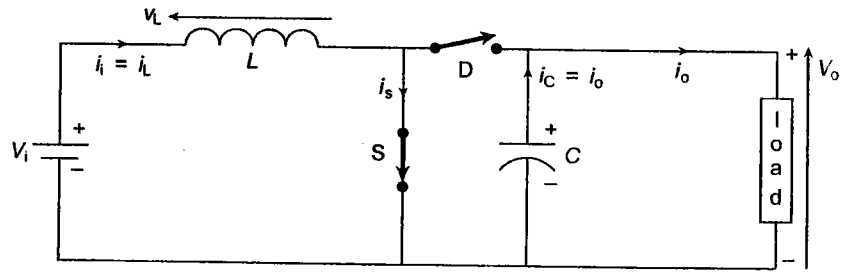
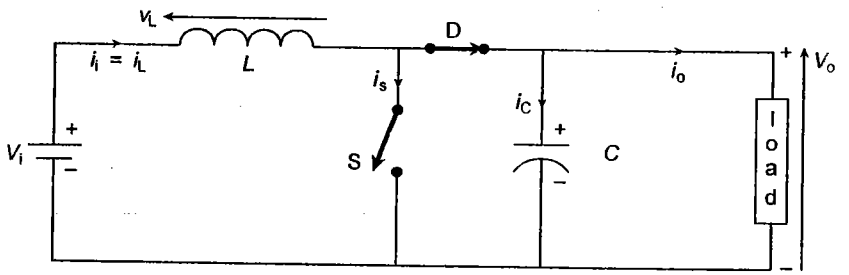


Figure 7.20 Circuit diagram of a boost conveter.

appears across the switch, which is greater than V_o. It turns on the diode D (anode being at a higher potential). The inductor current now charges the capacitor and the current flows through L, D, C and load. The stored energy of inductor is transferred to the capacitor and the inductor current falls linearly. In addition to the stored energy of the inductors, the energy from source is also fed to the load. The equivalent circuits for different switching conditions are shown in Fig. 7.21.



(a) Mode I, when switch S is on ($0 < t < T_{on}$)



(b) Mode II, when switch S is off ($T_{on} < t < T$)

Figure 7.21 Different modes of switching of boost converters.

In this type of converter, the output current is always continuous, while the input current may be continuous or discontinuous. Moreover, the capacitor voltage or V_o remains constant due to high value of C. The waveforms for two modes are shown in Fig. 7.22.

MATHEMATICAL ANALYSIS

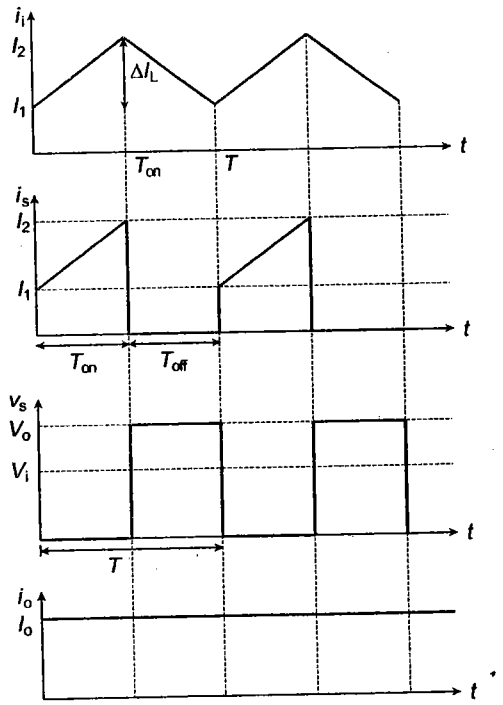
The assumptions are same as it was made in for the buck converters.

Continuous conduction mode The voltage impressed across the inductor during on-period is V_i. During this period, the current rises linearly from a minimum level, I_1 to a maximum level, I_2. Therefore,

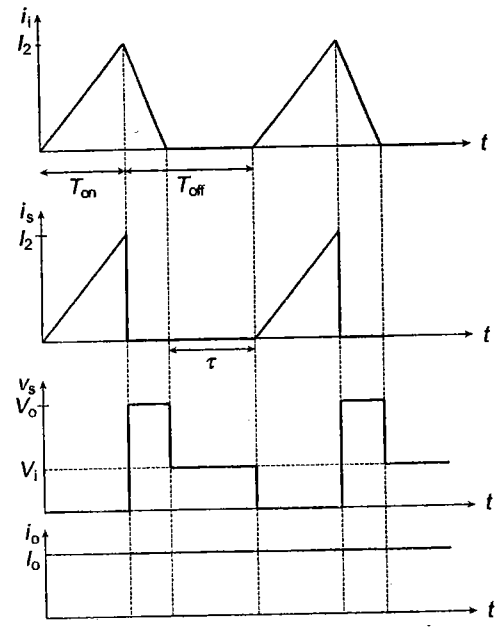
$$v_L = L\frac{I_2 - I_1}{T_{on}} = V_i \quad \text{or} \quad T_{on} = \frac{L\Delta I_L}{V_i} \tag{7.25}$$

The voltage impressed across the inductor during off-period is $V_o - V_i$ and the current drops linearly from the maximum level, I_2 to the minimum level, I_1. Therefore, the voltage across the inductor is given by

$$v_L = \frac{L(I_2 - I_1)}{T_{off}} = V_o - V_i \quad \text{or} \quad T_{off} = \frac{L\Delta I_L}{V_o - V_i} \tag{7.26}$$



(a) Continuous mode



(b) Discontinuous mode

Figure 7.22 Waveforms of different modes of operation of a boost converter.

From (7.25) and (7.26), equating for ΔI_L, it gives

$$\Delta I_L = \frac{V_i T_{on}}{L} = \frac{V_o - V_i}{L} T_{off}$$

or

$$V_o = \frac{V_i T_{on} + V_i T_{off}}{T_{off}} = \frac{T_{on} + T_{off}}{T_{off}} V_i = V_i \frac{T}{T_{off}}$$

or

$$V_o = \frac{V_i}{1 - D} \tag{7.27}$$

It is evident from the above equation, for $D = 0$ to $D = 1$, $V_o \geq V_i$, and ideally, V_o may vary from V_i to infinite. Therefore, in general, V_o is greater than or equal to V_i. However, due to parasitic parameters stray inductance and capacitance of the converter circuits, after attaining certain high-voltage level, V_o decreases for D close to 1.

As the switching device is considered to be lossless, the power input ($V_i I_i$) and power output ($V_o I_o$) of the converter is same. Therefore, from (7.27)

$$V_i I_i = V_o I_o = \frac{V_i I_o}{1 - D} \quad \text{or} \quad I_i = \frac{I_o}{1 - D} \tag{7.28}$$

Substituting for T_{on} and T_{off}, from (7.25) and (7.26), the switching frequency is given by

$$f = \frac{1}{T} = \frac{1}{T_{on} + T_{off}} = \frac{V_i (V_o - V_i)}{V_o \Delta I_L L} \tag{7.29}$$

Therefore, from (7.27) and (7.29), the ripple current is given by

$$\Delta I_L = \frac{V_i (V_o - V_i)}{V_o L f} = \frac{V_i}{fL}\left(1 - \frac{V_i}{V_o}\right) = \frac{V_i}{fL}[1 - (1 - D)]$$

or

$$\Delta I_L = \frac{V_i D}{fL} \tag{7.30}$$

Discontinuous conduction mode In this mode, i_L reduces to zero during $(T_{off} - \tau)$ period ($I_1 = 0$). From (7.25) and (7.26), equating for ΔI_L, it gives

$$\Delta I_L = \frac{V_i T_{on}}{L} = \frac{(V_o - V_i)(T_{off} - \tau)}{L}$$

or

$$\frac{V_o}{V_i} = \frac{1 - (\tau/T)}{(T_{off} - \tau)/T} = \frac{1 - (\tau/T)}{1 - D - (\tau/T)}$$

or

$$V_o = \frac{1 - (\tau/T)}{1 - D - (\tau/T)} V_i \tag{7.31}$$

7.7.3 Buck-boost Type

The buck-boost type dc-dc converters give the output voltage, both more than as well as less than the input voltage level. It depends upon whether the duty ratio is more than 50% or less than 50%, respectively. However, the output voltage has opposite polarity that of the input voltage. The circuit topology is shown in Fig. 7.23. When the switch is on, the inductor stores energy from the supply. When the switch turns off at the end of the on-period, the fall in inductor current

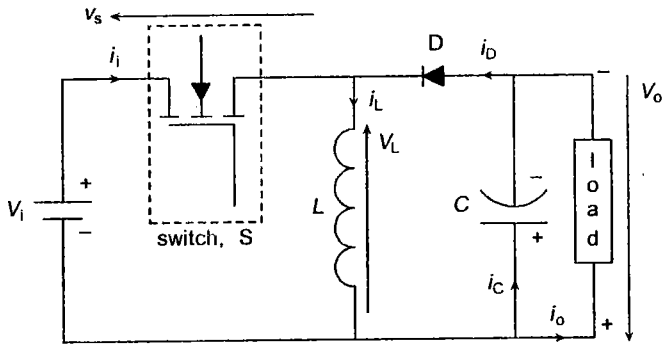


Figure 7.23 Circuit diagram of a buck-boost converter.

generates a negative voltage across the inductor (upper side negative). It makes the cathode of the diode negative and provides another path of current through the capacitor and the load. During the off-period, the stored inductor energy is transferred to the capacitor and the load. Both the input and output current are discontinuous. However, the inductor current could be continuous or discontinuous but V_o remains constant due to large value of C. Current and voltage waveforms for both the conditions are shown in Fig. 7.24.

Mathematical Analysis

The assumptions are same as it was made in the previous cases.

Continuous conduction mode During the on-period, the voltage across the inductor is V_i and the current rises linearly from a minimum level, I_1 to a maximum level, I_2. Thus, the inductor voltage is given by

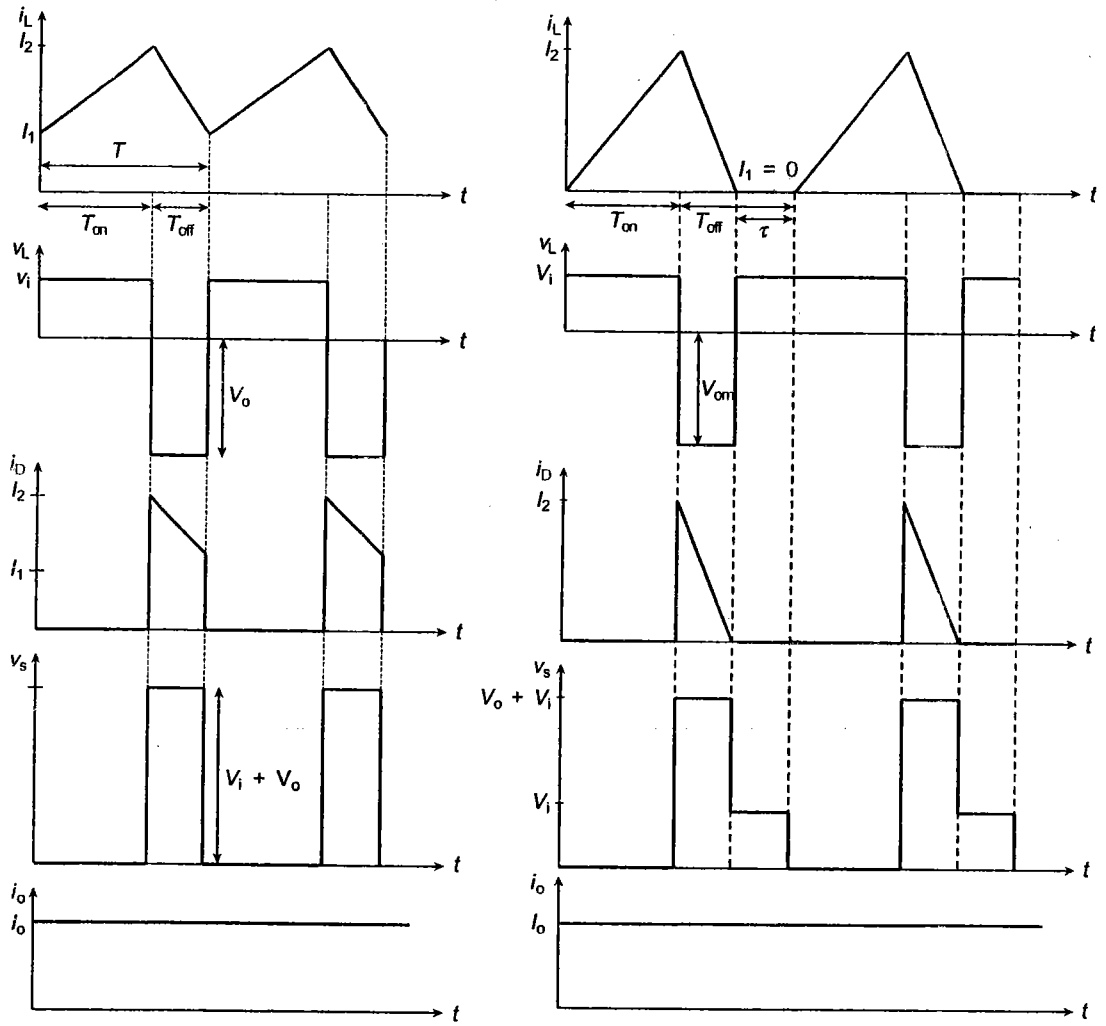
$$v_L = L\frac{I_2 - I_1}{T_{on}} = V_i \quad \text{or} \quad T_{on} = \frac{L\Delta I_L}{V_i} \tag{7.32}$$

During the off-period, the voltage across the inductor is negative and the current falls from I_2 to I_1, the inductor voltage is given by

$$v_L = L\frac{\Delta I_L}{T_{off}} = -V_o \quad \text{or} \quad T_{off} = -\frac{L\Delta I_L}{V_o} \tag{7.33}$$

From (7.32) and (7.33), equating for ΔI_L, it gives

$$\Delta I_L = \frac{V_i T_{on}}{L} = -\frac{V_o T_{off}}{L} \quad \text{or} \quad V_o = -\frac{T_{on}}{T_{off}}V_i = -V_i\frac{D}{1-D} \tag{7.34}$$



(a) Continuous mode (b) Discontinuous mode

Figure 7.24 Current and voltage waveforms of a buck-book converter.

It is evident from (7.34), the converter operates in buck mode when $D < 0.5$ and therefore $V_o < V_i$. Also, it operates in boost mode when $D > 0.5$ and therefore $V_o > V_i$.

For a lossless converter system, the switching loss in the device is zero. Both the input power ($V_i I_i$) and the output power ($V_o I_o$) are equal. Therefore, from (7.34),

$$I_i = I_o \frac{V_o}{V_i} = -I_o \frac{D}{1-D} \tag{7.35}$$

Substituting for T_{on} and T_{off}, the switching frequency is given by

$$f = \frac{1}{T} = \frac{1}{T_{on} + T_{off}} = \frac{V_i V_o}{L \Delta I_L (V_o - V_i)} \tag{7.36}$$

Also, the ripple current through the inductor is given by

$$\Delta I_L = \frac{V_i V_o}{fL(V_o - V_i)} = \frac{V_i D}{fL} \tag{7.37}$$

Discontinuous conduction mode During this mode, i_L reduces to zero in $(T_{off} - \tau)$ period ($I_1 = 0$). When the switch is on, the inductor voltage is given by

$$v_L = L\frac{I_2 - I_1}{T_{on}} = V_i \quad \text{or} \quad \Delta I_L = \frac{V_i}{L} T_{on} \tag{7.38}$$

When the switch is off, the inductor voltage is given by

$$v_L = L\frac{\Delta I_L}{T_{off} - \tau} = -V_o \quad \text{or} \quad \Delta I_L = -\frac{V_o}{L}(T_{off} - \tau) \tag{7.39}$$

Equating (7.38) and (7.39) for ΔI_L, it gives

$$\frac{V_i}{L} T_{on} = -\frac{V_o}{L}(T_{off} - \tau)$$

$$V_o = -\frac{T_{on}}{T_{off} - \tau} V_i = -\frac{D}{1 - D - (\tau/T)} V_i \tag{7.40}$$

Circuit Topology of Converters

All the three types of dc-dc converter discussed in preceding sections can be realized by cyclic rotation of the inductor, diode and a static switch, as shown in Fig. 7.25.

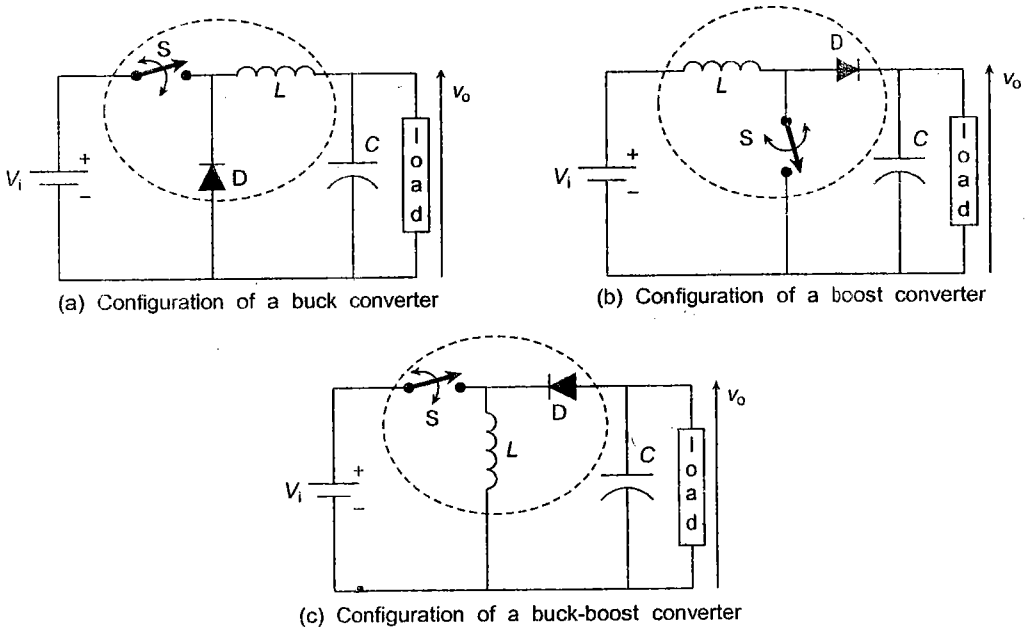
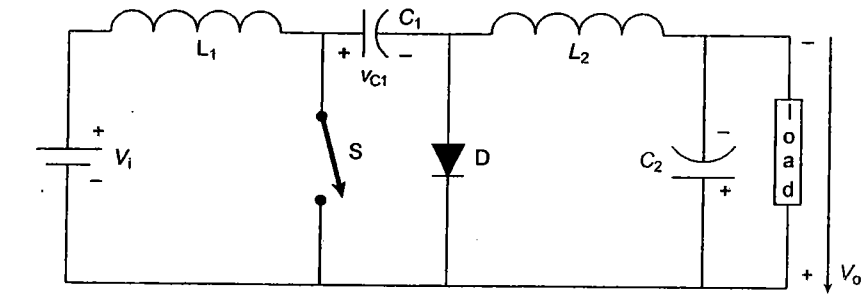


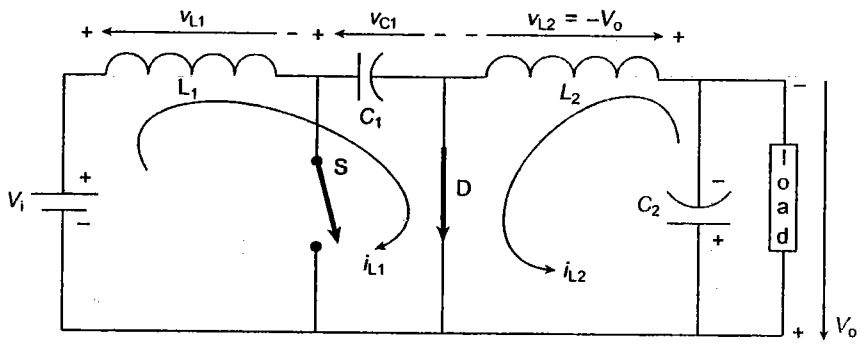
Figure 7.25 Three types of dc-dc converters realized by cyclic rotation of circuit components.

7.7.4 Cuk Converters

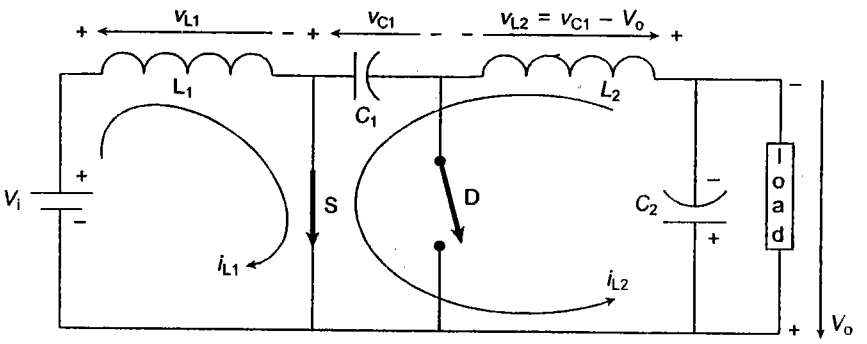
This is a dc-dc converter which transfers energy from the source to the load, both during on-period and off-period of switching. This is a highly efficient dc-dc converter, where the capacitor works as an energy storing element. The input current is continuous and the polarity of the output voltage is reverse (opposite of the input voltage). The output voltage may be more or less than the input voltage. Thus it operates in both buck and boost mode which depends upon the duty-ratio. The circuit topology of Cuk converter is shown in Fig. 7.26.



(a) Circuit diagram



(b) During off period



(c) During on period

Figure 7.26 Circuit diagram of Cuk converters.

Initially the switch S is off and D conducts (as D is forward biased because of the input source voltage). The operation of the circuit starts after C_1 is fully charged. Now, as the switch (S) is turned on at $t = 0$, the diode (D) is reversed biased because of v_{C1}. Now, the capacitor (C_1) discharges through the load and the capacitor (C_2). The inductor (L_1) stores energy from the source. When the switch (S) is turned off at $t = T$, the capacitor (C_1) charges through the source and L_2 transfers its stored energy to the load. The current and voltage waveforms are shown in Fig. 7.27.

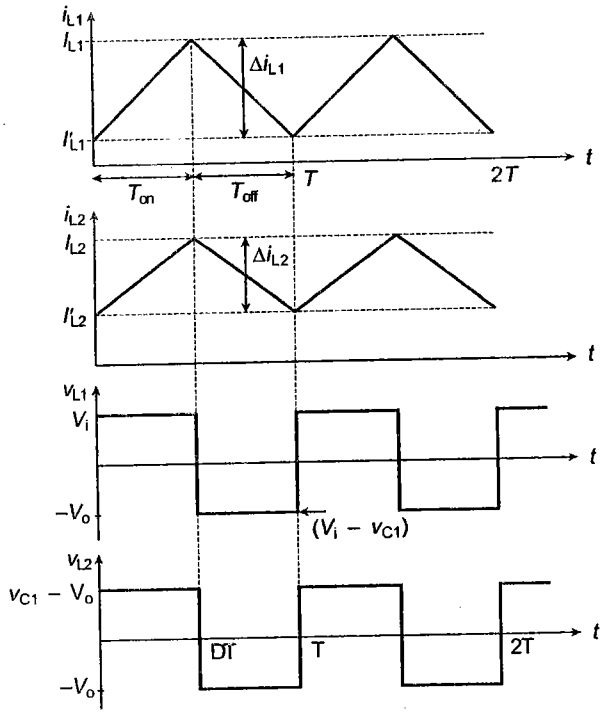


Figure 7.27 Waveforms of Cuk converters.

MATHEMATICAL ANALYSIS

The assumptions made for the previous cases are also applied here. When the switch (S) is on, the current through the inductor (L_1) rises linearly from the minimum level (I'_{L1}) to the maximum level (I_{L1}). The inductor voltage is given by

$$v_{L1} = L_1 \frac{I_{L1} - I'_{L1}}{T_{on}} = V_i \quad \text{or} \quad T_{on} = \frac{L_1 \Delta I_{L1}}{V_i} \tag{7.41}$$

where $\Delta I_{L1} = I_{L1} - I'_{L1}$.

The current falls linearly from I_{L1} to I'_{L1}, when the switch (S) is off. Therefore, the inductor voltage is given by

$$v_{L1} = L_1 \frac{-\Delta I_{L1}}{T_{off}} = -(v_{C1} - V_i) \quad \text{or} \quad T_{off} = \frac{L_1 \Delta I_{L1}}{v_{C1} - V_i} \tag{7.42}$$

Equating for ΔI_{L1}, from (7.41) and (7.42), it gives

$$\Delta I_{L1} = \frac{V_i T_{on}}{L_1} = \frac{(v_{C1} - V_i) T_{off}}{L_1} \quad \text{or} \quad v_{C1} = \frac{V_i}{1 - D} \tag{7.43}$$

Similarly, the current through L_2 varies linearly between a maximum level (I_{L2}) to a minimum level (I'_{L2}). The inductor voltage is equal to the sum of v_{C1} and V_o. Therefore,

$$v_{L2} = v_{C1} - V_o = L_2 \frac{\Delta I_{L2}}{T_{on}} \quad \text{or} \quad T_{on} = \frac{L_2 \Delta I_{L2}}{v_{C1} - V_o} \tag{7.44}$$

where $\Delta I_{L2} = I_{L2} - I'_{L2}$.

When the switch (S) is off, the inductor current falls linearly from I_{L2} to I'_{L2}. The inductor voltage is given by

$$v_{L2} = -V_o = -L_2 \frac{\Delta I_{L2}}{T_{off}} \quad \text{or} \quad T_{off} = L_2 \frac{\Delta I_{L2}}{V_o} \tag{7.45}$$

Equating for ΔI_{L2}, from (7.44) and (7.45), it gives

$$\Delta I_{L2} = \frac{(v_{C1} - V_o) T_{on}}{L_2} = \frac{V_o T_{off}}{L_2} \quad \text{or} \quad v_{C1} = \frac{V_o}{D} \tag{7.46}$$

Equating for V_{C1}, from (7.43) and (7.46), it gives

$$V_o = \frac{D}{1 - D} V_i \tag{7.47}$$

The above equation shows that the converter operates in boost mode for $D > 0.5$ and it operates in buck mode for $D < 0.5$. Also, V_o becomes equal to V_i for $D = 0.5$. For an ideal or lossless converter system, the input and the output powers are equal ($V_i I_i = V_o I_o$). Therefore,

$$I_i = \frac{V_o}{V_i} I_o = \frac{D}{1 - D} I_o \tag{7.48}$$

The switching frequency is given by

$$f = \frac{1}{T} = \frac{1}{T_{on} + T_{off}} = \frac{L_2 \Delta I_{L2} v_{C1}}{V_o (V_{C1} + V_o)} \quad \text{or} \quad \Delta I_{L2} = \frac{V_o (v_{C1} + V_o)}{L_2 v_{C1} f} \tag{7.49}$$

From (7.46) and (7.47), putting for v_{C1} and V_o, it gives

$$\Delta I_{L2} = \frac{D V_i}{f L_2} \tag{7.50}$$

Example 7.5 Find the duty-ratio of a Cuk converter operating at 25 kHz to obtain an output voltage, 200 V. The input dc voltage supply consists of two series connected 12-V batteries. Also, find the voltage across the switch.

Solution The input voltage, $V_i = 2 \times 12$ V = 24 V. The output voltage is given by

$$V_o = \frac{D}{1 - D} V_i \quad \text{or} \quad D = \frac{V_o}{V_o + V_i} = \frac{200}{200 + 24} = 0.893$$

The voltage across the switch is v_{C1} that appears during the off-period, which is given by

$$v_{C1} = \frac{V_i}{1-D} = \frac{24}{1-0.893} = 224.3 \text{ V}$$

Therefore, the voltage rating of the switch is selected according to the maximum allowable duty ratio (D_{max}) of the converter.

7.8 DC-TO-DC CONVERTERS WITH ISOLATION

Sometimes, several regulated dc output voltage of different levels are required (e.g. to obtain different output ground and independent regulated dc voltage source, viz., +5 V, +9 V, +12 V, −12 V, etc.). There are several other advantages of using isolated version of dc-dc converters. Electrical isolation between the source and the load is also activated for protection purpose. A step-up or step-down output can be obtained by simply changing the turn ratio of the isolating transformer, as shown in Fig. 7.28. The limitation of original buck-boost converter (reverse polarity output voltage) can be eliminated by simply interchanging the isolating transformer secondary connection. This type of isolated dc-dc converters are used in switched mode power supply (SMPS) discussed in Chapter 10. Here four basic configurations are discussed: fly-back, forward, push–pull and half-bridge/full-bridge.

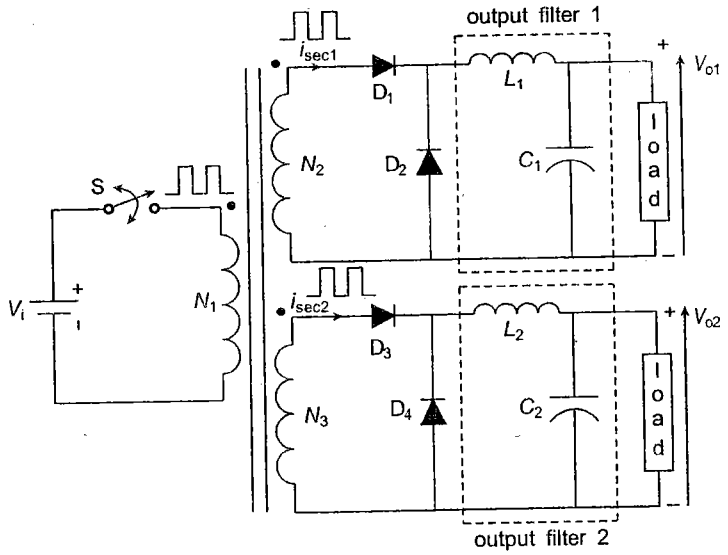
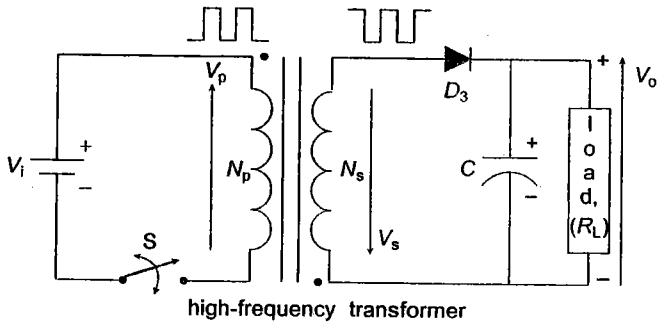


Figure 7.28 Multiple isolated outputs of a forward dc converter.

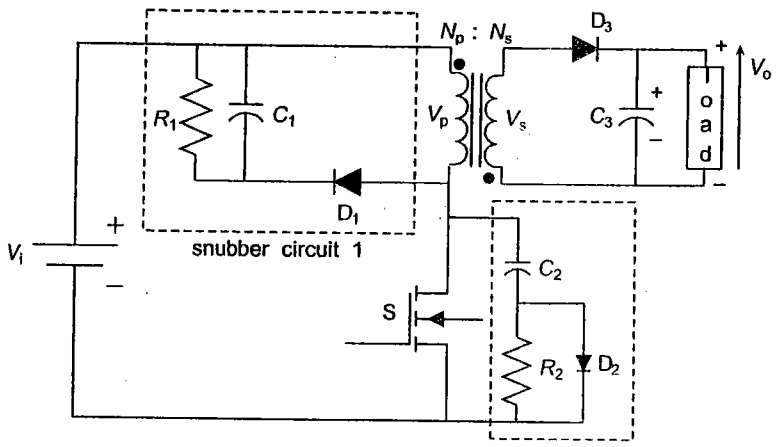
7.8.1 Flyback Converters

For high frequency applications, a ferrite-core transformer is used which provides electrical isolation. In normal silicon–steel core transformers, the hysteresis-loop is quiet wide. It leads to a

high hysteresis loss because of high switching frequency of the chopper or dc converters. A ferrite-core transformer offers the advantage of very low hysteresis loss because of very narrow B-H loop. The basic circuit topology of a flyback converter is shown in Fig. 7.29.



(i) Circuit topology



(ii) Actual circuit

Figure 7.29 An isolated output flyback dc-to-dc converter.

When the switch (S) is on, the source voltage is directly applied to the primary of the transformer, inducing an emf in the secondary. But the opposite polarity of the voltage (same voltage polarity at dotted terminals), keeps the diode (D_3) reverse biased. Thus current does not flow in the secondary winding. The primary winding of the transformer behaves like an inductor storing energy in its magnetic field. When S is turned off, it induces a negative voltage due to decreasing current ($v_L = -di/dt$). Then the diode becomes forward biased and conducts. Thus, the stored energy is transferred to the load during the off-period. The current and voltage waveforms of the high-frequency transformer (assuming a lossless core) is shown in Fig. 7.30. The switching device is always in series with the primary winding. Even in case of short circuit at load terminal, it does not directly reflect during the conduction period of the device.

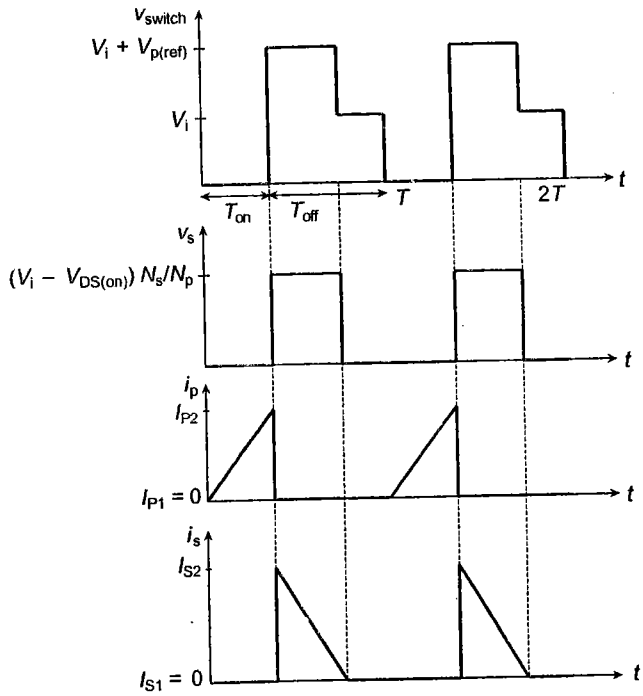


Figure 7.30 Waveforms of an isolated flyback converter.

MATHEMATICAL ANALYSIS

For the sake of simplicity of analysis, the resistance and leakage inductance of windings are neglected. When the switch (S) is turned on, the voltage across the primary winding is given by

$$V_p = V_i - V_{DS(on)} \tag{7.51}$$

where $V_{DS(on)}$ is on-state voltage drop of the switch, e.g. MOSFET or any other switching device.

When the switch is on, the secondary voltage is given by

$$V_S = \frac{N_s}{N_p}[V_i - V_{DS(on)}] \tag{7.52}$$

where N_p and N_s are numbers of turns in primary and secondary windings, respectively.

When the switch (S) is off, the voltage across the secondary winding is given by

$$V_s = V_{D3} + V_{C3}$$

where V_{D3} is the voltage across diode (D_3) and V_{C3} is the voltage across capacitor (C_3). During the off-period, a reflected voltage will appear across the primary winding which is given by

$$V_{p(refl)} = V_s \frac{N_p}{N_s} \tag{7.53}$$

The reflected primary voltage becomes zero, as soon as the secondary current reaches zero. The voltage waveform is shown in Fig. 7.31. To avoid core saturation, there should not be any dc component of voltage across the transformer primary (i.e. the volt–time area during on-period and off-period should be equal).

$$[V_i - V_{DS(on)}]T_{on} = V_{p(refl)}T_{off}$$

or

$$V_{p(refl)} = [V_i - V_{DS(on)}]\frac{T_{on}/T}{T_{off}/T} = [V_i - V_{DS(on)}]\frac{D}{1-D} \tag{7.54}$$

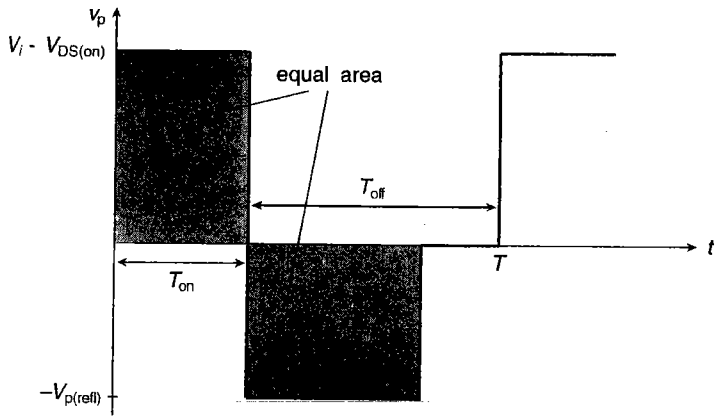


Figure 7.31 Waveform of primary winding voltage of flyback converters.

Thus, the output voltage, from (7.53) and (7.54), is given by

$$V_o = V_s - V_{D3} = \frac{N_s}{N_p}[V_i - V_{DS(on)}]\left(\frac{D}{1-D}\right) - V_{D3}$$

Therefore, sufficient time is required for the flux balance of core. The off-period (T_{off} or $1 - D$) should be less than 50%. The maximum voltage across the switch is given by

$$V_{DS(on)max} = V_i + V_{p(refl)} = V_i + \frac{N_p}{N_s}V_o \tag{7.55}$$

The expression for average and rms value of input current can be found with the help of energy storage in the primary winding. The energy stored in the inductor of primary winding (L_P) of the transformer is given by

$$W_P = \frac{1}{2}L_P I_{P(max)}^2 \tag{7.56}$$

where L_P and I_P are the inductance and the rms value of current of primary winding.

The average output power supplied to the load is given by

$$P_o = \frac{1}{2}fL_P I_{p(max)}^2 \tag{7.57}$$

where $I_{p(max)}$ is the peak or maximum current of the primary winding.

When the switch is on, the input current may be assumed to rise linearly. Therefore, the voltage of the primary winding (Ldi/dt) is given by

$$V_i = L_p \frac{I_{p(max)}}{T_{on}} = L_p I_{p(max)} \frac{T}{T_{on}} \frac{1}{T} = L_p I_{p(max)} \frac{1}{D} f$$

or

$$L_p I_{p(max)} = \frac{DV_i}{f} \tag{7.58}$$

From (7.57), it gives

$$I_{p(max)} = \frac{2P_o}{V_i} \frac{1}{D} \tag{7.59}$$

For a lossless system, the input power ($V_i I_i$) is equal to the output power ($P_o = V_o I_o$). Therefore, from (7.59), the average input current is given by

$$I_i = \frac{V_o I_o}{V_i} = \frac{P_o}{V_o} = \frac{I_{p(max)}}{2} D \tag{7.60}$$

The rms value of the primary current is given by

$$I_{p(rms)} = I_{p(max)} \sqrt{\frac{D}{3}} \tag{7.61}$$

The load filter or tank capacitor (Fig. 7.29), supplies the output voltage to the load during on-period of the device. The ripple voltage is inversely proportional to the time constant $C_3 R_L$. The per unit ripple factor is given by

$$\frac{\Delta V_o}{V_o} = \frac{T_{on}}{CR_L} \tag{7.62}$$

7.8.2 Forward Converters

The circuit topology of a forward converter is shown in Fig. 7.32. It has an isolating transformer, with three windings wound on a common core, i.e. the primary winding, the secondary winding

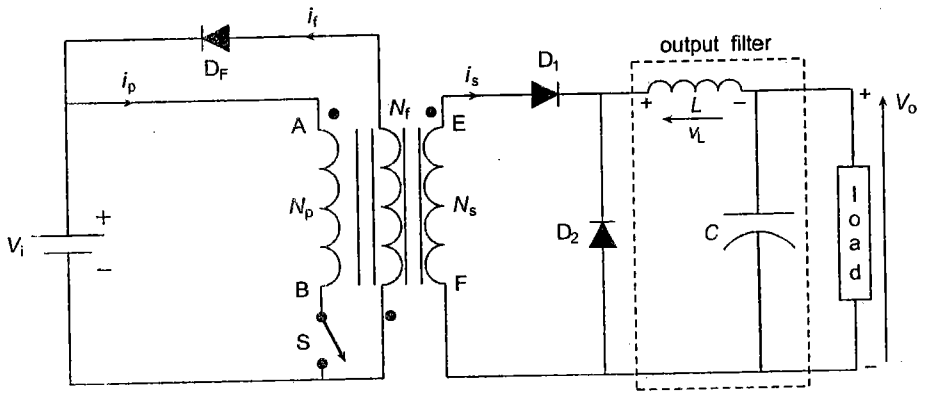


Figure 7.32 Circuit configuration of a forward converter with regenerative feedback winding.

and the feedback winding. The energy transfer takes place (from source to load), when the switch (S) is on. The on-period is called *forward mode* of operation.

When the switch (S) is on, the supply voltage is applied to the primary winding (AB) which induces a voltage in the secondary with terminal E as positive. Thus D_1 becomes forward biased. The energy transfers to load through diode D_1 and L stores the energy. In the mean time, energy is also stored in the magnetic field of the transformer and the core is set. The terminal A or cathode of D_F is positive during this period, therefore D_F remains off. When the switch (S) is turned off, the fall of inductive current of the primary winding (N_p) generates a negative voltage ($v_L = Ldi/dt$) across it. The lower terminal of the feedback winding and E becomes negative. Anode of D_F becomes positive and anode of D_1 become negative, and D_1 turns off. At this condition, D_2 conducts and stored energy of L flows to the load. The induced voltage across the feedback winding is more than the supply voltage, thus the feedback diode D_F turns on. The trapped energy in the common magnetic field of isolating transformer is returned back to the supply. The voltage across the feedback winding is held at V_i, till the feedback diode D_F continues to conduct. The diode D_F stops conduction when all the stored energy is returned back and the transformer core is reset (due to opposite direction of current). If the turn ratio, $N_p/N_f = 1$, the maximum voltage across the switch is $2V_i$ (as the potential of BA is $+V_i$). Normally, the duty-ratio limit (D_{max}) is 50%. It ensures the required volts-second to reset the core. The relevant voltage and current waveforms are shown in Fig. 7.33.

Mathematical Analysis

Let the switch is an ideal device (lossless with no voltage drop). The induced voltage at the secondary winding, $V_s = N_s V_i/N_p$, where N_s is number of turns on secondary winding and N_p is number of turns on primary winding. Neglecting the voltage drop across the conducting diode (D_1), the inductor voltage is given by

$$v_L = V_s - V_o = (N_s V_i/N_p) - V_o \qquad 0 < t < T_{on} \tag{7.63}$$

When the switch is off, the free-wheeling diode (D_2) conducts. Therefore,

$$V_L = -V_o, \quad T_{on} < t < T \tag{7.64}$$

In an inductor, the energy stored over a cycle is zero. Therefore, for a constant average current, the net voltage over a cycle is zero. Therefore,

$$\int v_L dt = 0 \tag{7.65}$$

or

$$\int_0^{T_{on}} v_L \, dt = \int_{T_{on}}^{T} v_L \, dt \tag{7.66}$$

or

$$\left(\frac{N_s}{N_p} V_i - V_o\right) T_{on} = -V_o (T - T_{on}) \tag{7.67}$$

The average output voltage of a forward converter is given by

$$V_o = \frac{N_s}{N_p} V_i D \tag{7.68}$$

The peak open-circuit voltage across the switch is given by

$$V_{oc(s)} = \left(1 + \frac{N_p}{N_f}\right) V_i \tag{7.69}$$

where N_f is number of turns on feedback winding.

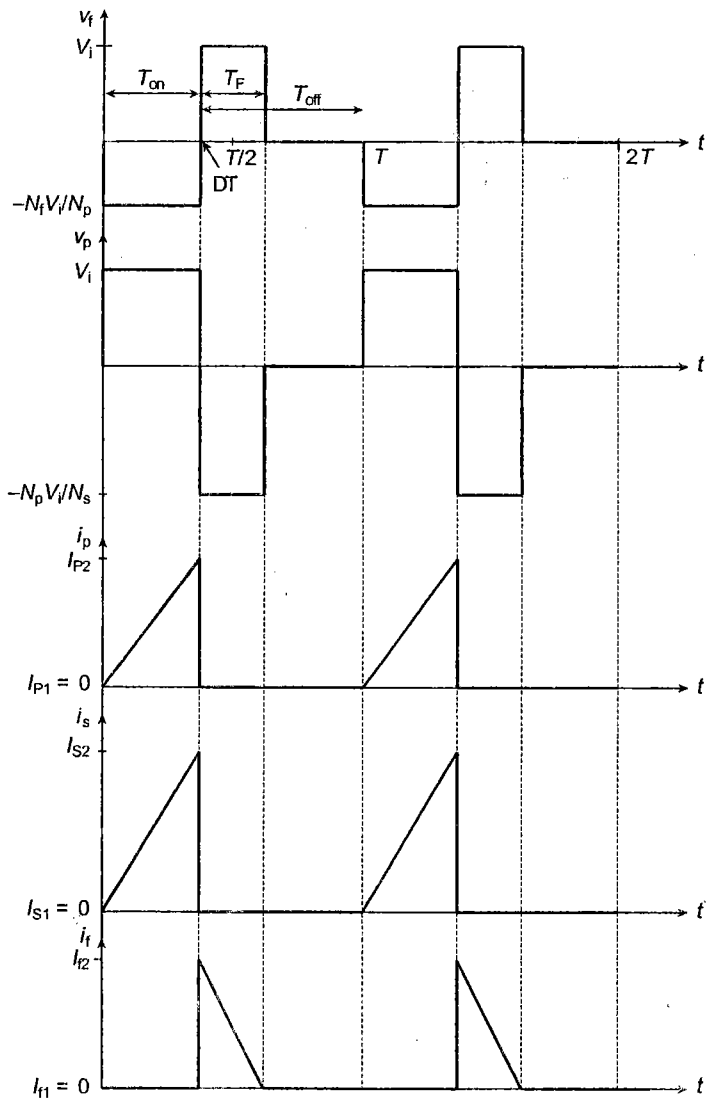


Figure 7.33 Waveforms of an isolated forward flyback converter ($N_s < N_p < N_f$).

To avoid saturation of the core, the transformer core flux should be fully reset at the end of each cycle. Therefore, the maximum duty ratio (D_{max}) corresponds to the condition when the energy stored during on-period should be equal to the energy released during off-period. It is the minimum off-period. The transformer should be designed with respect to the controllable output voltage range (maximum duty-cycle ratio). It is likely to occur for lowest supply voltage and highest load current.

Example 7.6 An isolated buck or forward converters has 150 turns in primary winding and 120 turns in the secondary winding. The dc input voltage is 160 V. Find the duration and the voltage across the primary and feedback windings during on and off periods. The converter operates at 25% duty ratio and 25 kHz. The number of turns of feedback winding, N_f = 180.

Solution The voltage of the primary winding during T_{on} period is V_i = 160 V. The reflected voltage in the primary winding (from the secondary winding) is given by

$$V_{p(ref)} = -\frac{N_p}{N_s} V_i = -\frac{150}{120} 160 = -200 \text{ V}$$

The conduction period (T_f) of the feedback diode (D_F) can be found from the equal volt-second criteria of the primary and feedback windings. Therefore,

$$160T_{on} = 200T_F \quad \text{or} \quad T_F = \frac{160}{200} T_{on}$$

Also, the period, T_{on} is given by

$$T_{on} = DT = \frac{D}{f} = \frac{0.25}{25 \times 10^3} = 10 \text{ μs}$$

It gives, T_F = 8 μs.

During T_{on} period, V_p = 160 V and during T_F period, $V_p = V_{p(ref)}$ = –200 V. The voltage in the feedback winding during T_{on} period is given by

$$V_F = -\frac{N_f}{N_p} V_i = -\frac{180}{150} 160 = -192 \text{ V}$$

During T_F period, v_F is clamped to V_i = 160 V.

7.8.3 Push–Pull Converters

The circuit configuration of a push–pull converter is shown in Fig. 7.34. When the switch (S_1) is on, the supply voltage (V_i) appears across the half of the primary winding and a current flows in the indicated direction. The core sets for flux of one direction. The energy is transferred to the load through D_1. When the switch S_2 is turned on and S_1 is turned off, the direction of current becomes reverse, causing the flux to flow in opposite direction. It resets the core. The energy transfers to the load through the diode D_2. The open-circuit voltage across the switch is $2V_i$, as $+V_i$ appears across half of the primary winding (auto transformer action). The push–pull converter has high efficiency but the voltage stress on switch is twice the supply voltage.

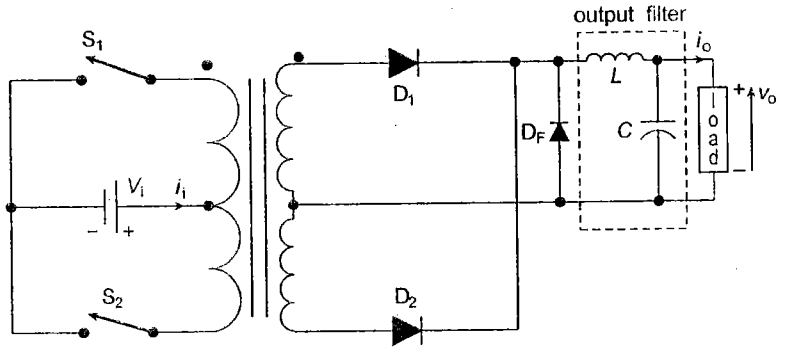


Figure 7.34 A circuit configuration of push–pull converter.

7.8.4 Full-bridge Converters

The circuit topology of a full-bridge converter is shown in Fig. 7.35. In this converter, S_1 and S_2 are turned on simultaneously in the half-cycle and S_3 and S_4 in the next half cycle. When S_1 and S_2

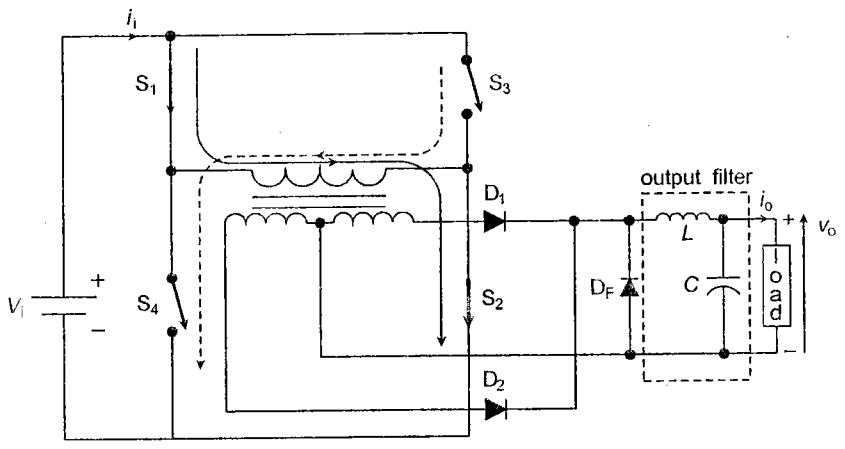


Figure 7.35 A circuit configuration of full-bridge dc-dc converter.

are on, the current, flows in one direction. The direction of current reverses when both S_3 and S_4 are switched on. Thus the flux in the core traverses the full hysterisis loop. Therefore, complete setting and resetting of the core take place. The open circuit voltage across each switch is V_i. The average output voltage, $V_o = (N_s/N_p)V_i$. The peak value of current through the switch is equal to I_i. The average current through the switch is $DI_i/2$ where $D = T_{on}/(T/2)$. This circuit configuration offers high efficiency and is commonly used in high-power applications (above 1 kW).

Example 7.7 A separately excited dc motor has the following name plate data: 220 V, 100 A, 2200 rpm. The armature resistance is 0.1 Ω and inductance is 5 mH. The motor is fed by a thyristor based chopper which is operating from a dc supply of 250 V. Due to restrictions in the

commutation circuit of SCR, the chopper can be operated over a duty-cycle range from 20% to 80%. Determine the range of speed over which the motor can be operated at the rated torque or load condition.

Solution The voltage equation of the armature circuit of motor is given by

$$E_b = V_o - I_a R_a$$

where V_o is the average output voltage of the chopper (or the armature voltage), E_b is the back emf and I_a and R_a are armature current and resistance respectively.

$$E_b = 220 - 100 \times 0.1 = 210 \text{ V}$$

Also, $E_b = k_b N$, where N is the speed of the motor in rpm. Then

$$K_b = \frac{E_b}{N} = \frac{210}{2200} = 0.095 \text{ V/rpm}$$

Input voltage to the chopper, $V_i = 250$ V. Voltage applied to the armature circuit of the motor for minimum and maximum duty ratio is given by

$$V_{o(min)} = D_{min} V_i = 0.2 \times 250 = 50 \text{ V}$$

$$V_{o(max)} = D_{max} V_i = 0.8 \times 250 = 200 \text{ V}$$

Since the torque is constant, the average armature current is same, i.e. 100 A. The minimum and maximum speed can be found using voltage equations.

$$E_{b(min)} = V_{o(min)} - I_a R_a = 50 - 100 \times 0.1 = 40 \text{ V}$$

Also,

$$E_{b(min)} = K_b N_{min} = 40 \quad \text{or} \quad N_{min} = \frac{40}{0.095} = 421 \text{ rpm}$$

$$E_{b(max)} = V_{o(max)} - I_a R_a = 200 - 100 \times 0.1 = 190 \text{ V}$$

Also,

$$E_{b(max)} = K_b N_{max} = 190 \quad \text{or} \quad N_{max} = \frac{190}{0.095} = 2000 \text{ rpm}$$

SUMMARY

A dc chopper or dc-to-dc converter is a switch-mode converter, used to obtain an adjustable output dc voltage from a fixed, variable or unregulated dc power supply. It acts as a dc transformer (similar to an autotransformer). The output voltage level can be raised or reduced with respect to the input dc voltage level. The semiconductor devices switch at a fast rate to control the output voltage or current. Thus size of L and C as well as ripples in load current reduce. These high-frequency converters most often act as an interface between dc-to-dc, dc-to-ac or ac-to-ac systems of different voltage level. Both thyristors and gate commutation devices are used. Except for very high power/high voltage applications, the thyristor based choppers became obsolete.

Either voltage, current or load commutation circuit is a must and that is needed for thyristor based choppers. The reverse voltage-impulse commutation circuit is faster than the current-pulse commutation circuit (as the turn-off is limited to one diode voltage drop by the anti parallel return diode in the later case). Although, thyristor is a robust device but due to the need of commutation circuit and large turn-off time (t_q), fast switching gate-commutation devices (e.g. MOSFET, IGBT, SIT, etc.) are preferred. Normally, frequency of thyristor based choppers is limited to 10 kHz while the frequency of gate commutation device (e.g. MOSFET, SIT) can go up to several MHz. In general, these converters are not designed to be operated in discontinuous conduction mode. The reason is that the interruption of highly inductive current causes high voltage stress on the devices. The output dc voltage is controlled either by controlling the duty ratio or by changing the switching frequency. An adjustable frequency converter generates harmonics of variable frequencies and therefore filter design becomes difficult.

When one switch is used, converters operate in the first quadrant of the output characteristics and power transfers only in one direction. When two or more switches are used, the power transfer is reversible. Such converter finds its application in dc drives to control speed and torque in all the four quadrants. Moreover, it is also used as an asynchronous dc link between two ac systems or power transmission systems of different frequency and/or voltage.

REVIEW QUESTIONS AND PROBLEMS

1. What are merits of dc-dc converters?
2. A thyristor based chopper operates at 10 kHz in TRC mode. The turn-off time (t_q) of the inverter-grade SCR is 12 μs. Find the maximum possible duty ratio of the chopper.
3. Why is CLC technique used?
4. What is the application of class-C chopper in dc motors?
5. What are demerits of thyristor based choppers?
6. What are merits and demerits of buck-boost converters?
7. Why is a Cuk converter better than buck-boost converter?
8. Why does the output voltage of a boost converter not reach to extremely high voltage level, explain?
9. For a buck or step-down converter, when does the load current become discontinuous?
10. What are the advantages of isolated dc-to-dc converters?
11. What are the demerits of a linear power supply?
12. An ideal dc chopper operating at a frequency of 500 Hz feeds an *RL* load (R = 30 Ω and L = 9 mH) from a 48-V battery. The load is shunted by a free-wheeling diode. The battery is assumed to be lossless and the duty ratio of chopper is 50%. Compute: (i) peak load current, (ii) minimum load current, (iii) average load current and (iv) average load voltage.

13. A separately excited dc motor is fed from a chopper operating at 500 Hz with a duty cycle of 50% and is drawing an average current of 10 A from a 200-V dc source. A free-wheeling diode is connected across it. The motor has a negligible armature resistance, an armature inductance of 50 mH and a torque constant of 0.5 N-m/A. Determine the minimum and maximum motor armature current, motor back emf and mechanical torque developed.

14. Consider a chopper circuit of Fig. 7.8 with $C = 2$ μF. The chopper operates at 400 Hz and 50% duty cycle. The load current remains almost ripple free at 10 A. Assuming the input voltage to be 200 V and devices to be ideal. What is the turn-off time available to the main thyristor (T_m)? (*Hint:* For a impulse-commutated chopper, the time available to turn-off, $t_c = V_s C/I_0$).

15. A dc chopper circuit connected to dc supply of 80 V supplies an inductive load 40 mH in series with a resistance of 4 Ω. A free-wheeling diode is connected across the load. The current is required to be maintained between the limits 10 A and 12 A. Calculate the time ratio of the chopper.

16. A step-up chopper with a pulse width of 140 μs is operating on 230-V dc supply. Compute the load voltage if the blocking period of the device is 50 μs.

17. A load commutated chopper fed from a 230-V dc source has a constant load current of 50 A. For a blocking period of 0.3 ms and a chopping frequency of 2 kHz, calculate: (a) the value of commutating capacitance, (b) average output voltage, (c) circuit turn-off time and (d) total commutation interval.

18. A dc motor with armature resistance of 0.4 Ω and armature inductance of 10 mH is having a back emf of 100 V while carrying a current of 10 A. The motor is connected to a dc source of 200 V by the main SCR of the chopper. If the SCR turns off after 1 ms, compute the current in the motor (i) at the instant the thyristor turns off and (ii) 10 ms after SCR turns off. (*Hint:* (i) Take initial current = 10 A and $T_{on} = 1$ ms).

8

Inverters*

8.1

INTRODUCTION

The process of conversion of a dc power into an ac power at a desired output voltage and frequency is called inversion. This can be done by a fully-controlled converter (using thyristors), connected to the ac mains. This is called a *line-commutated* inverter and operates at the line frequency only. When a thyristor based inverter supplies an ac power to an isolated load, forced commutation techniques are required. This makes the inverter bulkier and costlier. Therefore, thyristor based inverters are used only in high-power applications. For low- and medium-power inverters, gate-controlled turn-off devices (gate-commutation devices), such as power BJT, MOSFET, IGBT, GTO, SIT, etc., are used. In addition to being fully controlled, these have high-switching frequencies. Therefore, these devices may be very efficiently employed in inverters, where the output voltage is to be controlled using the pulse width-modulation (PWM) technique.

Inverters are used in various applications requiring variable voltage, variable frequency ac supply. Some important applications are:

- Variable speed ac motor drives
- Induction heating
- Standby power supply
- High voltage dc transmission systems.

8.2

CLASSIFICATION OF INVERTERS

There are different basis of classification of inverters. Inverters are broadly classified as current-source inverter and voltage-source inverter. Moreover, it can be classified on the basis of devices used (SCR or gate-commutation devices), circuit configuration (half-bridge or full-bridge), nature

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of output voltage (square, quasi-square or sine-wave) and type of circuit (Switch-mode PWM or resonant converters), etc.

8.2.1 Current-source Inverters (CSI)

This type of inverter is fed by a 'current source' with a high-internal impedance (using current limiting chokes or inductor in series with a dc source). Therefore, supply current does not change quickly. The load current is varied by controlling the input dc voltage to the current-source inverter. CSI are used in a very high-power ac drives.

8.2.2 Voltage-source Inverters (VSI)

This type of inverter is fed by a dc source of small internal impedance. Looking from the ac side, the terminal voltage remains almost constant irrespective of the load current drawn. Depending on the circuit configurations, the voltage source inverter may be classified as half-bridge and full-bridge inverters. Voltage-source inverters may further be classified as square-wave inverter and pulse-width modulated inverter.

Square-wave inverters A square-wave inverter produces a square-wave ac voltage of a constant magnitude. The output voltage of this type of inverter can only be varied by controlling the input dc voltage.

Pulse-width modulated (PWM) inverters In a PWM inverter, the output has one or more pulses in each half-cycle. Varying the width of these pulses, the output voltage may be controlled. The magnitude of input dc voltage is essentially constant in this inverter. There are many techniques of the pulse-width modulation that will be discussed in a separate section.

8.3 CLASSIFICATION OF THYRISTOR-BASED INVERTERS

Thyristor-based inverters are broadly classified as line-commutated inverters and forced commutated inverters.

Line-commutated Inverters

A fully controlled 1-phase or 3-phase converter connected to a battery or a dc source, acts as an inverter. The firing angle (α) is greater than $\pi/2$. It is a voltage-source inverter, where commutation is done by an application of negative line voltage across the conducting thyristors.

Forced-commutated Inverters

This type of inverter requires additional circuitry for commutation of thyristors. Depending on the commutation technique used, these inverters are classified as:

Series inverters In series inverters, commutating elements (inductor and capacitor) are permanently connected in series with the load impedance. Therefore performance of inverter depends on these elements.

Parallel inverters Here commutating elements are separate, which are connected in parallel with the conducting thyristor.

Auxiliary commutated inverters In this case, an auxiliary thyristor is used to commutate a conducting thyristor (e.g. McMurray or modified McMurray inverters).

Complementary commutated inverters In this case, tightly coupled inductors are used to turn-off the other SCR of a pair (e.g. McMurray Bedford inverters).

8.4

SINGLE-PHASE, HALF-BRIDGE, VOLTAGE-SOURCE INVERTERS

The basic topology of a single-phase, half-bridge inverter fed by a dc voltage source is shown in Fig. 8.1. S_1 and S_2 are gate-commutated power semiconductor devices (switches). When closed, these switches conduct and current flows in the direction of arrow. The operation of this inverter for different type of loads is explained in the following sections.

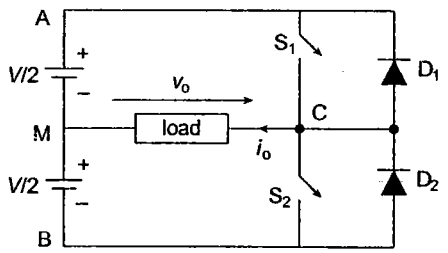
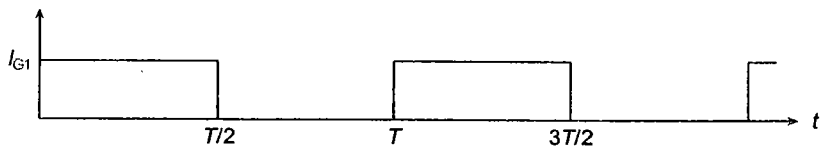


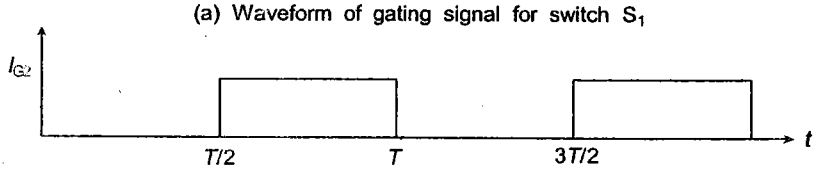
Figure 8.1 Circuit configuration of a single-phase, half-bridge inverter.

8.4.1 Resistive Loads

Figure 8.2 shows the gating signals I_{G1} and I_{G2} of switches S_1 and S_2, respectively. The switch S_1 is closed for half time period ($T/2$) of the desired ac output. It connects point A of the dc source to point C and the output voltage v_o becomes equal to $+V/2$. At $t = T/2$, gating signal is removed

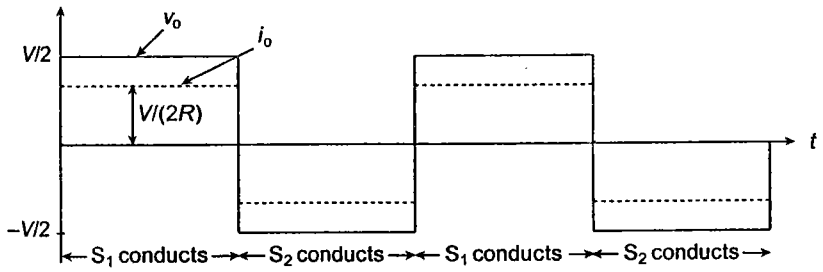


(a) Waveform of gating signal for switch S_1



(b) Waveform of gating signal for switch S_2

Figure 8.2 (*Cont.*)



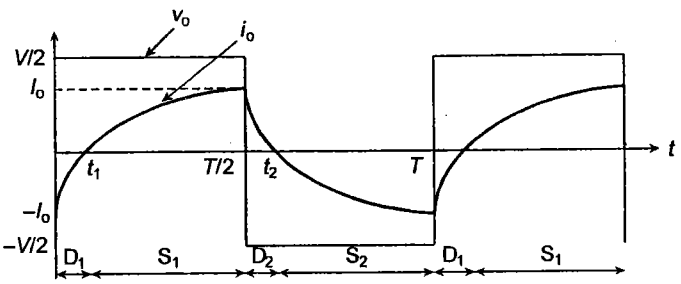
(c) Voltage and current waveforms for resistive load

Figure 8.2 Gating signals I_{G1} and I_{G2} of switches S_1 and S_2.

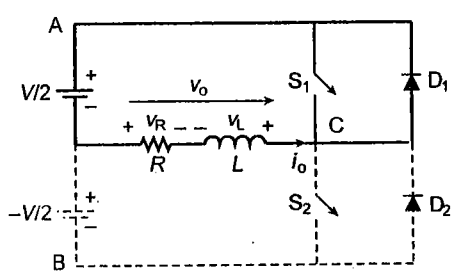
from S_1 and it turns off. For the next half time period ($T/2 < t < T$), the gating signal is given to S_2. It connects point B of the dc source to point C and the output voltage reverses. Thus, by closing S_1 and S_2 alternately, for half time periods, a square-wave ac voltage is obtained at the output. For a resistive load, the load current $i_o = v_o/R$. Hence the wave shape of output current is identical to that of the output voltage, as shown in Fig. 8.2c. In this case, diodes D_1 and D_2 do not play any role. The frequency of the output voltage, $f_o = 1/T$. Simply by controlling the time periods of the gate-drive signals, the frequency can be varied.

8.4.2 *RL* Loads

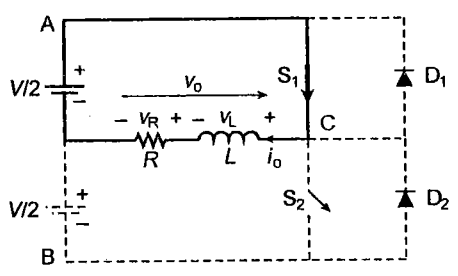
The operation of a single-phase, half-bridge inverter for an *RL* load is divided into four distinct modes. Voltage and current waveforms are shown in Fig. 8.3a.



(a) Voltage and current waveforms for *RL* load

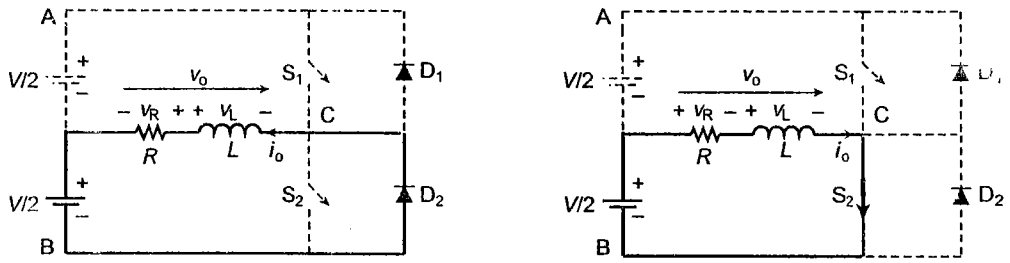


(b) Switching diagram of mode I



(c) Switching diagram of mode II

Figure 8.3 (*Cont.*)



(d) Switching diagram of mode III (e) Switching diagram of mode IV

Figure 8.3 Voltage and current waveforms of an *RL* load.

Mode I: $(0 \le t \le t_1)$ At $t = 0$, the gating signal is removed from S_2 and it turns off. At this instant, the load current (i_o), is at its negative peak value (from the previous cycle). The current cannot reverse instantaneously because of the inductive load. A path for the negative current is provided by the feedback diode, D_1, which is forward biased due to reversal of the voltage (v_L) across inductance (v_L becomes positive and it is more than $V/2$ at $t = 0$). The voltage across D_1 keeps S_1 in reverse biased condition and it remains in off state even though the gating signal has been applied to it at $t = 0$. During this interval $(0 < t < t_1)$, load voltage is positive and load current is negative. Thus, the energy stored in the inductance (in the previous cycle), is fed back to the upper dc source through D_1 and the load current decays. The switching diagram for this mode is shown in Fig. 8.3b, where the current path is shown by thick lines.

Mode II: $(t_1 \le t \le T/2)$ At $t = t_1$, diode D_1 is commutated and switch S_1 is turned on. The current through the load builds up in positive direction and becomes maximum at $t = T/2$. The gating signal of S_1 is withdrawn at this instant. During this interval, v_o and i_o are positive and energy is stored in the inductance. The switching diagram for this mode is shown in Fig. 8.3c.

Mode III: $(T/2 \le t \le t_2)$ At $t = T/2$, S_1 is turned off. At this instant, the current is positive maximum and it cannot reverse instantaneously because of the inductive load (a negative voltage, $v_L = di/dt$ at cathode of D_2). The feedback diode, D_2 is forced to turn on and to carry the positive load current. The load current decays and becomes zero at $t = t_2$. During this interval $(T/2 \le t \le t_2)$, the load voltage is negative and the load current is positive. Energy is released by the inductor and is fed back to the lower dc source. The switching diagram for this mode is shown in Fig. 8.3d.

Mode IV: $(t_2 \le t \le T)$ At $t = t_2$, D_2 is commutated and S_2 is turned on. The load current builds up in reverse direction and becomes negative maximum at $t = T$. The switching diagram for this mode is shown in Fig. 8.3e.

The voltage equation is given by

$$\frac{V}{2} = Ri_o(t) + L\frac{di_o(t)}{dt}, \qquad \text{for } 0 < t < \frac{T}{2} \tag{8.1}$$

The solution to the above first order differential equation, with initial load current, $-I_o$, can be obtained as:

$$i_o(t) = \frac{V}{2R}(1 - e^{-Rt/L}) - I_o e^{-Rt/L} \tag{8.2}$$

The expression of I_o may be obtained from equation (8.2),

$$i_o\left(\frac{T}{2}\right) = I_o = \frac{V}{2R}\frac{1 - e^{-RT/(2L)}}{1 + e^{-RT/(2L)}} \tag{8.3}$$

Substituting this value of I_o in equation (8.2),

$$i_o(t) = \frac{V}{2R}(1 - e^{-Rt/L}) - \frac{V}{2R}\frac{1 - e^{-RT/(2L)}}{1 + e^{-RT/(2L)}}\, e^{-Rt/L} \tag{8.4}$$

or

$$i_o(t) = \frac{V}{2R}\left[1 - \frac{2}{1 + e^{-RT/(2L)}}\, e^{-Rt/L}\right] \tag{8.5}$$

Again, the voltage equation is given by

$$-\frac{V}{2} = Ri_o(t') + L\frac{di_o(t')}{dt'}, \qquad \text{for } \frac{T}{2} < t < T \tag{8.6}$$

where, $t' = t - (T/2)$. The solution of the first-order differential equation (8.6) with initial load current is given by

$$i_o\left(\frac{T}{2}\right) = I_o = -\frac{V}{2R}\left\{1 - \frac{2}{1 + e^{-RT/(2L)}} \exp\left[-\frac{R}{L}\left(t - \frac{T}{2}\right)\right]\right\}, \qquad \text{for } \frac{T}{2} < t < T \tag{8.7}$$

8.4.3 *RC* Loads

For an *RC* load, the switch S_1 conducts during the interval $0 < t < T/2$ and a positive current flows through the load. The capacitor is charged and its voltage builds up from the negative peak ($-V_o$), to the positive peak ($+V_o$). The charging current decays exponentially, as shown in Fig. 8.4. In the interval $T/2 < t < T$, the switch S_2 conducts and a negative load current flows through the load which charges the capacitor in the reverse direction. The negative load current decays, as the capacitor voltage varies from $+V_o$ to $-V_o$.

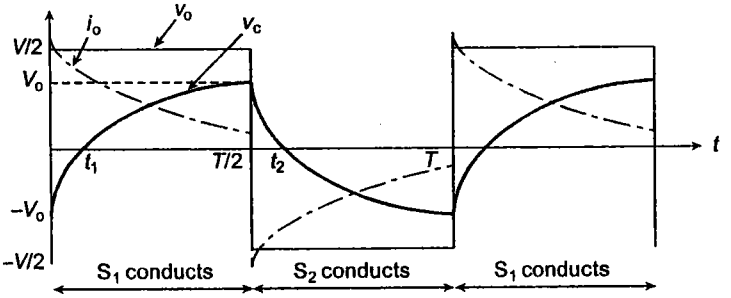


Figure 8.4 Voltage and current waveforms for an *RC* load.

The voltage equation for an RC load, is given by

$$\frac{V}{2} = Ri_o(t) + v_c(t), \qquad \text{for } 0 < t < \frac{T}{2} \tag{8.8}$$

where v_c is voltage across the capacitance. Replacing the load current (i_o), in terms of capacitor voltage (v_c), the above equation may be written as

$$\frac{V}{2} = RC\frac{dv_c(t)}{dt} + v_c(t) \tag{8.9}$$

The solution of above differential equation, with initial condition as $v_c(0) = -V_o$ yields,

$$v_c(t) = \frac{V}{2}[1 - e^{-t/(RC)}] - V_o e^{-t/(RC)} \tag{8.10}$$

Applying the condition $v_c(T/2) = V_o$ in (8.10), V_o is given by

$$V_o = \frac{V}{2}\frac{1 - e^{-T/(2RC)}}{1 + e^{-T/(2RC)}} \tag{8.11}$$

Using (8.11), (8.10) may be written as

$$v_c(t) = \frac{V}{2}\left[1 - e^{-t/(RC)}\right] - \frac{V}{2}\frac{1 - e^{-T/(2RC)}}{1 + e^{-T/(2RC)}} e^{-t/(RC)}$$

or

$$v_c(t) = \frac{V}{2}\left[1 - \frac{2}{1 + e^{-T/(2RC)}} e^{-t/(RC)}\right] \tag{8.12}$$

The load current is given by

$$i_o(t) = C\frac{dv_c(t)}{dt} = \frac{V}{R}\frac{e^{-t/(RC)}}{1 + e^{-T/(2RC)}} \tag{8.13}$$

Equations (8.12) and (8.13) give $v_c(t)$ and $i_o(t)$ for the first half-cycle. Similarly, for the second half-cycle ($T/2 < t < T$), for the sake of simplicity of analysis, the time reference is shifted by $T/2$. Therefore,

$$v_c(t') = -\frac{V}{2}\left[1 - \frac{2}{1 + e^{-T/(2RC)}} e^{-t'/(RC)}\right] \tag{8.14}$$

and

$$i_o(t') = -\frac{V}{R}\frac{e^{-t'/(RC)}}{1 + e^{-T/(2RC)}} \tag{8.15}$$

where $t' = t - (T/2)$.

8.5

SINGLE-PHASE, FULL-BRIDGE INVERTERS

The single-phase, half-bridge inverters, discussed in Section 8.5, require only two controlled switches and two diodes. However, this inverter can be used only when three-wired dc supply is

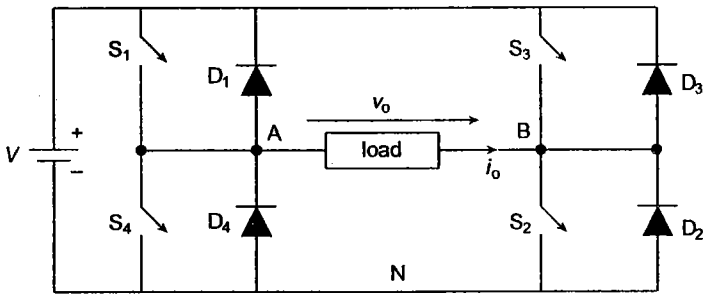
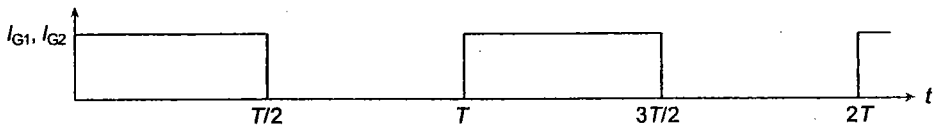
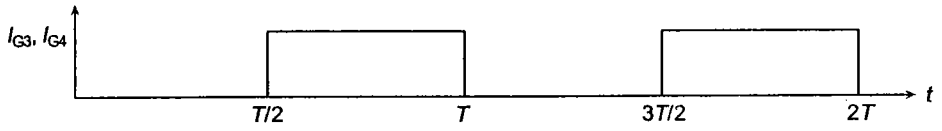


Figure 8.5 Circuit configuration of a single-phase, full-bridge inverter.

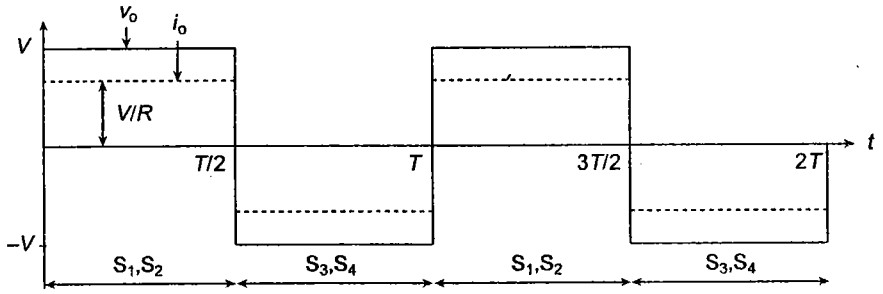
available. Moreover, the voltage across the off-state power semiconductor device is V, which is double the load voltage. These drawbacks are removed in full-bridge inverters (Fig. 8.5). The inverter uses two pairs of controlled switches (S_1S_2 and S_3S_4) and two pairs of diodes (D_1D_2 and D_3D_4). The devices of one pair operate simultaneously. The gating signals of the switch-pairs S_1S_2 and S_3S_4 are shown in Figs. 8.6a and b, respectively.



(a) Gating signal for switch S_1, S_2

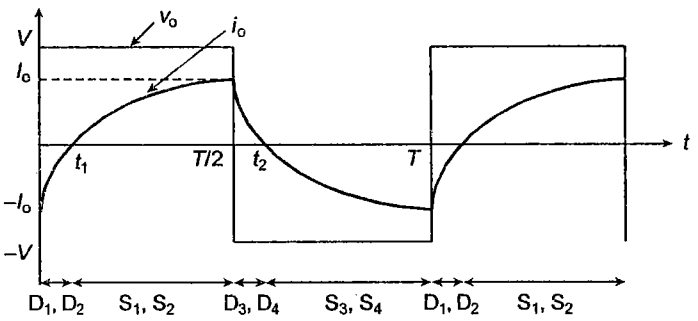


(b) Gating signal for switch S_3, S_4



(c) Voltage and current waveforms for resistive loads

Figure 8.6 (*Cont.*)



(d) Voltage and current waveforms for *RL* loads

Figure 8.6 Gating signals and waveforms of a full-bridge voltage-source inverter.

For a resistive load, the switch pair S_1S_2 closes for the time interval $0 < t < T/2$ and the output voltage (v_o), becomes $+V$. At $t = T/2$, S_1S_2 pair turns off and simultaneously, S_3S_4 pair turns on to make $v_o = -V$. At $t = T$, S_1S_2 pair is again closed to make $v_o = V$ and the cycle repeats. By operating the two switch pairs at the desired frequency, a square-wave ac voltage is obtained at the output. The load current waveform is also a square wave with magnitude V/R, as shown in the Fig. 8.6c.

For an *RL* load, waveforms of load voltage and load current are shown in Fig. 8.6d. At $t = 0$, the load current is at its negative peak and its direction cannot reverses instantaneously, due to inductive nature of the load. The diode pair D_1D_2 provides a path for the negative current. The output voltage becomes positive ($+V$) and the negative load current decays to zero at $t = t_1$. During this period, energy is fed back to the source through the feedback diodes D_1 and D_2. At $t = t_1$, the diode pair D_1D_2 commutates and the switch pair S_1S_2, which is already recieved the gating signal, turns on. It provides the path for the positive load current. The load current builds up and reaches its positive peak at $t = T/2$. At this instant, the switch pair S_1S_2 turns off. The positive current continues to flow for some more time (up to $t = t_2$) through the diode pair D_3D_4. As the load voltage is negative, the energy is fed back to the source. At $t = t_2$, D_3D_4 pair commutates and S_3S_4 pair starts conduction for the negative load current.

The expressions of the load current, for different types of loads may be obtained by replacing the term $V/2$ with V in the corresponding equations for the half-bridge inverter.

8.6 PERFORMANCE PARAMETERS OF INVERTERS

Ideally, an inverter should give a sinusoidal voltage at its output. However, outputs of practical inverters are non-sinusoidal and may be resolved into fundamental and harmonic components. Performance of an inverter is usually assessed with the following performance parameters.

1. *Harmonic factor of nth harmonic:* A *harmonic factor* is a measure of the individual harmonic contribution in the output voltage of an inverter. It is defined as:

$$\mathrm{HF}_n = \frac{V_n}{V_1} \tag{8.16}$$

where V_n is the rms values of the nth harmonic component and V_1 is the rms value of the fundamental component of the output voltage.

2. *Total harmonic distortion (THD)*: A *total harmonic distortion* is a measure of closeness in a shape between the output voltage waveform and its fundamental component. It is defined as the ratio of the rms value of the total harmonic component of the output voltage and the rms value of the fundamental component. Mathematically,

$$\text{THD} = \frac{\sqrt{\sum_{n=2,3,\ldots}^{\infty} V_n^2}}{V_1} = \frac{\sqrt{V_{\text{rms}}^2 - V_1^2}}{V_1} \tag{8.17}$$

where V_{rms} is the rms value of the output voltage.

3. *Distortion factor (DF):* A *distortion factor* indicates the amount of harmonics that remain in the output voltage waveform, after the waveform has been subjected to second-order attenuation (i.e. divided by n^2). It is defined as

$$\text{DF} = \frac{\sqrt{\sum_{n=2,3,\ldots}^{\infty} (V_n/n^2)^2}}{V_1}$$

4. *Lowest-order harmonics* (LOH): The lowest frequency harmonic, with a magnitude greater than or equal to three per cent of the magnitude of the fundamental component of the output voltage, is called the *lowest-order harmonic*. Higher the frequency of the LOH, lower will be the distortion in the current waveform.

8.7 PERFORMANCE OF SQUARE-WAVE INVERTERS

The output voltage waveform of a square-wave inverter is shown Fig. 8.7. V_L, the magnitude of the square wave, is $V/2$ for a half-bridge inverter and V for a full-bridge inverter.

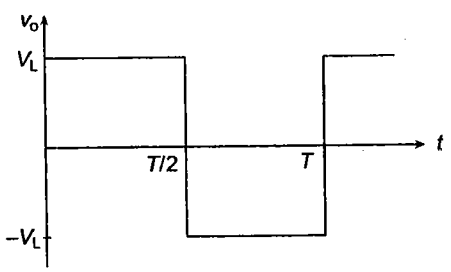


Figure 8.7 Voltage waveform of a square-wave inverter.

The voltage v_o may be expressed in Fourier series as

$$v_o(t) = \sum_{n=1}^{\infty} a_n \cos(n\omega t) + \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{8.18}$$

where

$$a_n = \frac{1}{\pi} \int_0^{2\pi} v_o(t) \cos(n\omega t)\, d(\omega t) \tag{8.19}$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} v_o(t) \sin(n\omega t)\, d(\omega t) \tag{8.20}$$

As the voltage waveform possesses half-wave symmetries, only odd 'b' components shall be present in the fourier series, which is given by

$$b_n = \frac{2}{\pi} \int_0^{\pi} v_o(t) \sin(n\omega t)\, d(\omega t)$$

$$= \frac{2}{\pi} \int_0^{\pi} V_L \sin(n\omega t)\, d(\omega t)$$

$$= \frac{4V_L}{n\pi}, \qquad \text{for } n = 1, 3, 5, \ldots$$

Putting the values of the constants a_n and b_n, from (8.18)

$$v_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_L}{n\pi} \sin(n\omega t) \tag{8.21}$$

The rms value of the nth component

$$V_n = \frac{4V_L}{n\pi\sqrt{2}} = \frac{0.9V_L}{n}, \qquad \text{for } n = 1, 3, 5, \ldots \tag{8.22}$$

for $n = 1$, the rms value of the fundamental component is given by

$$V_1 = 0.9V_L \tag{8.23}$$

Using (8.16), (8.22) and (8.23), the nth harmonic factor may be obtained as

$$HF_n = \frac{1}{n}, \qquad \text{for } n = 3, 5, 7, \ldots \tag{8.24}$$

Putting different values of n,

$$HF_3 = 0.333,\ HF_5 = 0.20,\ HF_7 = 0.143,\ HF_9 = 0.111,\ HF_{11} = 0.091,\ \ldots$$

The complete harmonic spectrum is shown in Fig. 8.8. The third harmonic component is the

lowest-order harmonic (LOH) as its magnitude is 33.33% of the fundamental (more than 3%). The rms value of the output voltage may be obtained as

$$V_{rms} = V_L \tag{8.25}$$

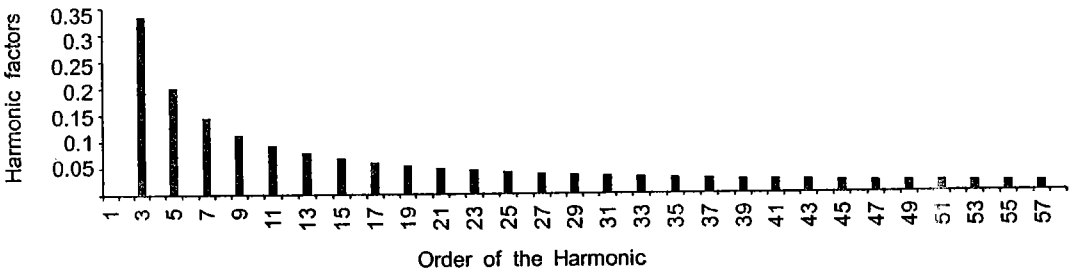


Figure 8.8 Voltage harmonic spectrum of a square-wave inverter.

From (8.17), (8.23) and (8.25), we get

$$\text{THD} = \frac{\sqrt{V_L^2 - (0.9V_L)^2}}{0.9V_L} = 0.4834 \text{ or } 48.34\%$$

If the square-wave inverter feeds an *RL* load, the load current is non-sinusoidal, as shown in Fig. 8.3a. The load current may be expressed in Fourier series as

$$i_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_L}{n\pi\sqrt{R^2 + (n\omega L)^2}} \sin(n\omega t - \varphi_n) \tag{8.26}$$

where φ_n is the phase angle of the nth harmonic component of the load current. It is given by

$$\varphi_n = \tan^{-1}\frac{n\omega L}{R}$$

8.8 PULSE-WIDTH MODULATED INVERTERS

The square-wave inverters, discussed in Sections 8.4–8.7, suffer from two major drawbacks:

1. For fixed-source voltage, the output voltage of the inverter cannot be controlled. To achieve voltage control, the inverter must be fed either from a controlled ac-dc or dc-dc converter.
2. The output voltage contains appreciable harmonics (low-frequency range), as shown in Fig. 8.8. THD is also very high (48.34%).

To achieve voltage control within the inverter and to reduce the harmonic contents in the output voltage, pulse-width modulated (PWM) inverters are used. In PWM inverters, widths of output pulses are modulated to achieve the voltage control. Among the large number of modulation techniques, simple modulation techniques are:

(a) Single pulse-width modulation (SPWM)
(b) Multiple or uniform pulse-width modulation (UPWM)
(c) Sinusoidal pulse-width modulation (sin-PWM).

8.8.1 Single Pulse-width Modulation

In this modulation technique, the output voltage of the inverter has only one pulse in each half cycle. The width of this pulse is controlled to vary the output voltage. To achieve SPWM control using a full-bridge inverter, as shown in Fig. 8.5, the required gating signals are shown in Fig. 8.9. The output voltage is $+V$ when S_1S_2 or D_1D_2 conducts. It is $-V$ when the S_3S_4 or D_3D_4 conduct. The voltage and current waveforms for an *RL* load, along with the conduction intervals of various devices are shown in Fig. 8.9. The operation may be divided into six different modes, as tabulated below:

Mode	*Load voltage*	*Load current*	*Conducting devices*	*Operation*
I	Zero	Negative	S_4,D_2	Freewheeling
II	Positive	Negative	D_1D_2	Regeneration
III	Positive	Positive	S_1S_2	Inversion
IV	Zero	Positive	S_1D_3	Freewheeling
V	Negative	Positive	D_3D_4	Regeneration
VI	Negative	Negative	S_3S_4	Inversion

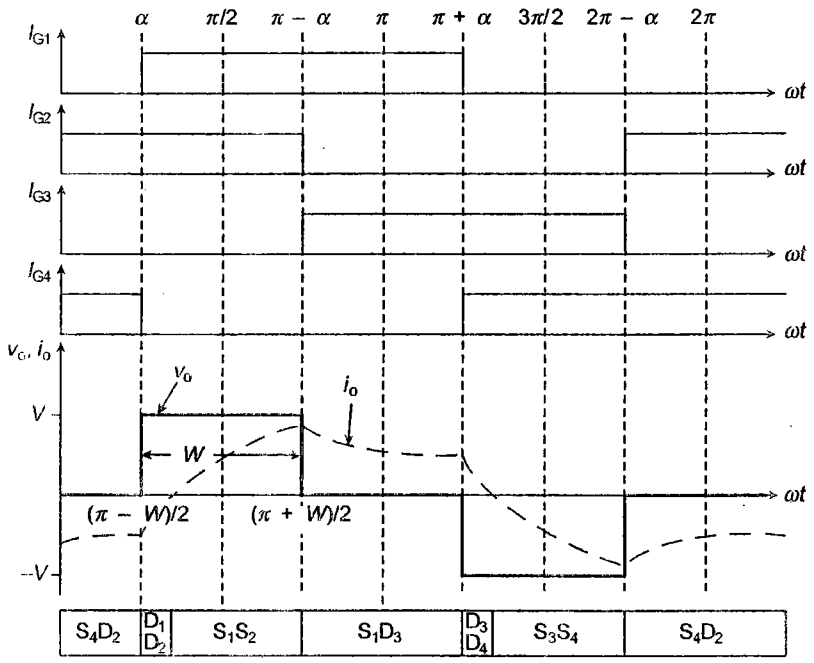


Figure 8.9 Gating signals, voltage and current waveforms of an SPWM inverter.

The width of output pulses (W) and the delay angle (α) of the gating signal I_{G1} may be related as $W = \pi - 2\alpha$. By controlling α from zero to $\pi/2$, the width of output pulses may vary from π to zero.

The rms value of the output voltage is given by

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_{(\pi-W)/2}^{(\pi+W)/2} V^2 d(\omega t)} = V\sqrt{\frac{W}{\pi}} \tag{8.27}$$

Thus the output voltage may be varied from 0 to V, by varying the pulse width from zero to π. The output voltage waveform possesses odd- and half-wave symmetries. Therefore, only odd b components shall be present in the Fourier-series expression, which are given by

$$b_n = \frac{2}{\pi}\int_{(\pi-W)/2}^{(\pi+W)/2} V \sin(n\omega t)\, d(\omega t), \qquad \text{for } n = 1, 3, 5, \ldots \tag{8.28}$$

$$= \frac{4V}{n\pi}\sin\frac{nW}{2}, \qquad \text{for } n = 1, 5, 9, \ldots \tag{8.29}$$

$$= -\frac{4V}{n\pi}\sin\frac{nW}{2}, \qquad \text{for } n = 3, 7, 11, \ldots \tag{8.30}$$

Using (8.29) and (8.30), the output voltage may be written as

$$v_o(t) = \frac{4V}{\pi}\left(\sin\frac{W}{2}\sin\omega t - \frac{1}{3}\sin\frac{3W}{2}\sin 3\omega t + \frac{1}{5}\sin\frac{5W}{2} + \cdots\right) \tag{8.31}$$

To eliminate the nth harmonic, $\sin(nW/2) = 0$ or $nW/2 = k\pi$. Therefore, $W = 2k\pi/n = 360k/n$ degrees, where k is an integer. For example, to eliminate the third harmonic, the required pulse width $W = 360/3 = 120°$. Similarly, to eliminate the fifth harmonic, $W = 360/5 = 72°$ or $W = 144°$.

The variations of different harmonic components, the fundamental component and the rms output voltage with the pulse width are shown in Fig. 8.10, as a ratio of the source voltage. The

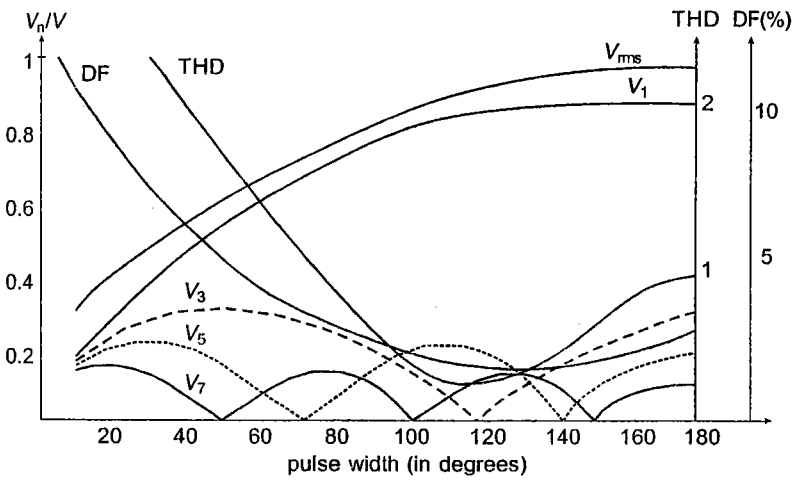


Figure 8.10 Harmonic profile of single PWM inverter.

variations in the total harmonic distortion (THD) and the distortion factor (DF) are also shown in the same figure. It may be observed that DF is minimum for the pulse width around 120°. For smaller pulse widths or lower values of rms voltages, the harmonic contents are comparable to the fundamental, resulting in very high values of THD and DF. Therefore, single PWM technique can only be used to control the output voltage within a narrow range.

8.8.2 Uniform Pulse-width Modulation

In a uniform PWM inverter, the output voltage has several pulses of equal width in each half-cycle. The gating signals may be obtained by comparing a square-wave reference signal with a high-frequency triangular carrier wave as shown in Fig. 8.11.

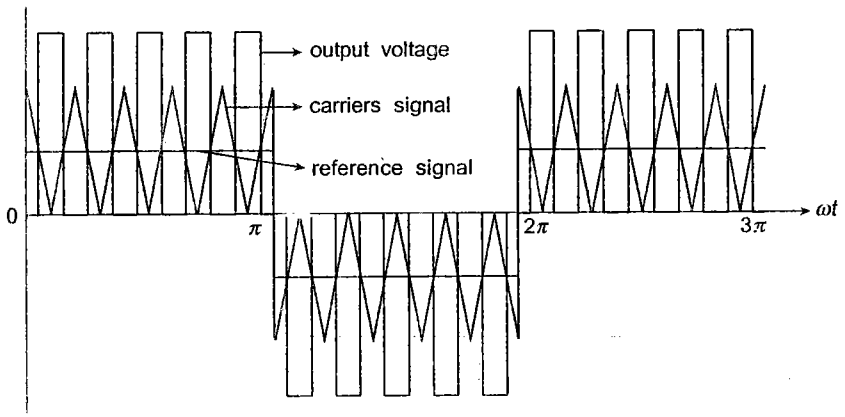


Figure 8.11 Generation of gating signals and output voltage waveforms of an UPWM inverter.

The number of output pulses in each half-cycle may be obtained as

$$N = \frac{f_c}{2f_{ref}} = \frac{m_f}{2} \tag{8.32}$$

where f_c and f_{ref} are the frequencies of carrier signal and reference signal, respectively, and m_f is the frequency modulation ratio.

The ratio of the amplitudes of the carrier signal (A_c) and the reference signal (A_{ref}) is called the *amplitude modulation ratio* or modulation index (m_a). Mathematically,

$$m_a = \frac{A_c}{A_{ref}} \tag{8.33}$$

The rms value of the output voltage may be obtained as

$$V_o = \left(\frac{V^2 W}{\pi/N}\right)^{1/2} = V\sqrt{\frac{WN}{\pi}} \tag{8.34}$$

where W is the width of each pulse. By varying the amplitude modulation ratio from 0 to 1, the width of output pulses can be varied from 0 to π/N and hence the output voltage may be varied from 0 to V.

The output voltage may be expressed in Fourier series by evaluating various harmonic components using a computer programme. The variations of different harmonic components, THD and DF with amplitude modulation ratio are shown in Fig. 8.12. It may be observed that for lower values of m_a, THD becomes very high. However, DF remains almost constant at around 3.5% in the whole range of m_a. This modulation technique can therefore be used for voltage variation over a wide range.

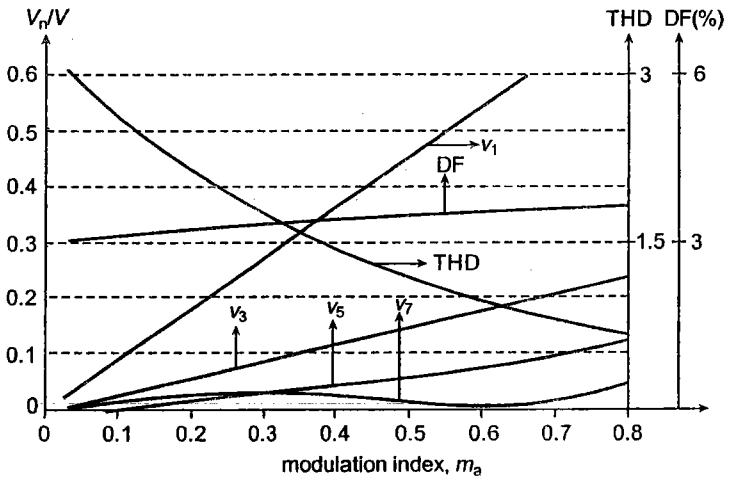


Figure 8.12 Harmonic profile of UPWM inverter.

8.8.3 Sinusoidal Pulse-width Modulation

In sinusoidal pulse-width modulation technique, the width of output pulses is not constant as compared to uniform PWM technique. Here the width of pulses varies in proportion to the magnitude of a sine wave. This is achieved by comparing a sinusoidal reference signal, v_{ref}, of a desired frequency with a high-frequency triangular carrier wave (v_c). Two types of switching schemes, bipolar switching scheme and unipolar switching scheme, are normally used.

Bipolar Switching Schemes

In bipolar switching scheme, the switches of the full bridge inverter of Fig. 8.5 are operated using the following logic:

1. $v_{ref} > v_c$, S_1 and S_2 are on and $v_o = V$.
2. $v_{ref} < v_c$, S_3 and S_4 are on and $v_o = -V$.

The output voltage oscillates between $+V$ and $-V$. The width of output pulses and hence the effective output voltage may be controlled by controlling the magnitude of the reference signal. The frequency of output voltage is governed by the frequency of reference signal. The reference signal, carrier signal, and the output voltage along with the fundamental component are shown in Fig. 8.13 for $m_a = 0.5$ and $m_f = 7$.

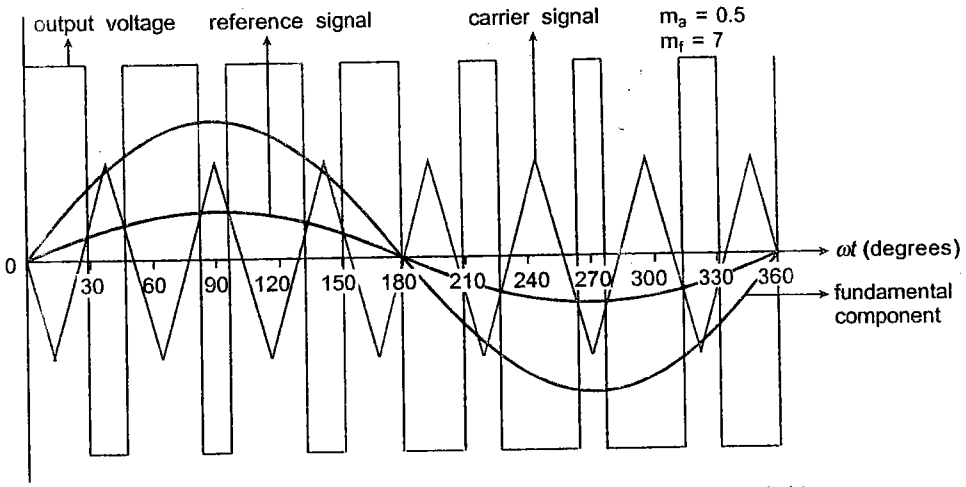


Figure 8.13 sin-PWM inverter waveforms with bipolar voltage switching.

The harmonic spectrum of the output voltage waveform for $m_a = 0.8$ and $m_f = 15$ is shown in Fig. 8.14, wherein, the peak values of the various harmonic components are shown as a ratio of

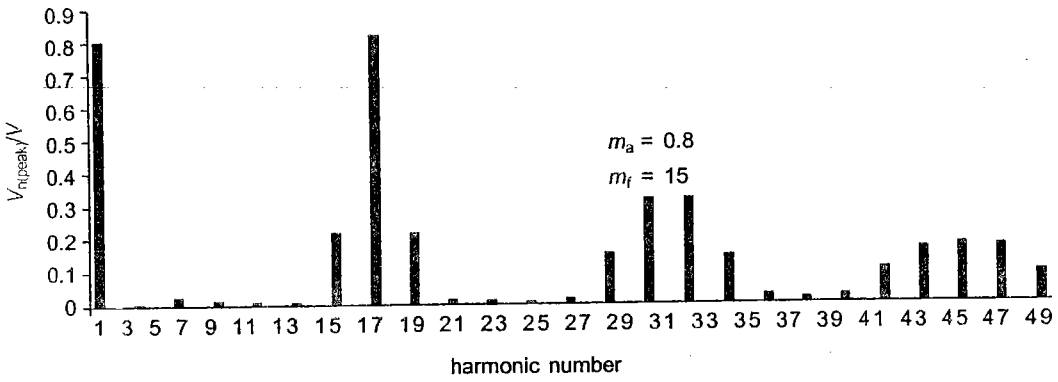


Figure 8.14 Harmonic spectrum of sin-PWM inverter with bipolar switching.

the source voltage. Following points may by observed from the harmonic spectrum:

(a) The fundamental component has a peak value equal to 0.8 (i.e. m_a) times the source voltage. This is true for all values of $m_a < 1$. In other words, the magnitude of the fundamental component varies linearly with m_a, where $m_a < 1$.

(b) The significant harmonics occur as sidebands of m_f (equal to 15 in the present case) and its integral multiples, that is, around m_f, $2m_f$, $3m_f$, and so on. The order of the harmonics may be given by

$$h = jm_f \pm k \tag{8.35}$$

where j is an integer. Here $k = 0, 2, 4$ and so on for odd values of j, and $k = 1, 3, 5$ and so on for even values of j.

Thus, h is always an odd integer provided m_f is chosen as odd integer, which results in odd- and half-wave symmetries of the output voltage.

Unipolar Switching Schemes

In unipolar switching scheme, the switch pairs S_1S_2 and S_3S_4 of the full-bridge inverter of Fig. 8.5, are not operated as pair. Instead, the switches of the first leg, i.e. S_1 and S_4, are operated by comparing the triangular carrier wave (v_c) with the sinusoidal reference signal (v_{ref}). The switches of the other leg, i.e. S_2 and S_3, are operated by comparing v_c with $-v_{ref}$. Following logic is used to operate these switches:

1. If $v_{ref} > v_c$, S_1 is on and if $v_{ref} < v_c$, S_4 is on.
2. If $-v_{ref} > v_c$, S_3 is on and if $-v_{ref} < v_c$, S_2 is on.

The different possible combinations of on-state switches and corresponding voltages are listed as follows:

1. S_1 and S_3 on, $V_{AN} = V$, $V_{BN} = V$, $v_o = V_{AB} = 0$;
2. S_1 and S_2 on, $V_{AN} = V$, $V_{BN} = 0$, $v_o = V_{AB} = V$;
3. S_4 and S_3 on, $V_{AN} = 0$, $V_{BN} = V$, $v_o = V_{AB} = -V$;
4. S_4 and S_2 on, $V_{AN} = 0$, $V_{BN} = 0$, $v_o = V_{AB} = 0$.

Here V_{AN} and V_{BN}, are the potentials of the load terminals A and B, with respect to the reference point N. The waveforms for the unipolar switching scheme, for $m_f = 12$ and $m_a = 0.8$. are shown in Fig. 8.15. It may be observed that the output voltage fluctuates from 0 to $+V$ in the positive half-cycle and from 0 to $-V$ in the negative half-cycle. This scheme is therefore called *unipolar switching* scheme. The output voltage waveform possesses half wave and odd symmetries. This will happen only if m_f is chosen to be an even integer (m_f should be odd in bipolar switching).

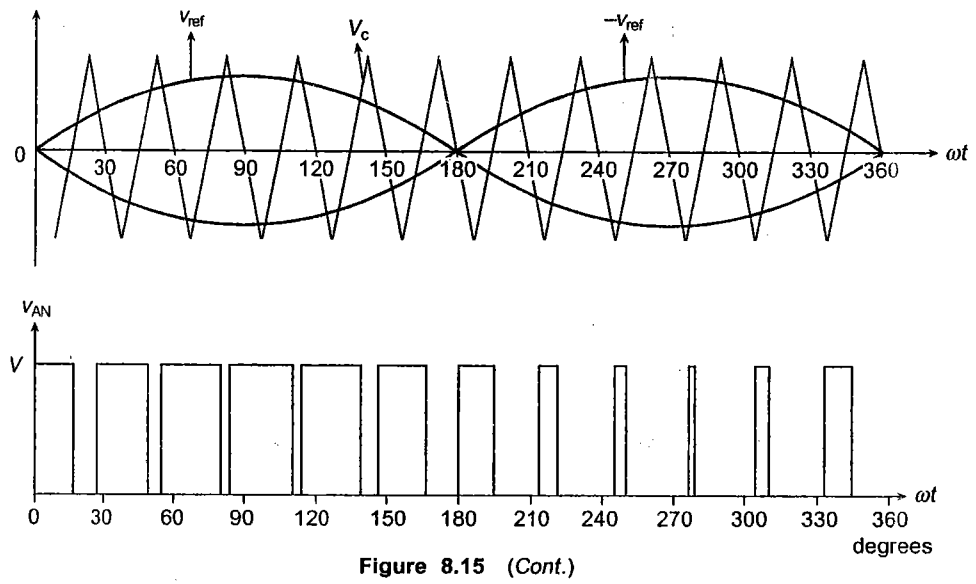


Figure 8.15 (*Cont.*)

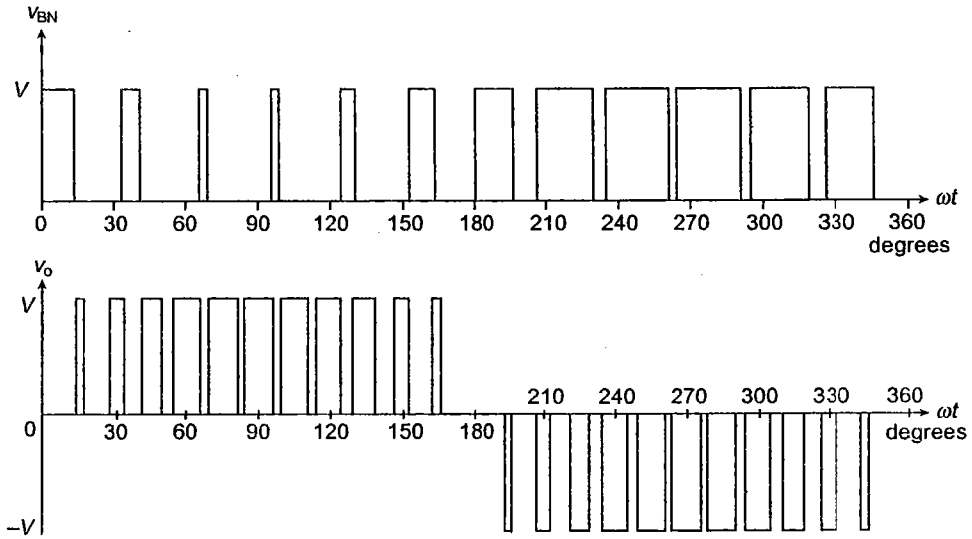


Figure 8.15 Waveforms for unipolar voltage switching scheme.

The harmonic spectrum of the output voltage waveform is shown in Fig. 8.16. Following points may be observed from the harmonic spectrum:

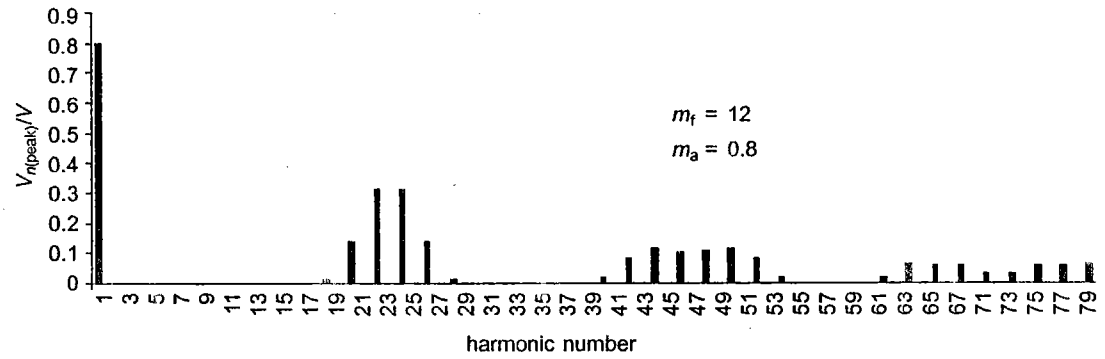


Figure 8.16 Harmonic spectrum of sin-PWM inverter with unipolar switching.

1. Like bipolar switching schemes, the fundamental component has a peak value equal to m_a times the source voltage. This is true for all values of m_a between 0 and 1.
2. The harmonics occur as side bands of $2m_f$ and its integral multiple. The advantage of unipolar switching scheme over the bipolar switching scheme is that the frequencies of the harmonics are doubled. This results in reduction in lower order harmonics. The order of the harmonics can be given by

$$h = j(2m_f) \pm k \tag{8.36}$$

where j is an integer and k is an odd integer.

8.9

PRINCIPLE OF OPERATION OF THREE-PHASE INVERTERS

A three-phase inverter can be formed by connecting three single-phase bridge inverters in parallel. Such a system requires twelve switch-diode pairs and three single-phase transformers. On the other hand, a single three-phase inverter unit consists of six switching devices and six diodes. A three-phase inverter is classified as 180°-conduction or 120°-conduction modes inverter, according to the period of conduction of each switch. The circuit configuration of a three-phase inverter is shown in Fig. 8.17.

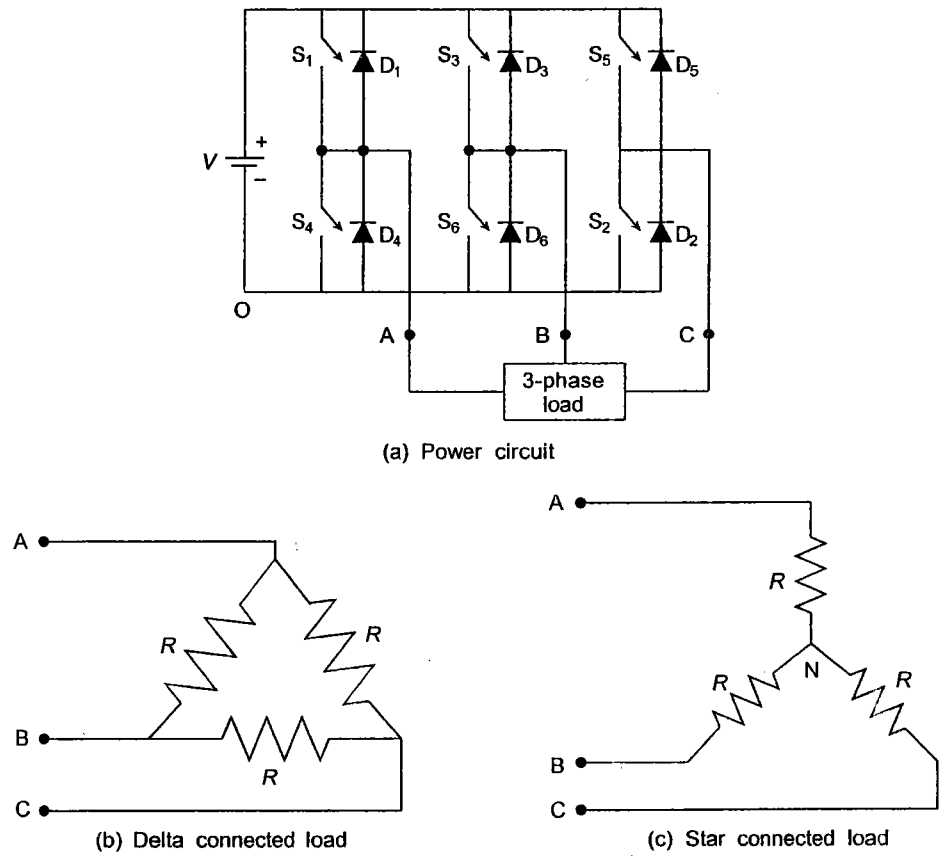


Figure 8.17 A three-phase full-bridge inverter.

8.9.1 180°-CONDUCTION MODE

In this control scheme, each switch conducts for a period of 180° or half-cycle electrical. Switches are triggered in sequence of their numbers with an interval of 60°. The gating signals for switches

are shown in Fig. 8.18. At a time, three switches (one from each leg) conduct. Thus two switches of the same leg are prevented from conducting simultaneously. One complete cycle is divided into six modes, each of 60° intervals.

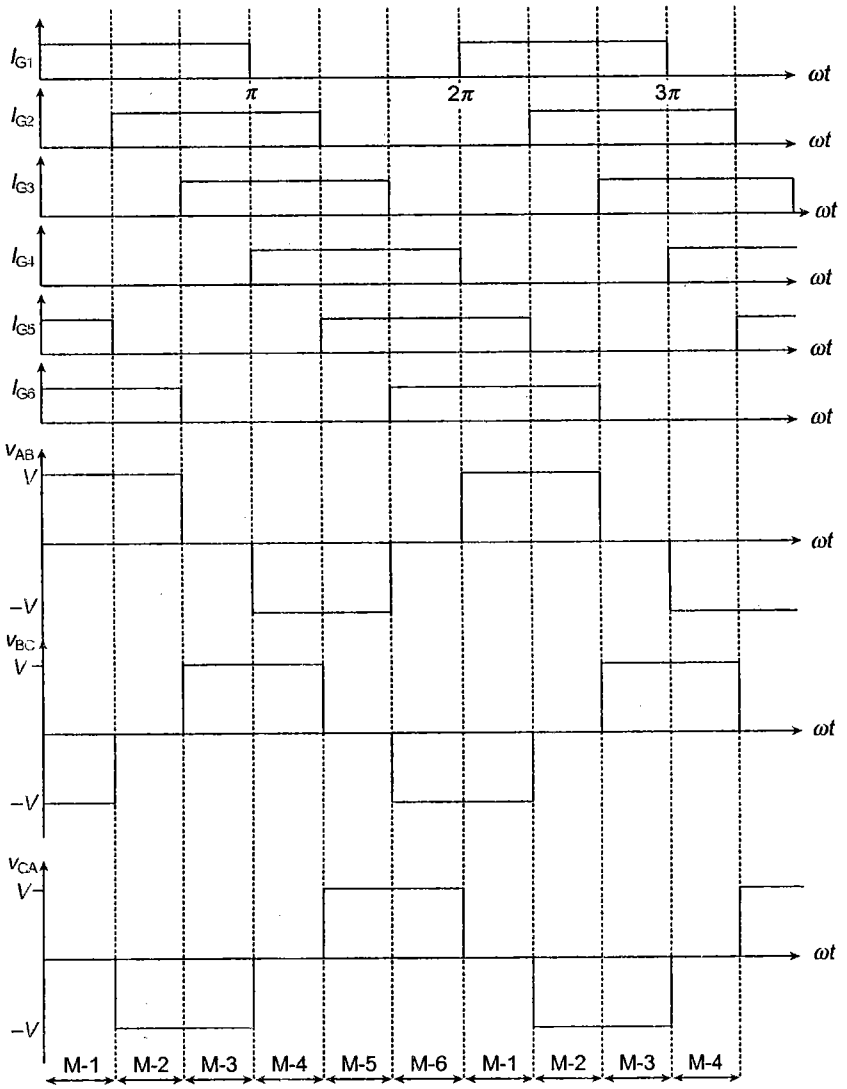


Figure 8.18 Gating signals and output voltages of a three-phase inverter for 180° conduction.

Potential of a load terminal, with respect to the common reference point O, is +V when the upper switch of the corresponding arm conducts and it is zero when the lower switch conducts. The potentials of the three load terminals A, B, and C with respect to the reference point O and the line voltages V_{AB}, V_{BC} and V_{CA} are given in Table 8.1. Waveforms of line voltages are shown in Fig. 8.18.

Table 8.1 Conducting Switches, Load Terminals and Line Voltages

Modes	Conducting switches	Load terminal potentials			Line voltages		
		V_{AO}	V_{BO}	V_{CO}	$V_{AB} = V_{AO} - V_{BO}$	$V_{BC} = V_{BO} - V_{CO}$	$V_{CA} = V_{CO} - V_{AO}$
I	S_5, S_6, S_1	V	0	V	V	$-V$	0
II	S_6, S_1, S_2	V	0	0	V	0	$-V$
III	S_1, S_2, S_3	V	V	0	0	V	$-V$
IV	S_2, S_3, S_4	0	V	0	$-V$	V	0
V	S_3, S_4, S_5	0	V	V	$-V$	0	V
VI	S_4, S_5, S_6	0	0	V	0	$-V$	V

The inverter may supply power to a delta-connected or a star-connected load, as shown in Fig. 8.17. For a delta-connected load, the phase currents can be directly obtained from the line voltages. The line currents can simply be obtained by application of Kirchhoff's current law. To evaluate the phase or line currents for a star-connected load, the phase voltage of the load must be determined. The equivalent circuits for modes I–III may be obtained, as illustrated in Fig. 8.19.

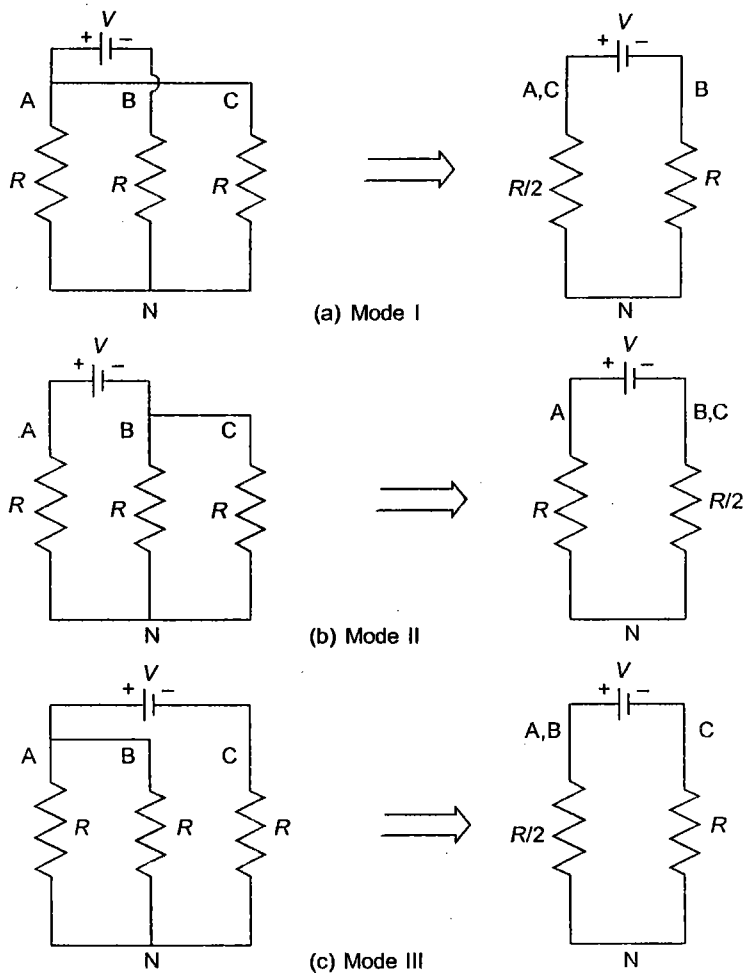


Figure 8.19 Equivalent circuits of star-connected load for 180° conduction.

From the equivalent circuits, phase voltages is given by

During Mode I: **($0 \le \omega t < \pi/3$)** From Fig. 8.19a, we have

$$v_{AN} = v_{CN} = \frac{R/2}{R + (R/2)} V = \frac{V}{3} \quad \text{and} \quad v_{BN} = -\frac{R}{R + (R/2)} V = -\frac{2}{3} V$$

During Mode II: **($\pi/3 \le \omega t < 2\pi/3$)** From Fig. 8.19b, we have

$$v_{AN} = \frac{R}{R + (R/2)} V = \frac{2}{3} V \quad \text{and} \quad v_{BN} = v_{CN} = -\frac{R/2}{R + (R/2)} V = -\frac{1}{3} V$$

During Mode III: **($2\pi/3 \le \omega t \le \pi$)** From Fig. 8.19c, we obtain

$$v_{AN} = v_{BN} = \frac{R/2}{R + (R/2)} V = \frac{V}{3} \quad \text{and} \quad v_{CN} = -\frac{R}{R + (R/2)} V = -\frac{2}{3} V$$

Equivalent circuits for modes IV, V and VI may be obtained by reversing the polarity of the voltage source in the equivalent circuits for modes I, II and III, respectively. The phase voltages are shown in Fig. 8.20.

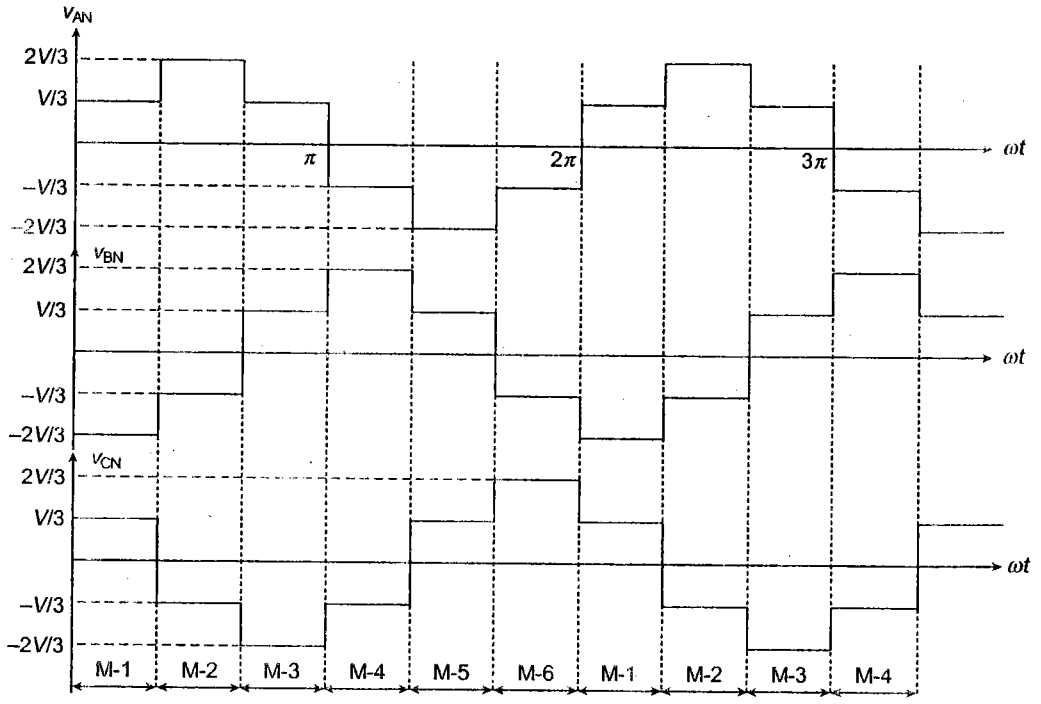


Figure 8.20 Phase voltages of star-connected load for 180° conduction.

The output line voltages can be expressed by the following Fourier expansion:

$$v_{AB} = \sum_{n=2k+1}^{\infty} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \sin\left(n\omega t + \frac{n\pi}{6}\right) \tag{8.37}$$

$$v_{BC} = \sum_{n=2k+1}^{\infty} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \sin\left(n\omega t - \frac{n\pi}{2}\right) \tag{8.38}$$

$$v_{CA} = \sum_{n=2k+1}^{\infty} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \sin\left(n\omega t + \frac{5n\pi}{6}\right) \tag{8.39}$$

where $k = 0, 1, 2, 3, \ldots$.

From equations (8.37)–(8.39), it is obvious that triplen harmonics ($n = 3, 9, \ldots$) are zero.

The line-to-line rms voltage is given by

$$V_L = \left[\frac{2}{2\pi}\int_0^{2\pi/3} V^2 d(\omega t)\right]^{1/2} = \frac{\sqrt{2}}{\sqrt{3}}V = 0.816\ \text{V} \tag{8.40}$$

The rms value of the nth harmonic component of the line voltage is given by

$$V_{Ln} = \frac{1}{\sqrt{2}} \frac{4V}{n\pi} \cos\frac{n\pi}{6} \tag{8.41}$$

The rms value of the fundamental component of line voltage is given by

$$V_{L1} = \frac{1}{\sqrt{2}} \frac{4V}{\pi} \cos\frac{n\pi}{6} = 0.78\ \text{V} \tag{8.42}$$

The rms value of phase voltage is given by

$$V_{ph} = \frac{V_L}{\sqrt{3}} = \frac{\sqrt{2}}{3}V = 0.47\ \text{V} \tag{8.43}$$

The output power of inverter is given by

$$P_L = 3\frac{V_{ph}^2}{R} = \frac{2}{3}\frac{V^2}{R} \tag{8.44}$$

Current of each phase flows through the upper switch of the corresponding leg in one half-cycle and through the lower switch in the other half-cycle. Thus, the rms value of the switch current can be obtained as

$$I_{\text{switch (rms)}} = \frac{I_{ph}}{\sqrt{2}} = \frac{V_{ph}/R}{\sqrt{2}} = \frac{V}{3R} \tag{8.45}$$

8.9.2 120°-CONDUCTION MODE

In this scheme, each switch conducts for 120° duration. Two switches conduct simultaneously in the sequence S_6S_1, S_1S_2, S_2S_3, S_3S_4, S_4S_5, S_5S_6. The switching scheme is shown in Fig. 8.21. A

delay of 60° is provided between the turning-on and turning-off of two switches of each leg. Thus short-circuiting of the dc source is avoided. As only two switches conduct at a time, one load terminal remains floating in this conduction scheme.

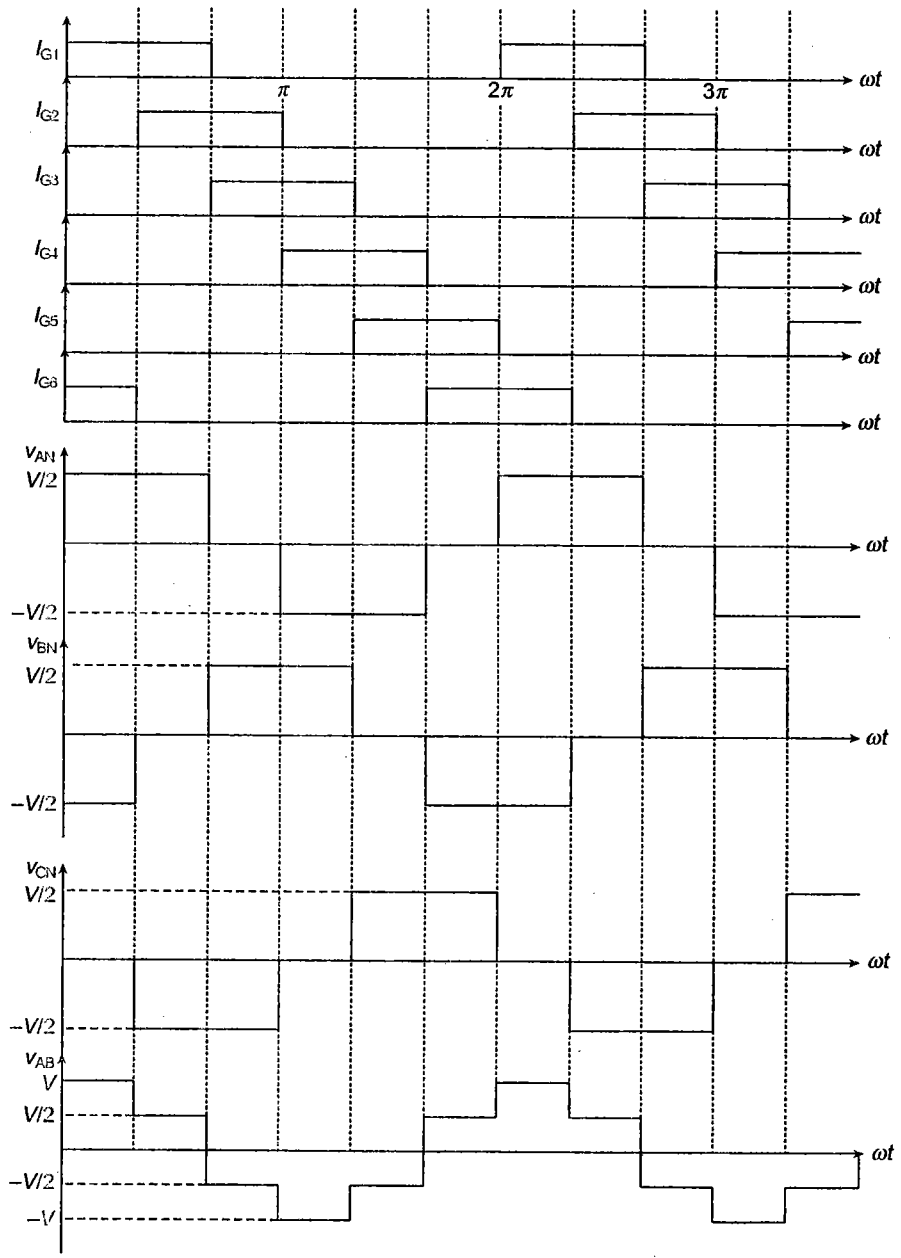


Figure 8.21 Gating signals and output voltages of a three-phase inverter for 120° conduction.

For a balanced Y-connected resistive load, the equivalent circuits are shown in Fig. 8.22. The analysis is presented for half-cycle.

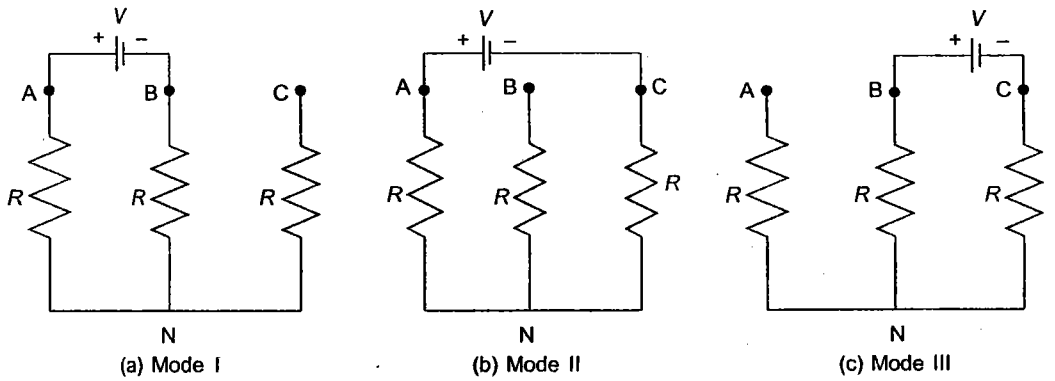


Figure 8.22 Equivalent circuits of a star-connected load for 120° conduction.

Mode I: **($0 \le \omega t < \pi/3$)** From Fig. 8.22a, we have

$$v_{AN} = \frac{V}{2}, \qquad v_{BN} = -\frac{V}{2}, \qquad v_{CN} = 0$$

Then

$$v_{AB} = v_{AN} - v_{BN} = \frac{V}{2} - \left(-\frac{V}{2}\right) = V$$

$$v_{BC} = v_{BN} - v_{CN} = -\frac{V}{2} - 0 = -\frac{V}{2}$$

$$v_{CA} = v_{CN} - v_{AN} = 0 - \frac{V}{2} = -\frac{V}{2}$$

During mode II: **($\pi/3 \le \omega t < 2\pi/3$)** From Fig. 8.22b, we obtain

$$v_{AN} = \frac{V}{2}, \qquad v_{BN} = 0, \qquad v_{CN} = -\frac{V}{2}$$

Then

$$v_{AB} = v_{AN} - v_{BN} = \frac{V}{2} - 0 = \frac{V}{2}$$

$$v_{BC} = v_{BN} - v_{CN} = 0 - \left(-\frac{V}{2}\right) = \frac{V}{2}$$

$$v_{CA} = v_{CN} - v_{AN} = -\frac{V}{2} - \frac{V}{2} = -V$$

Mode III: ($2\pi/3 \leq \omega t \leq \pi$) From Fig. 8.22c, we have

$$v_{AN} = 0, \qquad v_{BN} = \frac{V}{2}, \qquad v_{CN} = -\frac{V}{2}$$

Then

$$v_{AB} = v_{AN} - v_{BN} = 0 - \frac{V}{2} = -\frac{V}{2}$$

$$v_{BC} = v_{BN} - v_{CN} = \frac{V}{2} - \left(-\frac{V}{2}\right) = V$$

$$v_{CA} = v_{CN} - v_{AN} = -\frac{V}{2} - 0 = -\frac{V}{2}$$

Equivalent circuits for modes IV, V and VI may be obtained by reversing the polarity of voltage source in the equivalent circuits for modes I, II and III, respectively. The phase voltages are shown in Fig. 8.21.

The output voltages can be expressed in Fourier series as:

$$v_{AN} = \sum_{n=2k+1}^{\infty} \frac{2V}{n\pi} \cos\frac{n\pi}{6} \sin\left(n\omega t + \frac{n\pi}{6}\right) \tag{8.46}$$

$$v_{BN} = \sum_{n=2k+1}^{\infty} \frac{2V}{n\pi} \cos\frac{n\pi}{6} \sin\left(n\omega t - \frac{n\pi}{2}\right) \tag{8.47}$$

$$v_{CN} = \sum_{n=2k+1}^{\infty} \frac{2V}{n\pi} \cos\frac{n\pi}{6} \sin\left(n\omega t + \frac{5n\pi}{6}\right) \tag{8.48}$$

where $k = 0, 1, 2, 3, \ldots$.

The rms value of fundamental phase voltage,

$$V_{ph1} = \frac{2V}{\sqrt{2}\pi} \cos\frac{\pi}{6} = \frac{\sqrt{3}}{\sqrt{2}\,\pi} V = 0.39 \text{ V} \tag{8.49}$$

The rms value of fundamental line voltage,

$$V_{L1} = \sqrt{3} V_{ph1} = \frac{3V}{\sqrt{2}\pi} = 0.675 \text{ V} \tag{8.50}$$

The rms value of phase voltage,

$$V_{ph} = \left[\frac{1}{\pi} \int_0^{2\pi/3} \left(\frac{V}{2}\right)^2 d(\omega t)\right]^{1/2} = \frac{V}{\sqrt{6}} = 0.408 \text{ V} \tag{8.51}$$

The rms value of line voltage,

$$V_L = \sqrt{3}V_{ph} = 0.707 \text{ V} \tag{8.52}$$

The output power of the inverter,

$$P_L = 3\frac{V_{ph}^2}{R} = \frac{V^2}{2R} \tag{8.53}$$

The rms value of the switch current can be obtained as

$$I_{switch\,(rms)} = \frac{I_{ph}}{\sqrt{2}} = \frac{V_{ph}/R}{\sqrt{2}} = \frac{V}{2\sqrt{3}\,R} \tag{8.54}$$

The load power is given by

$$P_L = 3I_{ph}^2R = 6I_{switch\,(rms)}^2R$$

which gives

$$I_{switch\,(rms)} = \frac{1}{2\sqrt{3}}\frac{V}{R}$$

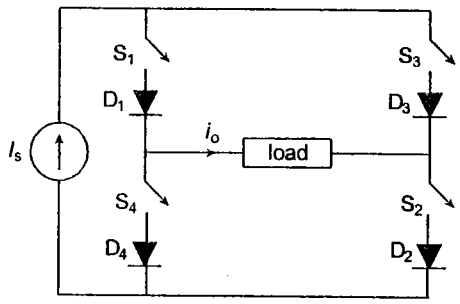
8.9.3 Comparison of 180°- and 120°-conduction Schemes

It may be observed that, for 180°-conduction scheme, there is no delay between switching-on and switching-off of the switches in the same arm. As the turn-off time of a semiconductor switch is more than the turn-on time, both switches of same arm remain conducting for some time and short circuiting of the dc source takes place. This problem is overcome in 120°-conduction scheme by providing a time lag of $T/6$ seconds or $\pi/3$ radians between turn-on and turn-off of two switches of same arm. This results in reliable and safe operation of the inverter, at the cost of poor utilization of switches (i.e. their capacity).

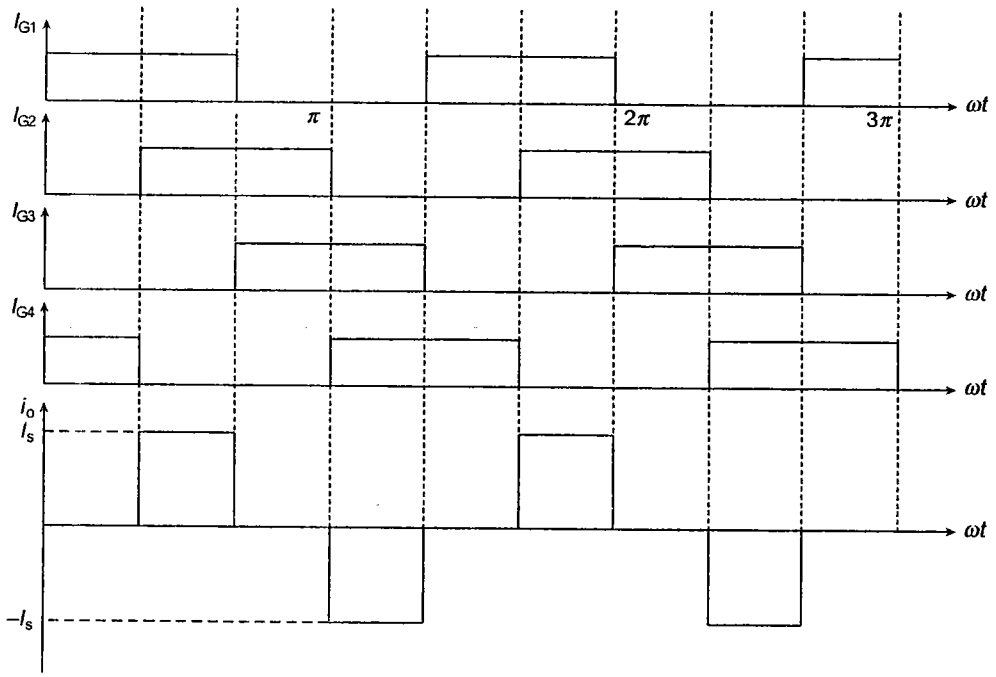
8.10 CURRENT SOURCE INVERTERS

In a current source inverter (CSI), the input is a constant dc current, regardless of the dc input voltage variation. The constant current characteristic is obtained by inserting a high inductor in series with a dc voltage source. The input source could be a controlled rectifier bridge or a combination of uncontrolled converter and a chopper in series with a large inductor. By controlling the output voltage of controlled rectifier or chopper, the dc input current can be controlled. The load current is independent of the nature of load. However, the output voltage depends upon the nature of load.

A basic single-phase CSI, using gate-commutated power semiconductor switches such as, BJT, MOSFET, IGBT, etc., is shown in Fig. 8.23a. A diode is connected in series with each switch to block the reverse voltage across the switch.



(a) Single-phase CSI circuit



(b) Gating signals and output current waveform

Figure 8.23 A basic single-phase CSI using gate-commutated power semiconductor switches.

For continuous flow of a source current, two switches must always conduct—one from upper-half and the other from lower-half. When two switches of opposite arm conduct, the source current flows through the load and when two switches of same arm conduct, the source current bypasses the load. The gating signals and the resulting output current are shown in Fig. 8.23b.

A basic thyristor based single-phase CSI is shown in Fig. 8.24. Capacitors are used here as a commutating device. Initially, let T_1 and T_2 are conducting and the capacitors are charged with the polarities, as shown. The positive load current is flowing through T_1, D_1, load, D_2 and T_2. To commutate the conducting thyristors T_1 and T_2, the other two thyristors T_3 and T_4 are triggered.

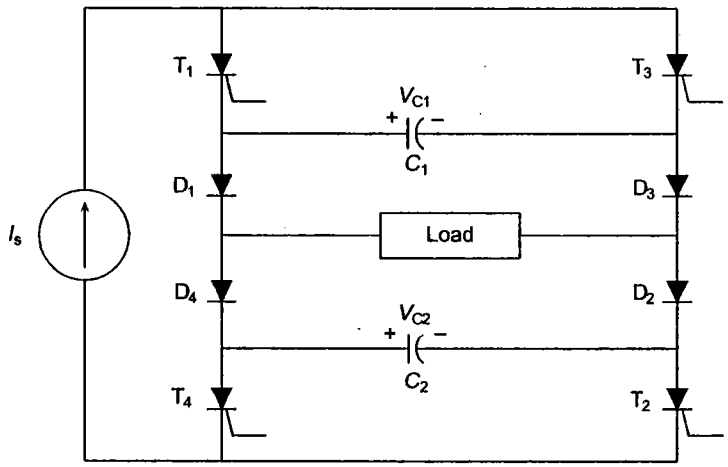
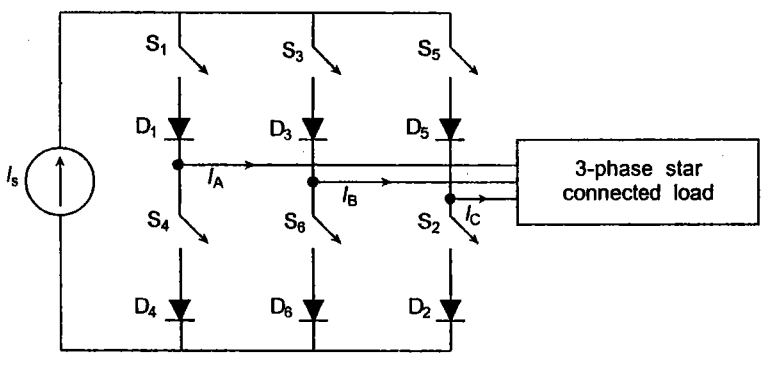


Figure 8.24 Thyristor based current source inverter.

When these thyristors start conducting, the reverse capacitor voltages v_{C1}, and v_{C2} appear across the thyristors T_1 and T_2, respectively, turning them off. Now, the current flows through T_3, C_1, D_1, load, D_2, C_2 and T_4. Now the polarity of the capacitor reverses due to charging current in reverse direction. When the capacitor voltages become equal to the load voltage, the load current falls to zero and the diodes D_1 and D_2 are commutated. The load current now flows in reverse direction through T_3, D_3, load, D_4 and T_4. Similarly, when the thyristors T_1 and T_2 are triggered, the capacitor voltages turn-off T_3 and T_4 in similar fashion.

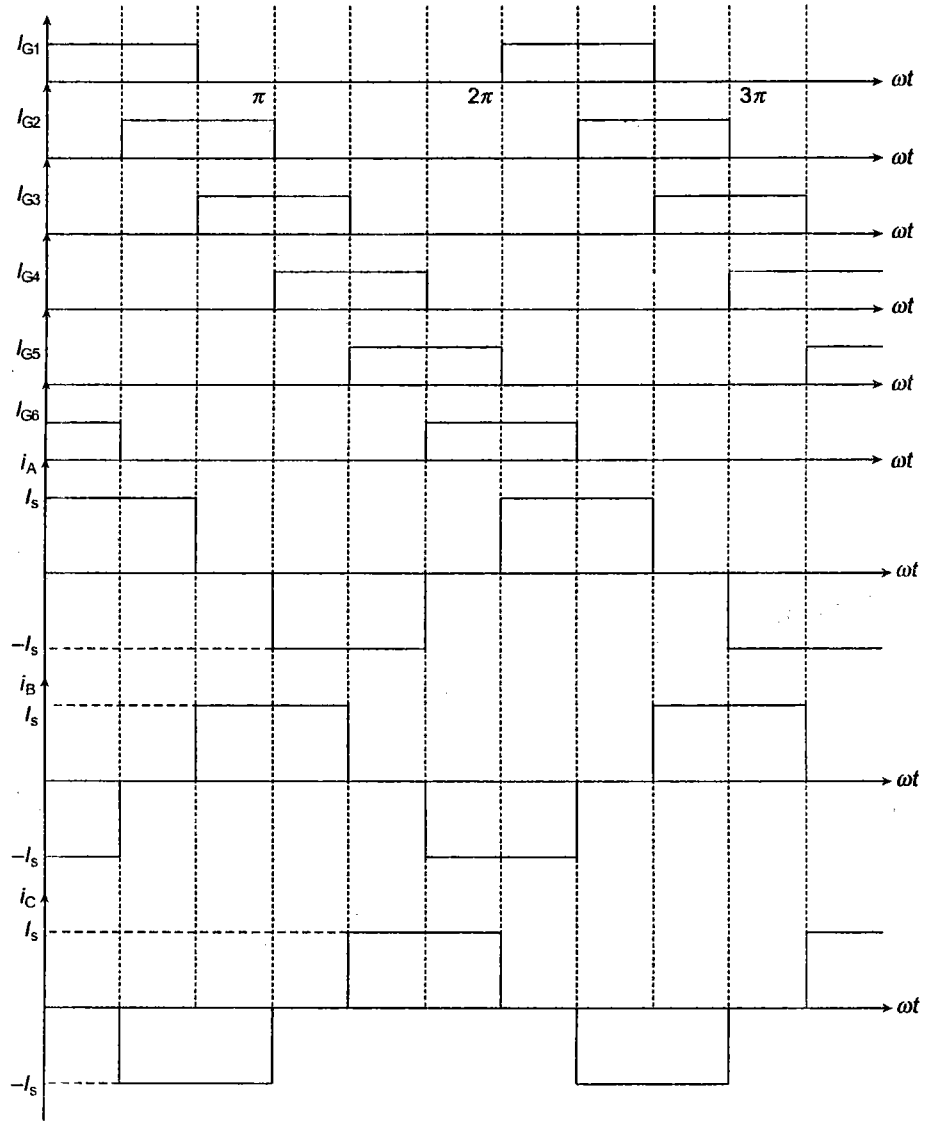
THREE-PHASE CURRENT SOURCE INVERTER

A basic three-phase CSI, feeding a star connected resistive load, is shown in Fig. 8.25a. Diodes are used in series with each switch to handle reverse voltage, which should be avoided to appear across the power semiconductor based switches. The switches are turned on in sequence of their numbers, with an interval of 60° and each switch conducts for 120° duration. At a time two



(a) Circuit

Figure 8.25 (*Cont.*)



(b) Gating signals and output currents

Figure 8.25 A three-phase CSI.

switches conduct—one from the upper group and other from the lower group. The load current of a particular phase is $+I_s$ when upper switch of the corresponding arm conducts, and it is $-I_s$ when the lower switch conducts.

The major advantage offered by a CSI is its short-circuit fault protection. Since the input is a controlled current source, the current does not rise to a dangerously high level in the event of a fault. It makes the converter highly reliable and it is used in fast traction drives (National Grande, France). A thyristor based CSI has a simple commutation circuit and it may use a

converter grade thyristor which is cheaper than the inverter grade counterpart. As a converter is used as an input source, the converter–inverter combination has inherent four-quadrant operation capability. However, a CSI suffers stability problems on light loads and operating problems at high frequency. Moreover, its response is sluggish.

A CSI finds its applications mainly in a 3-phase induction motor drive, lagging VAR compensator and solar photo-voltaic utility systems, etc.

8.11

FORCED COMMUTATED THYRISTOR-BASED INVERTERS

For low- and medium-power applications, gate commutated power devices, like BJT, MOSFET, IGBT, etc., are used. For high-voltage applications, these devices are to be connected in series, and for high-current applications, these are connected in parallel. For high-power applications (e.g. HVDC transmission) both series and parallel combinations of these devices are required. This makes the control circuit quite complex. In such cases thyristor based inverters are used. The commonly used voltage source inverters are: modified McMurray inverter and McMurray–Bedford inverters.

8.11.1 Modified McMurray Inverter

This inverter uses auxiliary commutation scheme to turn off a conducting thyristor. A single-phase modified McMurray half-bridge inverter is shown in Fig. 8.26. The main inverter circuit is similar to the half-bridge circuit of Fig. 8.1, except that it uses thyristors T_1 and T_2 in place of gate commutated switches S_1 and S_2. The commutation circuit consists of two auxiliary thyristors TA_1 and TA_2 along with anti-parallel diodes DA_1 and DA_2, commutating elements L and C, and damping resistance R. To transfer current from T_1 to T_2, TA_1 is triggered and to transfer current from T_2 to T_1, TA_{21} is triggered.

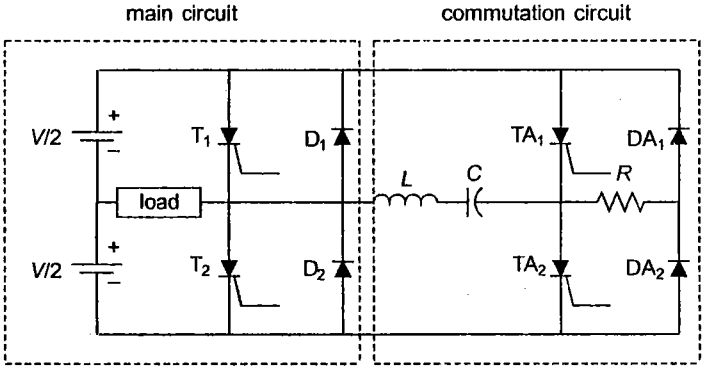


Figure 8.26 Circuit of a modified McMurray half-bridge inverter.

For the sake of simplification, it is assumed that all the devices and circuit elements are ideal. Moreover, it is assumed that the load is highly inductive so that the load current remains constant during commutation interval. The operation is divided into eight modes. The equivalent circuits for different modes are shown in Fig. 8.27, wherein, thick lines show conducting part of the circuit, and non-conducting parts are shown by dotted lines. The relevant waveforms are shown in Fig. 8.28.

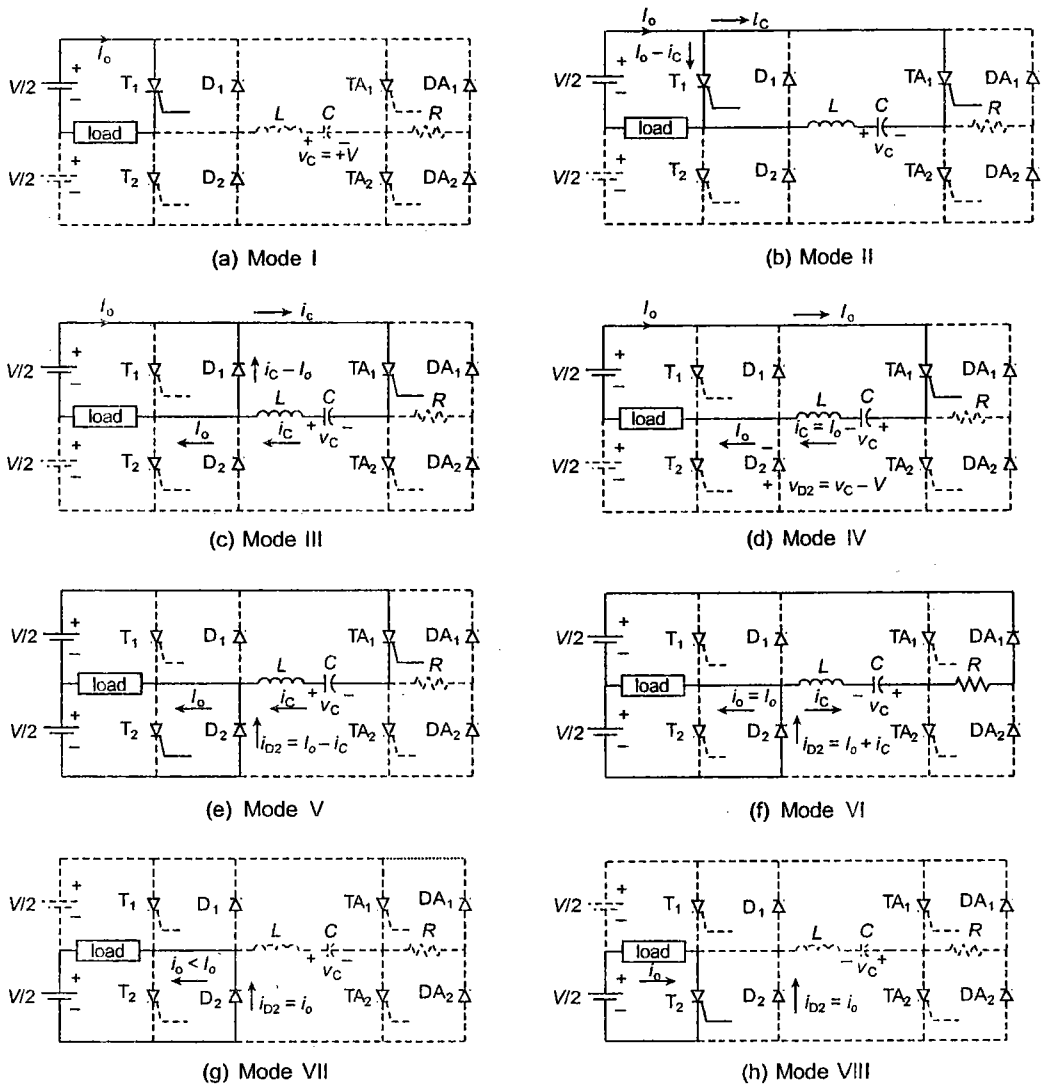


Figure 8.27 Different modes of operation of a modified McMurray half-bridge inverter.

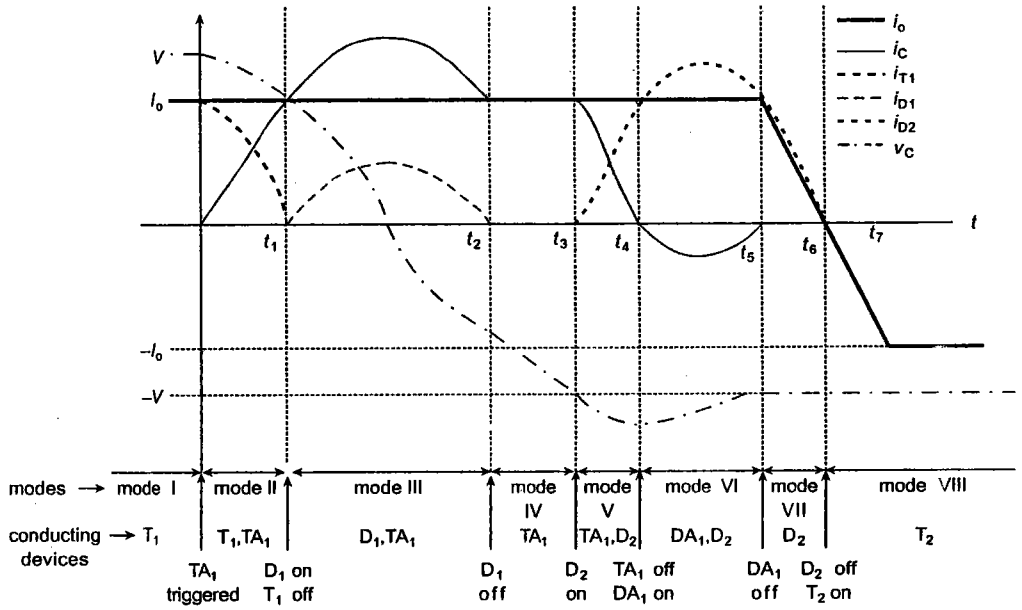


Figure 8.28 Waveforms of a modified McMurray half-bridge inverter.

Mode I ($t < 0$) In this mode main thyristor T_1 conducts and a constant positive load current (I_o) flows. The load voltage is positive and the capacitor is charged up to $+V$ (left plate positive), as shown in Fig. 8.27a. The auxiliary thyristor TA_1 is forward biased by the capacitor voltage.

Mode II ($0 < t < t_1$) TA_1 is triggered at $t = 0$ to commutate T_1. This results in flow of resonating current i_C through L, C, T_1 and TA_1, as shown in Fig. 8.27b. This current increases while the net current through T_1 ($i_{T1} = I_o - i_C$) reduces. At $t = t_1$, i_C becomes equal to I_o while i_{T1} reduces to zero. Then T_1 turns-off.

Mode III ($t_1 < t < t_2$) As the resonating current i_C becomes higher than the load current (I_o), the surplus current ($i_C - I_o$) flows through the diode D_1, as shown in Fig. 8.27c. The resonating current reaches the peak value and the falls to I_o at t_2, as shown in Fig. 8.28. The current through D_1, (i_{D1}), also becomes zero at t_2 which commutates D_1. During this interval, the capacitor voltage reduces. It becomes negative (right plate positive) after i_C reaches its peak value.

Mode IV ($t_2 < t < t_3$) When D_1 turns off at the end of mode-III, the capacitor is charged in reverse direction (right plate positive) by the constant load current I_o. During this interval, the voltage across diode D_2, v_{D2}, is equal to $v_c - V$. (This may be verified by applying KVL to the path formed by the voltage source, TA_1, C, L and D_2.) At t_3, the capacitor charges to a voltage slightly higher than V. This results in forward biasing of D_2, and D_2 turns on.

Mode V ($t_3 < t < t_4$) When D_2 turns on, I_o is shared by i_{D2} and i_C, as shown in Fig. 8.27e. As i_C decreases, i_{D2} increases, which is equal to ($I_o - i_C$). At t_4, $i_C = i_{TA1} = 0$ and TA_1 turns off. After t_3, trigger signal is given to T_2. However, it will turn on only when D_2 turns off.

Mode VI ($t_4 < t < t_5$) As i_C tries to reverse at t_4, DA_1 turns on. At this instant, the capacitor voltage is more than the source voltage. Now the capacitor discharges through V, D_2, L, DA_1 and the damping resistance R. At t_5, the capacitor current falls to zero and DA_1 is commutated. Moreover, the capacitor is charged up to $-V$ (right plate positive).

Mode VII ($t_5 < t < t_6$) During this interval, i_o flows through D_2 and the lower source, as shown in Fig. 8.27g. The load current reduces under the influence of the negative source voltage. At t_6, i_o becomes zero and D_2 turns off.

Mode VIII ($t > t_6$) When D_2 turns off, T_2, which is already recieving the gate signal, turns on. It conducts and the negative load current (Fig. 8.27h), rises to become equal to I_o at $t = t_7$. At this instant, the capacitor voltage forward biases the auxiliary thyristor TA_2. To initiate the turn-off process of T_2, TA_2 will be triggered.

In McMurray inverter, the trapped voltage across the capacitor, after the commutation process, is higher than the input voltage ($v_C > V$). In case of a modified McMurray inverter, a branch consisting of D_{A1}, D_{A2} and R is added in the basic McMurray inverter circuit. The excess potential left across the capacitor is reduced to the level of source voltage. The capacitor discharges through the oscillatory path consisting of L, C, R, D_{A1} and the dc source, till it becomes equal to V. Thus the capacitor is charged up to a fixed level, V, irrespective of load current.

The circuit of a single-phase modified McMurray full-bridge inverter is shown in Fig. 8.29. The circuit uses two auxiliary commutation circuits, one for each leg. Triggering of thyristor pair TA_1–TA_2 turns off the thyristor pair T_1–T_2 and triggering of thyristor pair TA_3–TA_4 turns off thyristor pair T_3 – T_4.

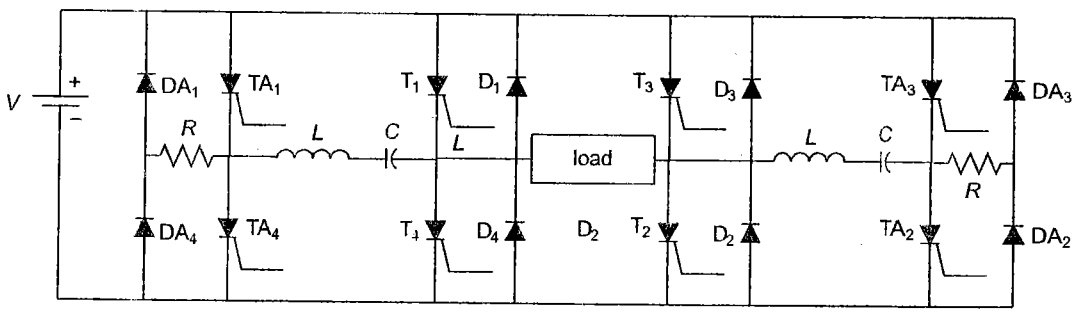


Figure 8.29 A modified McMurray full-bridge inverter.

8.11.2 McMurray–Bedford Inverter

This type of inverter employs complementary voltage commutation scheme. The basic circuit of a single-phase half-bridge McMurray–Bedford inverter is shown in Fig. 8.30. The main circuit consists of thyristors (T_1 and T_2) along with anti-parallel diodes (D_1 and D_2). The commutation circuit has a center-tapped inductor and two equal capacitors C_1 and C_2. The two halves of the inductor, L_1 and L_2, are tightly coupled.

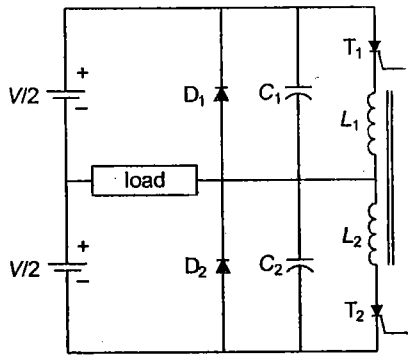
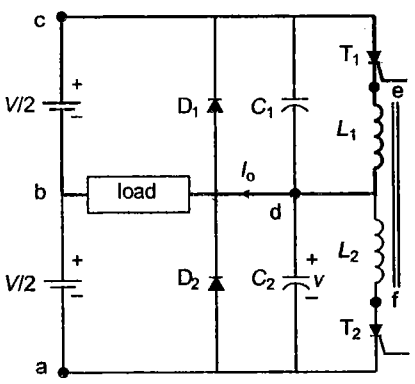
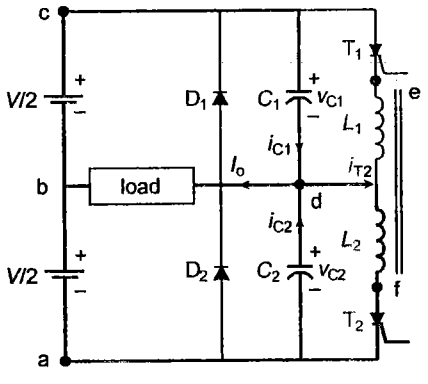
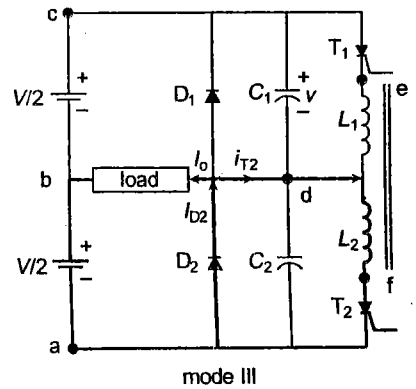


Figure 8.30 Single-phase half bridge McMurray–Bedford inverter.

For the sake of simplicity, all the devices and circuit elements are assumed to be ideal and the load current is assumed to be constant during the commutation interval. The operation of the inverter may be divided into five modes. The equivalent circuits for the different modes are shown in Fig. 8.31. In the figure, thick lines show the conducting part of the circuit. The relevant voltage and current waveforms are shown in Fig. 8.32.







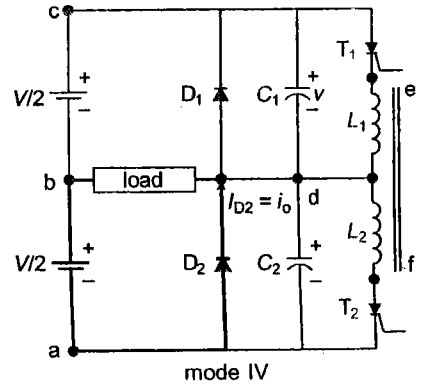


Figure 8.31 (*Cont.*)

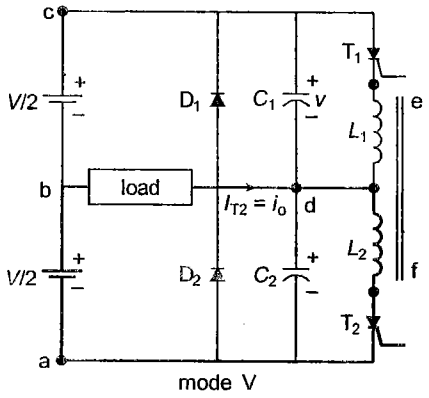


Figure 8.31 Different modes of operation of a McMurray–Bedford inverter.

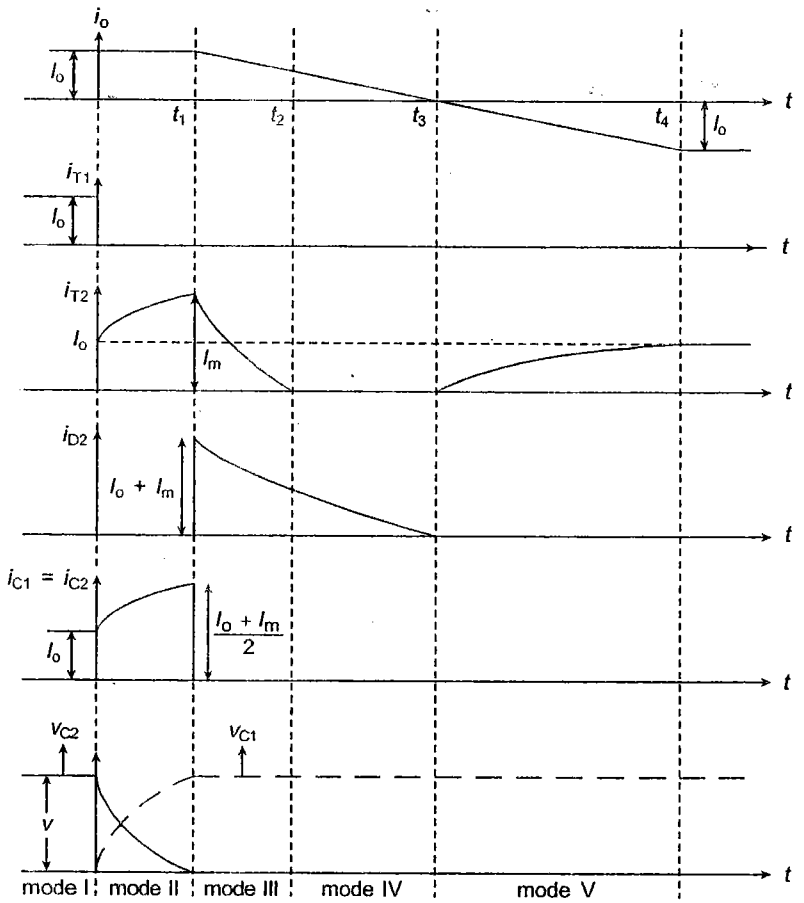


Figure 8.32 Voltage and current waveforms of McMurray–Bedford inverter.

Mode I **($t < 0$)** In this mode, the thyristors T_1 conducts and supplies the positive load current (I_o), as shown in Fig. 8.31. As I_o is constant, the voltage across the inductor, L_1 is zero. The potential of point 'd' is V, with reference to the point 'a'. Therefore, the source voltage appears across the capacitor, C_2 and the thyristors, T_2. During this interval, $v_{C1} = 0$ and $v_{C2} = V$.

Mode II **($0 < t < t_1$)** This mode begins at $t = 0$, when T_2 is triggered by applying a positive gate pulse. As soon as T_2 starts conducting, point 'f' gets connected to the negative supply terminal and the capacitor voltage (V) appears across the inductor, L_2. As L_1 and L_2 are tightly coupled, same voltage is induced in L_1. As a result, potential of point 'e' rises to $2V$ and a reverse voltage ($-V$) appears across T_1 to turn it off. The current carried by the upper half of the inductor (L_1) is immediately transferred to the lower half (L_2) so as to maintain constant flux in the inductor core. Thus, at $t = 0+$, $i_{T1} = 0$, and $i_{T2} = I_o$.

A loop is formed by the voltage source and the two capacitors ($v_{C1} + v_{C2} = V$). The expressions of the capacitor voltages (v_{C1} and v_{C2}) in terms of capacitor currents (i_{C1} and i_{C2} respectively), are given by

$$\frac{1}{C_1}\int i_{C1}\,dt + v_{C1}(t=0) - \frac{1}{C_2}\int i_{C2}\,dt + v_{C2}(t=0) = V$$

or

$$\frac{1}{C_1}\int i_{C1}\,dt + 0 - \frac{1}{C_2}\int i_{C2}\,dt + V = V$$

or

$$\frac{1}{C_1}\int i_{C1}\,dt = \frac{1}{C_2}\int i_{C2}\,dt$$

As $C_1 = C_2$, $i_{C1} = i_{C2}$. Applying Kirchhoff's current law at the junction 'd',

$$i_{C1} + i_{C2} = I_o + i_{T2}$$

or

$$i_{C1} = i_{C2} = \frac{I_o + i_{T2}}{2}$$

The capacitor C_2 discharges through the resonating circuit formed by C_2, L_2 and T_2. As $v_{C1} + v_{C2} = V$, the capacitor C_1 charges at the same rate. The resonating current i_{T2} rises from I_o (at $t = 0$) to the peak value, I_m (at $t = t_1$). At this instant, the capacitor C_2 is discharged to zero voltage and the capacitor, C_1 is charged up to the source voltage.

Mode III **($t_1 < t < t_2$)** At the end of time t_1, the direction of capacitor current and the polarity of the capacitor voltage tend to reverse, effecting turn-on of the diode, D_2. Now the stored energy in L_2 starts dissipating through D_2 and T_2. Adding a series resistance with D_2 can make the energy dissipation faster. When entire stored electromagnetic energy is dissipated, the current through T_2 ceases leading to its turn-off at $t = t_2$.

Mode IV **($t_2 < t < t_3$)** After the thyristor T_2 turns-off (at $t = t_2$), the load current flows through D_2. As the load voltage is reversed, the load current decreases and falls to zero at $t = t_3$.

Mode V ($t > t_3$) When the current through D_2 becomes zero, the reverse bias across T_2 is removed. Since gate signal of T_2 is available for the complete half-cycle, to turns it on. The negative load current starts flowing through T_2. This current varies up to $-I_o$ at $t = t_4$.

8.12

VOLTAGE CONTROL OF INVERTERS

An inverter may require voltage control to:

- cope with the variations in the input dc voltage
- compensate the voltage regulation of the inverter switches and transformer
- provide variable or adjustable voltage to the load.

Certain loads, such as variable frequency induction motor drive, require simultaneous control of frequency and voltage. Controlling the conduction intervals of the inverter switches can control frequency of the inverter output. Voltage control may be done by any of the following techniques:

1. Control of input dc voltage
2. External control of inverter ac output voltage
3. Internal control of inverter.

8.12.1 Control of Input dc Voltage

The output voltage of an inverter may be controlled by controlling the input dc voltage supplied to the inverter. Figure 8.33 shows the various schemes used to control the input dc voltage. If the basic source is dc, variable dc voltage may be obtained using a chopper or a dc-to-dc converter, as shown in Fig. 8.33a. If the basic source is ac, variable dc voltage may be obtained using any of the schemes shown in Fig. 8.33b–d.

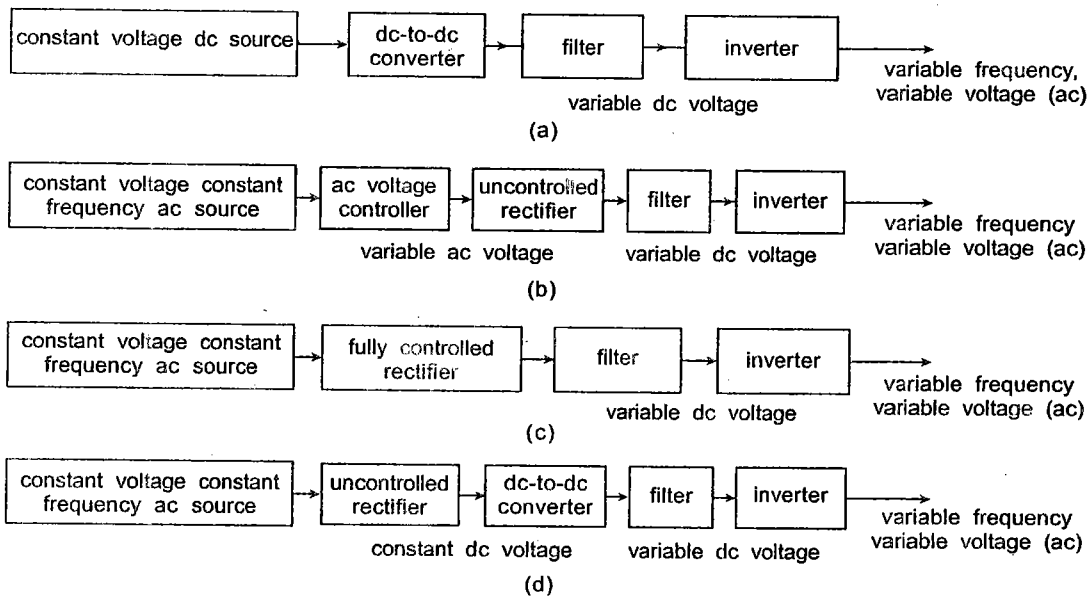


Figure 8.33 Inverter voltage control by control of dc input voltage.

In the scheme of Fig. 8.33b, the input ac voltage is first converted into a variable ac voltage using an ac voltage controller and then it is converted into dc with the help of an uncontrolled rectifier. In this system, variable voltage, variable frequency ac is obtained after three conversion stages. Obviously, efficiency of the system is poor. Moreover, the input power factor becomes poor at low voltages.

Figure 8.33c shows an improved scheme. In this scheme, variable dc voltage is obtained using a controlled rectifier. As only two conversion stages are required, the efficiency of the system is better than that for the previous scheme. At low output voltages, the input power factor is poor. Another drawback of the scheme is that the output of the controlled rectifier contains appreciable amount of low-frequency harmonics. Therefore, large size filter components are required. This makes the system response sluggish.

Drawbacks of the system of Fig. 8.33c are removed in the system shown in Fig. 8.33d. This system converts the input voltage into dc using an uncontrolled rectifier. The constant dc voltage is then converted into a variable dc using a high-frequency (dc-to-dc converter). As the chopper operates at a high frequency, its output contains harmonics at very high frequencies. Thus the size of filter components is reduced. Moreover, the fundamental input power factor remains unity under all conditions of operation. However, losses in the system increase due to use of an additional converter.

8.12.2 External Control of ac Output Voltage

The constant ac output voltage (rms) from an inverter may be controlled using an ac voltage regulator (ac phase control). This method introduces a large harmonic content in the output voltage. Moreover, the method can be used only for small power applications.

For high-power applications, two square-wave inverters may be connected in series to obtain variable ac voltage, as shown in Fig. 8.34. The output voltages of the inverter-I and inverter-II are

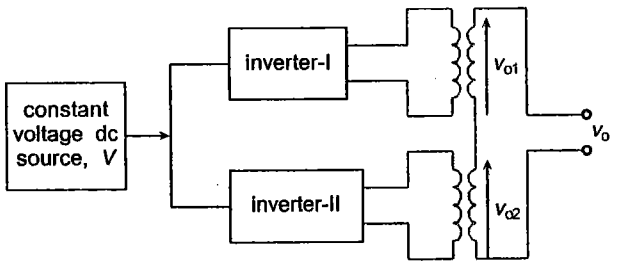


Figure 8.34 Series-connected inverters.

given to the primaries of the two transformers, whose secondary windings are connected in series. The output voltages of the two transformers, v_{o1} and v_{o2}, have same magnitude. The phase angle between v_{o1} and v_{o2}, φ, can be controlled by controlling the phase angle between the control signals of the two inverters. The resultant output voltage (v_o) has a constant magnitude $2V$ (double the peak of v_{o1} and v_{o2}) and a variable pulse width, π-φ, as shown in Fig. 8.35. By varying φ from 0 to π, the width of output pulses may be varied from π to 0 and hence the output voltage may be controlled from $2V$ to zero. At low voltages, it becomes a thin pulse, the harmonic contents in the output voltage become large. Therefore, this method of voltage control is used for voltage control (lower side) up to 25 to 30 per cent of the rated voltage.

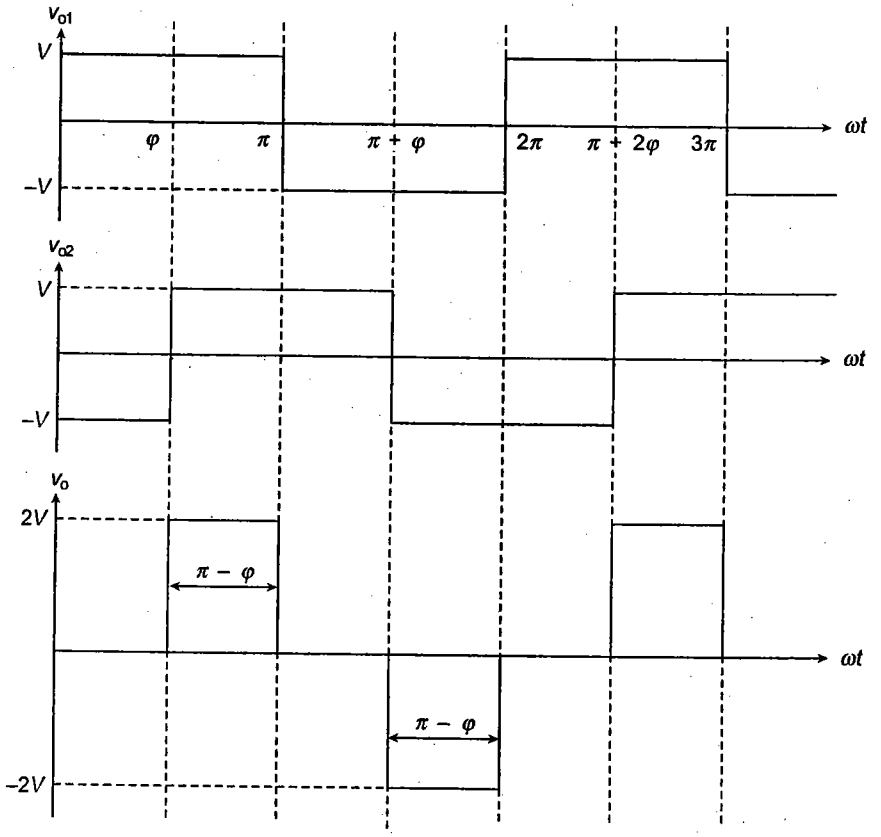


Figure 8.35 Waveforms of series-connected inverters.

8.12.3 Internal Control of Inverters

In this technique, the voltage control is obtained within the inverter. The output of the inverter is in the form of a pulse width modulated wave. Controlling the width of output pulses, controls the output voltage. This method not only provides variable output voltage but also eliminates certain low frequency harmonics, which are responsible for poor performance. This method is therefore, the most popular method of voltage control of inverter. Depending on the required range of voltage control and required performance, a suitable PWM technique may be used. The different PWM techniques are already discussed in Section 8.8.

Example 8.1 A single-phase, half-bridge inverter feeds a resistive load (R = 10 Ω). If the source voltage is 240 V, determine

(a) the rms value of fundamental component of output voltage,
(b) the output power,
(c) the peak off-state voltage across each semiconductor switch,
(d) the lowest order harmonic and the corresponding harmonic factor, and
(e) the rms and average values of currents through semiconductor switches.

Solution The magnitude of square-wave output voltage for the half-bridge inverter,

$$V_L = \frac{240}{2} = 120\ \text{V}$$

The output voltage may be expressed in Fourier series, using equation (8.21) as

$$v_o(t) = \sum_{n=1,3,5}^{\infty} \frac{4V_L}{n\pi} \sin(n\omega t)$$

$$= \frac{4 \times 120}{\pi} \sum_{n=1,3,5} \frac{\sin(n\omega t)}{n}$$

$$= 152.79\left[\sin(\omega t) + \frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \cdots\right]$$

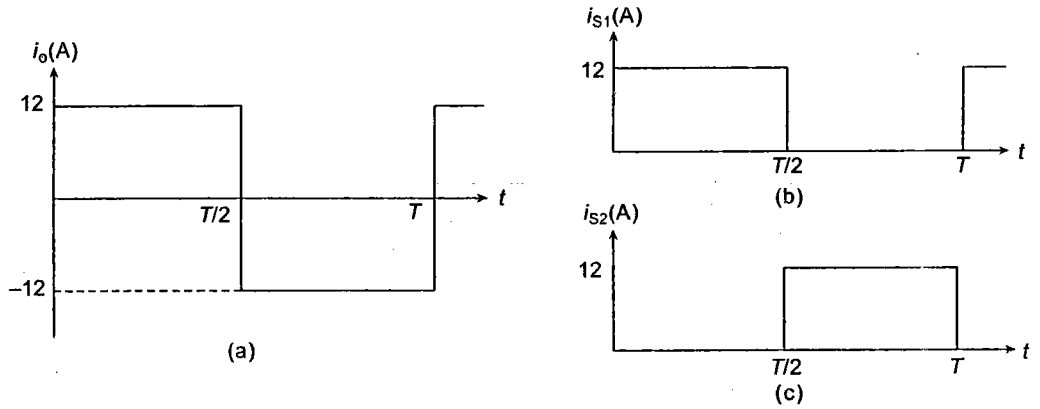


Figure 8.36 Waveforms of (a) output current (b) upper switch current (c) lower switch current (Example 8.1).

Now, we get the following:

(a) The rms value of fundamental component of the output voltage, $V_1 = 152.79/\sqrt{2} = 108.04$ V.

(b) The output power is given by $P_o = V_o^2/R$.
where V_o is the rms value of the output voltage. For the square-wave output, $V_o = V_L = 120$ V. Therefore, $P_o = 120^2/10 = 1440$ W.

(c) The peak voltage that appears across each semiconductor switch is $2V_L = 2 \times 120 = 240$ V.

(d) The lowest order harmonic is the third harmonic, which has rms value equal to $V_3 = 152.79/(3\sqrt{2}) = 36.01$ V. The corresponding harmonic factor is

$$\text{HF}_3 = \frac{V_3}{V_1} = \frac{36.01}{108.04} = 0.333.$$

(e) The output current has a square-wave shape with magnitude 120/10 = 12 A, as shown in Fig. 8.36a. In the positive half-cycle, the load current flows through the switch S_1 and in the negative half-cycle, the switch S_2 carries the load current. The waveforms of the currents through switches S_1 and S_2 are shown in Fig. 8.36b and c, respectively.

The average switch current may be obtained as

$$I_{s(avg)} = \frac{1}{T}\int_0^{T/2} 12\,dt = \frac{12(T/2)}{T} = 6 \text{ A}$$

The rms switch current is given by

$$I_{s(rms)} = \left[\frac{1}{T}\int_0^{T/2} (12)^2\,dt\right]^{1/2} = \left[\frac{1}{T} \times (12)^2 \times \frac{T}{2}\right]^{1/2} = \frac{12}{\sqrt{2}} = 8.48 \text{ A}$$

Example 8.2 A single-phase, half-bridge inverter with source voltage (total) $V = 500$ V, feeds an *RL* load with $R = 20\ \Omega$, and $L = 0.1$ H. If the frequency of the output voltage is 50 Hz, determine (a) the output current at the end of first cycle, (b) the expression of steady-state output current for both the half cycles and (c) the THD of load current.

Solution For the half-bridge inverter the magnitude of the square-wave voltage waveform V_L = V/2 = 250 volt. The time constant of the *RL* load $\tau = L/R = 0.1/20 = 0.005$ s. Time period of the output voltage $T = 1/50 = 0.02$ s.

(a) At $t = 0$, the *RL* load is subjected to a step function with magnitude V_L. The voltage equation is given by

$$V_L = Ri_o(t) + L\frac{di(t)}{dt}$$

Thus

$$i_o(t) = \frac{V_L}{R}\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] + I_o \exp\left(-\frac{t}{\tau}\right)$$

where I_o is the current at $t = 0$, which is zero in the present case. Putting the values, we get

$$i_o(t) = \frac{250}{20}\left[1 - \exp\left(-\frac{t}{0.005}\right)\right] = 12.5(1 - e^{-200t})$$

At half time period, i.e. $t = T/2 = 0.01$ s,

$$i_o = 12.5(1 - e^{-2}) = 10.81 \text{ A}$$

For the next half-cycle, the load voltage reverses and the load current is given by

$$i_o(t') = -12.5\ [1 - \exp(-200t')] + 10.81 \exp(-200t')$$

where $t' = t - (T/2)$. At the end of the first cycle,

$$t' = 0.02 - \frac{0.02}{2} = 0.01 \text{ s}$$

Then

$$i_o = -12.5\,[1 - \exp(-2)] + 10.81 \exp(-2) = -9.345 \text{ A}$$

(b) The steady state load current for the positive half-cycle can be obtained, from (8.5) as

$$i_o = \frac{V_L}{R}\left[1 - \frac{2}{1 + e^{-T/(2\tau)}} e^{-t/\tau}\right]$$

$$= \frac{250}{20}\left[1 - \frac{2}{1 + e^{-2}} e^{-200t}\right]$$

$$= 12.5\,(1 - 1.76\, e^{-200t})$$

For the negative half-cycle, from (8.7), the load current is given by

$$i_o = -12.5\,(1 - 1.76\, e^{-200\,(t\,-\,0.01)})$$

(c) Using (8.26), the rms value of the nth harmonic component is given by

$$I_n = \frac{4V_L}{n\pi\sqrt{2}\sqrt{R^2 + (n\omega L)^2}} = \frac{225.08}{n\sqrt{400 + 986.96n^2}}, \quad n = 1, 3, 5, \ldots$$

Putting different values of n, we get

$$I_1 = 6.044, \quad I_3 = 0.7785, \quad I_5 = 0.2845, \quad I_7 = 0.1455, \quad I_9 = 0.088, \quad I_{11} = 0.0585, \ldots$$

The THD for the load current may be obtained as

$$\text{THD}_i = \frac{\sqrt{I_3^2 + I_5^2 + I_7^2 + I_9^2 + I_{11}^2 + \cdots}}{I_1} = 0.1403 \text{ or } 14.03\%$$

Note: THD_i is 14.03%, which is far less than THD_v, which is 48.34%. This is because of the higher impedance offered by the inductance to the high-frequency harmonics, which are filtered out.

Example 8.3 The square-wave voltage, shown in Fig. 8.37, is applied to an RC load with $R = 10\ \Omega$, $C = 2000\ \mu\text{F}$. Draw the waveforms of the capacitor voltage and capacitor current (a) for the first cycle and (b) under steady-state condition.

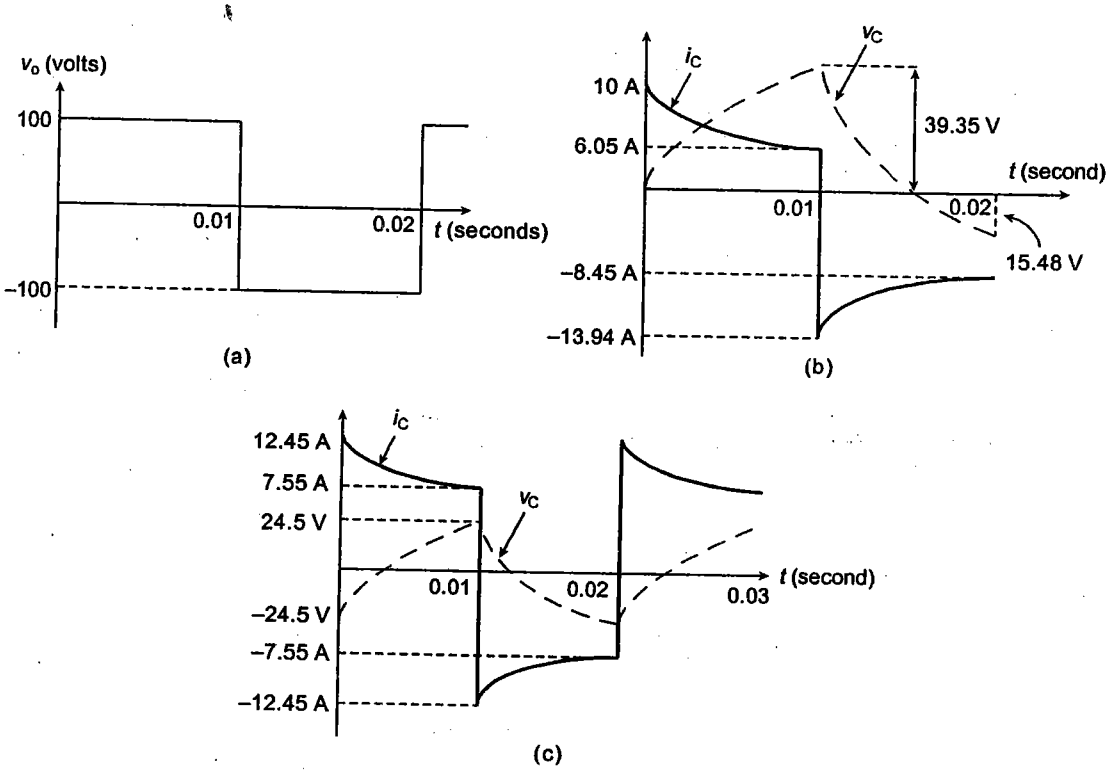


Figure 8.37 Solution to example 8.3

Solution

(a) The voltage equation of a series RC circuit is given by

$$v = Ri + \frac{1}{C}\int i\,dt \tag{1}$$

In terms of capacitor voltage, v_C, the above equation is given by

$$v = RC\frac{dv_C}{dt} + v_C \tag{2}$$

In the present case, v is equal to $+V$ for the positive half-cycle and $-V$ for the negative half-cycle. Therefore, for the positive half-cycle,

$$V = RC\frac{dv_C}{dt} + v_C$$

The solution of the differential equation is given by

$$v_c = V[1 - e^{-t/(RC)}] + v_{C0}\, e^{-t/(RC)} \tag{3}$$

where v_{C0} is the voltage across the capacitor at $t = 0$. Here

$$v_{C0} = 0, \quad V = 100, \quad RC = 10 \times 2 \times 10^{-3} = 20 \times 10^{-3} = 0.02, \quad T = \frac{1}{50} = 0.02 \text{ s}$$

Putting these values in (3),

$$v_C = 100\ (1 - e^{-50t})$$

At $t = T/2 = 0.01$ s,

$$v_C = 100(1 - e^{-50\times0.01}) = 39.35 \text{ V}$$

The expression of the capacitor current (or the load current) is given by

$$i_C = C\frac{dv_C}{dt} = \frac{V - v_{Co}}{R} e^{-t/(RC)} = \frac{100 - 0}{10} e^{-t/0.02} = 10e^{-50t} \quad \text{[from (3)]}$$

At t = 0+, i_C = 10 A; at t = 0.01, $i_C = 10\,e^{-0.5} = 6.065$ A. Therefore, the current decays exponentially from 10 A to 6.065 A in the first half-cycle. For the second half-cycle, v_C is given by

$$v_C = -100\,(1 - e^{-50t'}) + 39.35\ e^{-50t'}$$

where $t' = t - T/2 = t - 0.01$

At $t = 0.02$ s or $t' = 0.01$ s,

$$v_C = -100\,(1 - e^{-0.5}) + 39.35\ e^{-0.5} = -15.48 \text{ V}$$

For the second half-cycle,

$$i_C = \frac{-100 - v_{C(t=0.01)}}{10} e^{-50t'} = \frac{-100 - 39.35}{10} e^{-50t'} = -13.935\,e^{-50t'}$$

At t' = 0+, i_C = –13.935 A; at $t' = 0.01$, $i_C = -13.935\ e^{-0.5} = -8.425$ A. Therefore, the negative current decays exponentially from –13.935 A to –8.452 A in the second half-cycle. The waveforms of v_C and i_C for the first cycle are shown in Fig. 8.37b.

(a) From (8.12), the steady-state capacitor voltage for the positive half-cycle is given by

$$v_C(t) = 100\left(1 - \frac{2}{1 + e^{-0.01/0.02}} e^{-t/0.02}\right) = 100\,(1 - 1.245\,e^{-50t})$$

The expression for the load current is given by

$$i_C(t) = C\frac{dv_C}{dt} = 12.45\ e^{-50t}$$

For the negative half-cycle,

$$v_C(t') = -100\,(1 - 1.245\ e^{-50t'}), \qquad \text{where } t' = t - 0.01$$

and

$$i_C(t') = -12.45\ e^{-50t'}$$

At $t = 0$,

$$v_C = 100\,(1 - 1.245) = -24.5 \text{ V} \quad \text{and} \quad i_C = 12.45 \text{ A}$$

At $t = 0.01$ s,

$$v_C = 100\,(1 - 1.245\,e^{-0.5}) = 24.5 \text{ V} \quad \text{and} \quad i_C = 12.45\,e^{-0.5} = 7.55 \text{ A}$$

At $t' = 0$,

$$v_C = -100\,(1 - 1.245) = 24.5 \text{ V} \quad \text{and} \quad i_C = -12.45 \text{ A}$$

At $t' = 0.01$ s,

$$v_C = -100\,(1 - 1.245\,e^{-0.5}) = -24.5 \text{ V} \quad \text{and} \quad i_C = -12.45\ \ e^{-0.5} = -7.55 \text{ A}$$

The waveforms of v_C and i_C under steady-state condition are shown in Fig. 8.37c.

Example 8.4 The full-bridge inverter of Fig. 8.5 has a source voltage, $V = 220$ V. The inverter supplies an *RLC* load with $R = 5\ \Omega$, $L = 10$ mH and $C = 26\ \mu$F. The frequency of operation of inverter is 400 Hz. Calculate:

(a) the rms load current at fundamental frequency,
(b) the rms value of load current,
(c) the THD in the load current,
(d) the power output, and
(e) the average supply current.

Solution Given $V_L = 220$ V, $R = 5\ \Omega$, $L = 10$ mH, $C = 26\ \mu$F, $f = 400$ Hz,

The inductive reactance for the fundamental voltage,

$$X_L = 2\pi fL = 2 \times \pi \times 400 \times 10 \times 10^{-3} = 25.13\ \Omega$$

The capacitive reactance for the fundamental voltage,

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 400 \times 26 \times 10^{-6}} = 15.3\ \Omega$$

Impedance offered to nth harmonic component,

$$Z_n = \sqrt{R^2 + \left(nX_L - \frac{X_C}{n}\right)^2}$$

Putting different values of n, impedance offered to different harmonic components are

$$Z_1 = \sqrt{5^2 + (25.13 - 15.3)^2} = 11.03\ \Omega$$

$$Z_3 = \sqrt{25 + \left(3 \times 25.13 - \frac{15.3}{3}\right)^2} = 70.47\ \Omega$$

Similarly,

$$Z_5 = 122.69\ \Omega, \quad Z_7 = 173.79\ \Omega, \quad Z_9 = 224.52\ \Omega$$

From (8.22), the rms value of the nth harmonic component of the output voltage is given by

$$V_n = \frac{0.9V_L}{n} = \frac{0.9 \times 220}{n} = \frac{198}{n}$$

The rms value of the nth harmonic component of the current is given by

$$I_n = \frac{V_n}{Z_n} = \frac{198}{nZ_n} \tag{4}$$

(a) The rms value of the fundamental component of the load current

$$I_1 = \frac{198}{1 \times 11.03} = 17.95 \text{ A}$$

(b) Putting the values of n and Z_n in equation (4), rms values of the different harmonic components may be obtained as $I_3 = 0.94$ A, $I_5 = 0.32$ A, $I_7 = 0.16$ A, $I_9 = 0.1$ A, ...

The rms value of the load current

$$I = \sqrt{I_1^2 + I_3^2 + I_5^2 + I_7^2 + I_9^2 + \cdots}$$

$$= \sqrt{17.95^2 + 0.94^2 + 0.32^2 + 0.16^2 + 0.1^2 + \cdots}$$

$$= 17.98 \text{ A}$$

(c) THD in the load current

$$\text{THD}_i = \frac{\sqrt{I^2 - I_1^2}}{I_1} = \frac{\sqrt{17.98^2 - 17.95^2}}{17.95} = 0.0578 = 5.78\%$$

(d) The power output

$$P_o = I^2R = (17.98)^2 \times 5 = 1.616 \text{ kW}$$

(e) The average supply current

$$I_{av} = \frac{P_o}{V} = \frac{1616}{220} = 7.35 \text{ A}$$

Example 8.5 A single PWM inverter feeds an RL load with $R = 10\ \Omega$ and $L = 20$ mH. If the source voltage is 120 V, find out the total harmonic distortion in the load current. The width of each pulse is 120° and the output frequency is 50 Hz.

Solution From (8.31), the rms value of the nth harmonic component of the output voltage is given by

$$V_n = \frac{4V}{\sqrt{2}n\pi} \sin\frac{nW}{2}$$

Here $V = 120$ and $W = 2\pi/3$. Therefore,

$$V_n = \frac{4 \times 120}{\sqrt{2}\, n\pi} \sin\frac{n\pi}{3} = \frac{108.04}{n} \sin\frac{n\pi}{3}$$

The impedance offered to the nth harmonic current is given by

$$Z_n = \sqrt{R^2 + (n\omega L)^2} = \sqrt{10^2 + n^2(2\pi \times 50 \times 20 \times 10^{-3})^2} = \sqrt{100 + 39.478n^2}$$

The rms value of the nth harmonic current

$$I_n = \frac{V_n}{Z_n} = \frac{108.04}{n\sqrt{100 + 39.478n^2}} \sin\frac{n\pi}{3}$$

Putting different values of n, we get $I_1 = 7.922$ A, $I_3 = 0$, $I_5 = 0.5675$ A, $I_7 = 0.2963$ A, $I_9 = 0$, $I_{11} = 0.1218$ A, $I_{13} = 0.0814$ A. Then

$$\text{THD}_i = \frac{\sqrt{I_3^2 + I_5^2 + I_7^2 + I_9^2 + I_{11}^2 + I_{13}^2}}{I_1} = \frac{0.4323}{7.922} = 0.0545 = 5.45\%$$

Example 8.6 The output voltage of a uniform PWM inverter is shown in Fig. 8.38. Find out

(a) rms value of the output voltage,

(b) rms value of the fundamental component of the output voltage, and

(c) the total harmonic distortion.

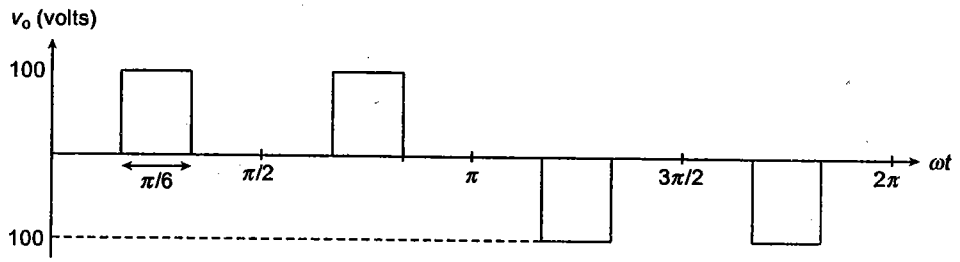


Figure 8.38 For example 8.6.

Solution (a) The rms value of output voltage

$$V_o = \left[\frac{100^2(\pi/6)}{(\pi/2)}\right]^{1/2} = 100\sqrt{\frac{1}{3}} = 57.735 \text{ V}$$

(b) The waveform possesses odd- and half-wave symmetry. Hence, only odd b-components will be present in the Fourier series, which are given by

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} v_o(t) \sin(n\omega t)\, d(\omega t) = \frac{4}{\pi}\left[\int_{30^\circ}^{60^\circ} 100 \sin(n\omega t)\, d(\omega t)\right]$$

and

$$b_1 = \frac{400}{\pi}\left[-\cos \omega t\right]_{30°}^{60°} = \frac{400}{\pi}(-\cos 60° + \cos 30°) = 46.604$$

The rms value of fundamental component

$$V_1 = \frac{46.604}{\sqrt{2}} = 32.953 \text{ V}$$

(c) $$\text{THD} = \frac{\sqrt{V_o^2 - V_1^2}}{V_1} = 1.4385 = 143.85\%$$

Example 8.7 A three-phase bridge inverter is fed from a 600 V dc source. The inverter is operated in 180° conduction mode and it is supplying a purely resistive, star-connected load with R = 15 Ω/phase. Determine

(a) the rms value of load current,

(b) the rms value of switch current,

(c) the power delivered to the load, and

(d) the average source current.

Solution (a) From (8.43), the rms value of the per-phase load voltage is given by

$$V_{ph} = \frac{\sqrt{2}}{3}V = \frac{\sqrt{2}}{3} \times 600 = 282.84 \text{ V}$$

Therefore, the rms value of load current per phase

$$I_{ph} = \frac{V_{ph}}{R} = \frac{282.84}{15} = 18.85 \text{ A}$$

(b) From (8.45), the rms value of current through switch

$$I_{\text{switch (rms)}} = \frac{V}{3R} = \frac{600}{3 \times 15} = 13.33 \text{ A}$$

(c) Power delivered to the load

$$P_L = 3\frac{V_{ph}^2}{R} = 3 \times \frac{282.84^2}{15} = 15999 \text{ W or } 16 \text{ kW}$$

(d) Power delivered by the source = $V_L I_{av} = P_L$, where, I_{av} is the average source current. Therefore,

$$I_{av} = \frac{P_L}{V_L} = \frac{15999}{600} = 26.66 \text{ A}$$

SUMMARY

1. Inverters convert dc voltage into single phase or three phase ac voltage.
2. In low and medium power inverters, gate commutated power semiconductor devices are used. For high power applications, thyristor based inverters are used.
3. Inverters may use half-bridge or full-bridge configurations. A half-bridge configuration requires a three-wired dc supply which is not necessary for a full-bridge configuration.
4. Square wave inverters provide fixed ac voltage with appreciable low frequency harmonics.
5. PWM inverters provide an adjustable ac voltage from a fixed dc voltage, with reduced harmonic content. Sinusoidal PWM technique is most effective in eliminating low frequency harmonics.
6. Three-phase inverters may use 120° conduction scheme or 180° conduction scheme. In 120° conduction scheme, short circuiting of dc source is avoided but the power semiconductor switches are poorly utilized.
7. Current source inverters provide short circuit protection and these are highly reliable.
8. McMurray inverter employs auxiliary current-commutation technique.
9. McMurray–Bedford inverter uses complementary voltage-commutation technique.
10. Frequency of an inverter may be controlled by controlling the conduction intervals of the inverter switches.
11. The output voltage of an inverter can be controlled by controlling the input dc voltage. However, the output voltage may be controlled most efficiently using PWM techniques.

REVIEW QUESTIONS AND PROBLEMS

1. Explain the principle of operation of an inverter.
2. How are inverters classified?
3. Compare the advantages and disadvantages of half-bridge and full-bridge inverters.
4. Explain the various performance parameters of an inverter.
5. What is the advantage of eliminating low-frequency harmonics from the output voltage of an inverter?
6. What are the different pulse-width modulation techniques used for inverters?
7. Compare the bipolar and unipolar switching schemes of a sinusoidal PWM inverter.
8. Explain 180° conduction scheme and 120° conduction scheme of a three-phase inverter and compare them.
9. Explain the working of a single-phase gate-commutation device based voltage source inverter.
10. Explain the working of a single-phase gate-commutation device based current source inverter.

11. What are the advantages and disadvantages of a current source inverter?

12. Explain the working of an auxiliary commutated inverter.

13. Explain the working of a complementary commutated inverter.

14. What are the different methods of voltage control of an inverter?

15. A single-phase, half-bridge inverter feeds a resistive load, $R = 5\ \Omega$. If the source voltage is 60 V, Determine:

(a) the rms value of the fundamental component of output voltage,
(b) the output power,
(c) the peak-off state voltage across each semiconductor switch,
(d) the lowest order harmonic and the corresponding harmonic factor, and
(e) the rms and average values of the current through semiconductor switches.

16. Repeat problem 15 for a single-phase, full-bridge inverter.

17. A single-phase, full-bridge inverter with the source voltage, $V = 240$ V feeds an *RL* load with $R = 10\ \Omega$ and $L = 0.1$ H. If the frequency of the output current is 50 Hz, determine:

(a) the instantaneous output current at the end of second cycle,
(b) the expression of steady-state output current for both the half cycles,
(c) THD for the load current, and
(d) the conduction intervals of each diode and each semiconductor switch, under steady-state condition.

18. The square-wave output voltage of a bridge inverter has a magnitude of 120 V and frequency of 50 Hz. The inverter is supplying an *RC* load with $R = 12\ \Omega$, C = 2.5 mF. Draw the waveforms of capacitor voltage and capacitor current: (a) for the first cycle and (b) under steady-state condition.

19. The square-wave voltage of Fig. 8.37(a), is applied to an inductance of 100 mH.

(a) Draw the waveform of load current for first cycle and for steady state, and
(b) repeat (a) for the case of an *RL* load with $R = 5\ \Omega$, $L = 1$ mH.

20. The full-bridge inverter of Fig. 8.5 has the source voltage, $V = 220$ V. The inverter supplies an *RLC* load with $R = 10\ \Omega$, $L = 30$ mH and $C = 100\ \mu$F. The frequency of operation of inverter is 50 Hz. Calculate:

(a) the rms load current at fundamental frequency,
(b) the rms value of load current,
(c) THD of the load current,
(d) the power output, and
(e) the average supply current.

21. A single PWM inverter with a source voltage of 120 V has to supply 1000 W to a purely resistive load of 10 Ω. Determine

(a) the width of output pulse,
(b) the fourier series expression of the output voltage, and
(c) average value of source current.

22. A single PWM full-bridge inverter with the source voltage, 240 V has to feed a purely resistive load of 10 Ω. The Pulse width is so selected that the third harmonic current is eliminated.

(a) Find out the output power and the average source current, and

(b) what should be the pulse width and the output power if the 5th harmonic component is to be eliminated?

23. A single PWM full-bridge inverter feeds an *RL* load with $R = 10\ \Omega$ and $L = 10$ mH. If the source voltage is 120 V, find out the total harmonic distortion in the output voltage and in the load current. The width of each pulse is 120° and the output frequency is 50 Hz.

24. Repeat problem 23 for $R = 10\ \Omega$ and $L = 40$ mH. Compare the results.

25. The output voltage of a uniform PWM inverter consists of three 120-V pulses per cycle, each of 30° duration. Find out:

(a) the rms value of output voltage,

(b) the rms value of fundamental component of output voltage, and

(c) the total harmonic distortion.

26. A three-phase bridge inverter is fed from a 480-V dc source. The inverter operates in 180° conduction mode and it supplies a purely resistive, star-connected load with $R = 10\ \Omega$/phase. Determine:

(a) the rms value of load current,

(b) the rms value of switch current,

(c) the power delivered to the load, and

(d) the average source current.

27. Repeat problem 26 in case the inverter is operated in 120° conduction mode.

28. A three-phase, full-bridge inverter with the source voltage of 220 V supplies a delta-connected purely resistive load ($R = 10\ \Omega$/phase). If the inverter is operated in 180° conduction mode, determine

(a) the rms value of per phase load current,

(b) the rms value of line current,

(c) the rms value of switch current,

(d) the power output, and

(e) the average source current.

29. Repeat problem 28 if the inverter is operated in 120° conduction mode.

9

Resonant Converters

9.1 INTRODUCTION

In case of switch-mode (or PWM) techniques used for dc-to-dc or dc-to-ac converters, the power semiconductor switches, during turn-on and turn-off processes, carry the entire load current. These switches are therefore, subjected to high-switching stresses and the switching power loss is significantly high. Moreover, the steep rise and snap of high current increases EMI due to large *di/dt* and *dv/dt*. To keep the switching losses low, fast or quick switching of devices is desirable.

A substantial increase in converter switching frequency minimizes the lower-order harmonics in PWM-type applications. It provides a higher current regulator bandwidth and reduces the size of reactive components and filter circuits. Moreover, the acoustic noise becomes insignificant above 18-kHz switching frequency. However, fast switching causes high *dv/dt* on output, which generates an interference due to capacitive coupling. Also, the diode reverse-recovery and snubber interaction cause high device stress under regeneration conditions. Therefore, either large SOA (higher device rating) is required or one has to compromise on reliability. Thus, in brief, both *di/dt* and *dv/dt* stresses on device increase.

If the operating frequency of the converter is increased to reduce its size and weight, the switching stress, losses in device and EMI increase linearly with the switching frequency. The current and the voltage trajectories of the device during turn-on and turn-off operation play very important role in the switching losses and stresses on the device. Since, in general, the switching turn-off time (t_{off}) is longer than the switching turn-on time (t_{on}), the former is more significant.

Figure 9.1 shows a typical switching circuit arrangement of the device (thyristor or RCT, BJT, MOSFET, IGBT, etc.) with a device-package fast-recovery diode (fabricated with device to reduce lead or connecting wire inductance and ease of connection) and snubber circuit. Figure 9.2 shows the trajectory of the device and corresponding power loss (P_d) in the device. It is evident that both device voltage (v_d) and device current (i_d) play very important role in the device switching loss (during the turn-off operation). Even in the presence of snubber circuits, the switching losses are significant.

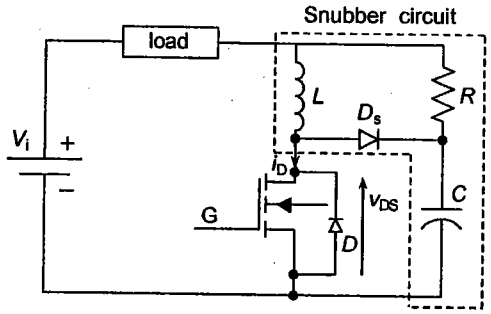
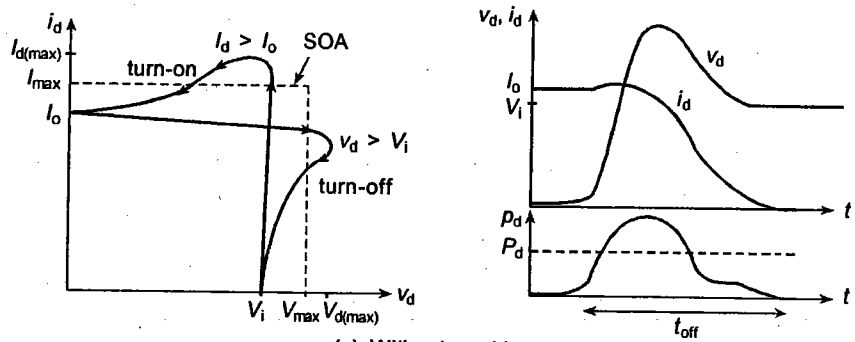
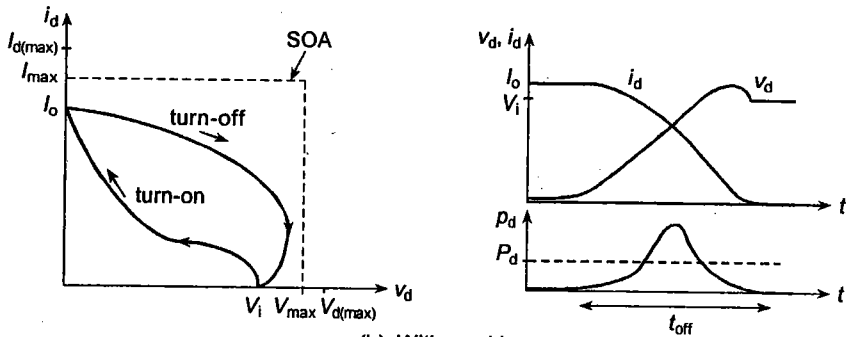


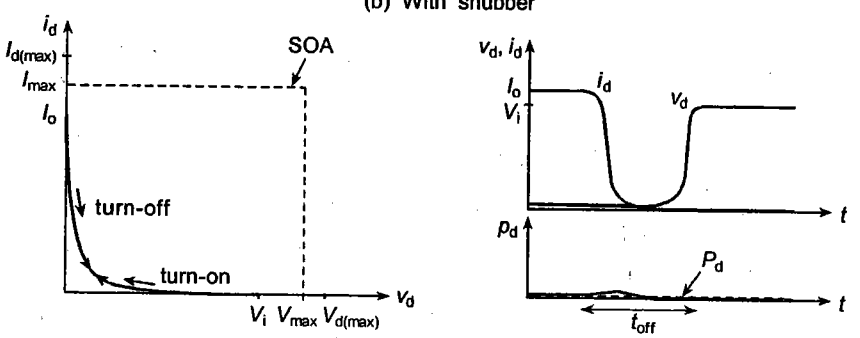
Figure 9.1 A typical switching circuit topology of a dc-dc switch mode converter (PWM control) with a snubber circuit.



(a) Without snubber



(b) With snubber



(c) With ZVS/ZCS

Figure 9.2 Trajectories of v_d, i_d and pd at different switching conditions.

To avoid these short-comings, resonant *LC* circuit is added in these converters. The current and/or voltage of an *LC* resonant circuit (series or parallel) undergo to a zero-level periodically. If the switches of the converters are turned on or turned off at zero voltage and/or zero current level, the switching losses, stress on devices, EMI generated, etc., reduce drastically (ideally, zero loss and zero stress). It is called *zero-voltage* switching (ZVS) or *zero-current switching* (ZCS), accordingly. Thus, size and weight of converters reduce and performance improves to a great extent. There are large numbers of circuit topologies of resonant converters.

The basic function of the switches in a resonant converter is to create a square-wave dc or ac waveform from the dc source and the resonating inductor and capacitor (*LC*) remove the unwanted harmonic components from the square-wave (Fig. 9.3). The *LC* resonant circuit is tuned to about the switching frequency of the converter. It removes the harmonics, not as a simple low-pass filter, rather due to ideally undamped or highly under-damped oscillation of the current and/or voltage.

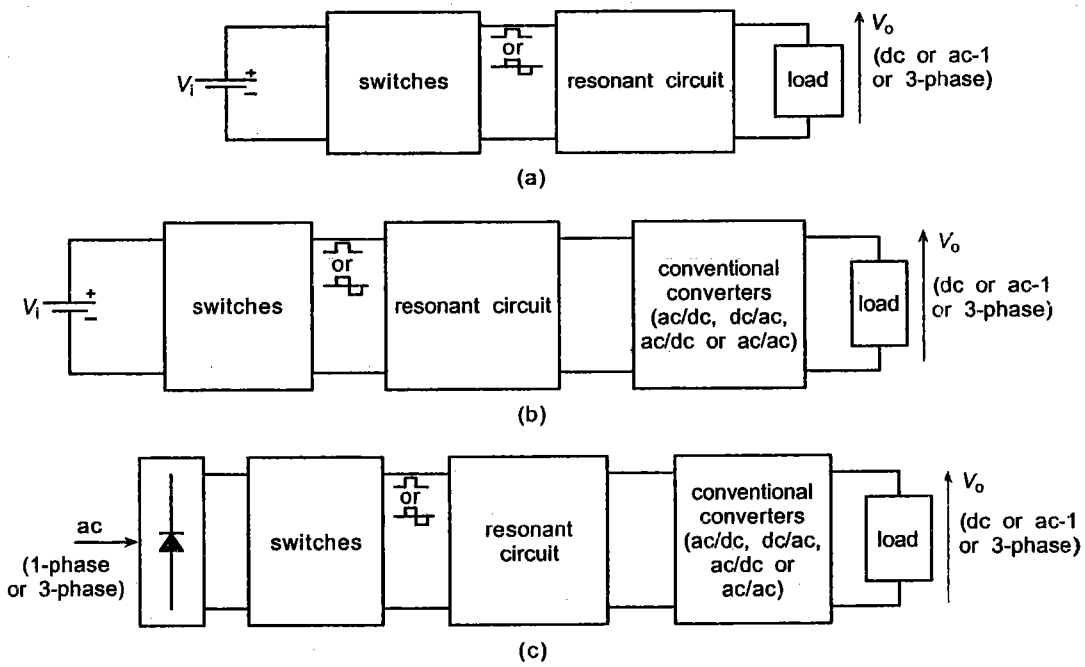


Figure 9.3 Block diagrams showing principles of different resonant converters.

In case of undamped condition ($R = 0$), the waveform is purely sinusoidal. Even in the presence of R (for a highly under-damped circuit), in the first half-cycle after every switching, the current (or voltage across R) waveform is almost sinusoidal (similar to that of *LC* circuit). However, it costs higher voltage stress on devices and higher on-state losses in devices (as the resonant current through devices increases).

There are two methods employed in resonant converters. First, the switch generates a square wave of voltage that is applied to a series *LC* circuit. It is called a *series-resonant* converter. Second, the switch generates a square wave of current that is applied to a parallel *LC* circuit. It is

called a *parallel-resonant* converter. The output of these converters are supplied to the load or maneuvered further for the desired output, e.g. dc-dc, dc-ac or ac-ac conversion using conventional converters, as shown in Fig. 9.3.

9.2 PRINCIPLE OF RESONANT CONVERTER CIRCUITS

Both series and parallel *LC* resonant circuits are used in resonant converters. These are discussed here separately.

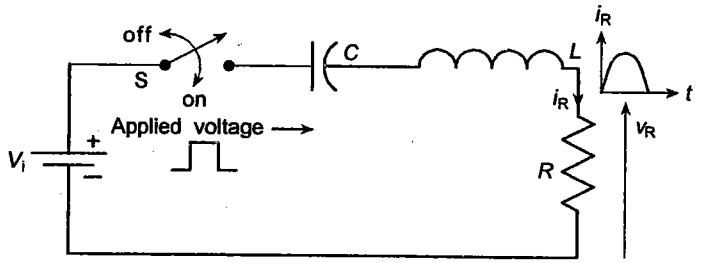
9.2.1 Series Resonant Circuits

In this case, the load resistance is in series with the *LC* resonating circuit. The reactance of the load (if any) is considered to be a part of *L* and/or *C*. As discussed in the previous section, it is basically a square-wave that is applied to the resonant circuit to generate sinusoidal voltage and/or current wave. The square wave can therefore be considered to be a step input during the turn-on period, as shown in Fig. 9.4a. The voltage equation is given by

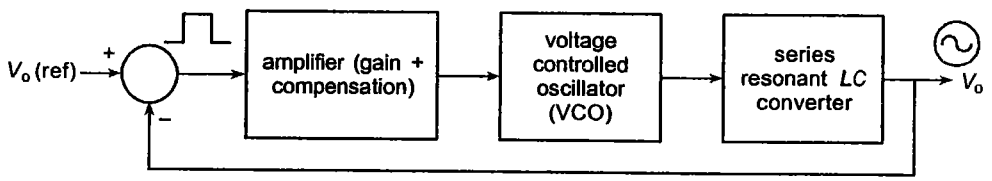
$$Ri + L\frac{di}{dt} + \frac{1}{C}\int i\,dt = 0 \tag{9.1}$$

The solution for zero initial condition (see Section A1, Fig. A4 in Appendix) is given by

$$i = \frac{V_i}{\omega_0 L}\exp(-\xi\omega_0 t)\sin\omega_r t = \frac{V}{\omega_0 L}e^{-\alpha t}\sin\omega_r t \tag{9.2}$$

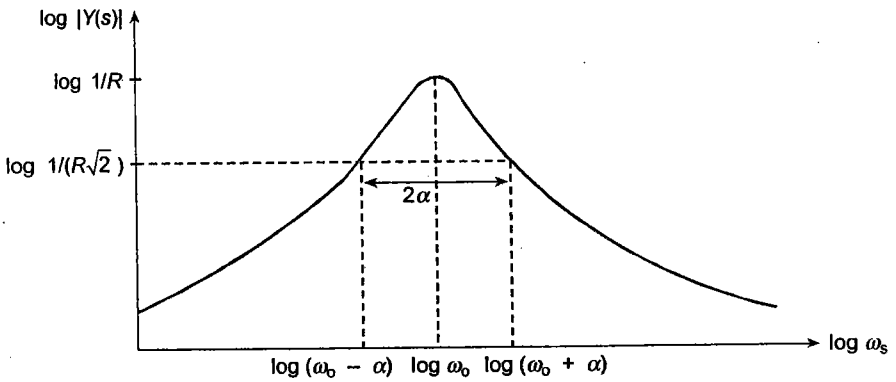


(a) Switching of an *RLC* series circuit

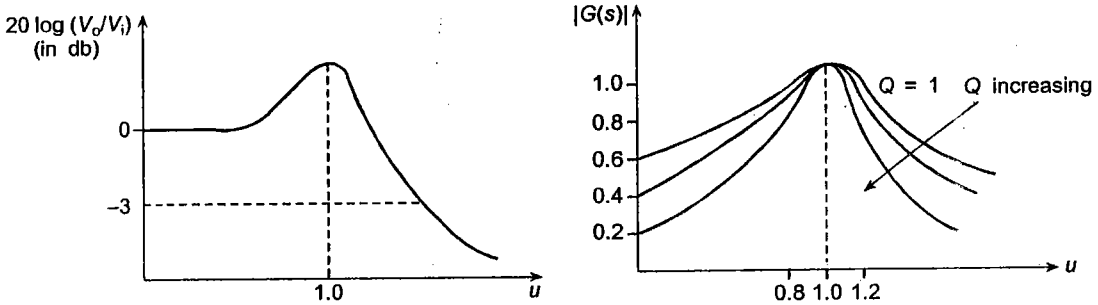


(b) Control scheme of series *RLC* resonant converters

Figure 9.4 (*Cont.*)



(c) Admittance variation of an *RLC* series circuit



(d) Gain variation of an *RLC* series circuit

Figure 9.4 Characteristics of a series *RLC* resonant converter.

where

$$\xi\omega_o = \alpha = \frac{R}{2L}, \quad \omega_o = \frac{1}{\sqrt{LC}}, \quad \omega_r = \sqrt{\frac{1}{LC} - \frac{RL}{2L}}, \quad \xi = \frac{R}{2}\sqrt{\frac{C}{L}}$$

and

$$v_C = V + (V_o - V_i)\, e^{-\alpha t}\left(\frac{\alpha}{\omega_r}\sin\omega_r t + \cos\omega_r t\right)$$

$$= V + (V_o - V_i)\, e^{-\alpha t}\left\{\left[1 + \left(\frac{\alpha}{\omega_r}\right)^2\right]^{1/2}\cos(\omega_r t + \theta)\right\} \tag{9.3}$$

where ω_o and ω_r are undamped (resonant) and damped angular frequency of oscillation, respectively; z-damping ratio, and $\theta = \tan^{-1}(\alpha/\omega_r)$. If $R = 0$, then it becomes an *LC* resonating circuit with undamped oscillation. Then, ξ becomes zero and $\omega_r = \omega_o$. Moreover, to determine the effectiveness of the *LC* resonating circuit, frequency domain analysis is important. The impedance and the admittance of the series *RLC* in frequency domain is given by

$$Z(s) = R + sL + \frac{1}{sC}$$

and

$$Y(s) = \left(R + sL + \frac{1}{sC}\right)^{-1} = \frac{2\alpha s}{s^2 + 2\alpha s + \omega_o^2}\frac{1}{R} \tag{9.4}$$

where the roots are $s_{1,2} = -\alpha \pm j\omega_r$ and

$$\omega_r = \sqrt{\omega_o^2 - \alpha^2} = \omega_o\sqrt{1 - \xi^2}$$

At resonance, $s = j\omega_o$, which gives

$$Y(s) = \frac{1}{R} \tag{9.5}$$

When admittance, $Y(s) = \{1/[R(\sqrt{2})]\}$, it is called *half-power point* or 3dB point. The ratio $\omega_o/(2\alpha)$ is called *quality factor*, Q of the filter. The voltage stress on the C or L depends upon Q. For example, when the switches are operated at resonance frequency, the switching frequency, $f_s = f_o$ (or $\omega_s = \omega_o$). The voltage drop on capacitor at the resonance frequency ($\omega_s = \omega_o$) is given by

$$\left|\frac{V_C}{V_i}\right|_{\omega_s=\omega_o} = \left[\frac{C_s}{sL + R + (1/C_s)}\right]_{\omega_s=\omega_o} = \frac{\omega_o}{2\alpha}$$

or

$$|V_C|_{\omega_s=\omega_o} = QV_i \tag{9.6}$$

As the sharpness of the curve increases (hence Q) for the effectiveness of the filter at the desired ω_s, $|V_C|$ also increases Q times of V_i. This is the most serious drawback of resonant converters, especially when Q is high and the load resistance (R) is small. Moreover, higher voltage stress demands devices of higher voltage rating. Since ξ also becomes small, the effect of damping reduces drastically. The first oscillation after switching, in both undamped LC circuit ($\xi = 0$) and RLC under-damped circuit ($\xi < 1$ and close to zero), do not vary significantly. Therefore, instead of a series RLC circuit, it can be analyzed as a series LC circuit, whose analysis is easy. The converter acts in both discontinuous conduction and continuous conduction modes for the switching frequency, $f_s < f_o/2$ and $f_o/2 < f_s < f_o$, respectively. However, when $f_s < f_o$, the switches turn-on at zero current and zero voltage.

The voltage gain of the RLC series circuit in the switching frequency domain is given by

$$G(s) = \frac{V_o(j\omega_s)}{V_i(j\omega_s)} = \frac{R}{R + j\omega_s L - (j/\omega_s C)}$$

$$= \frac{1}{1 + jQ[(\omega_s/\omega_o) - (\omega_o/\omega_s)]} \tag{9.7}$$

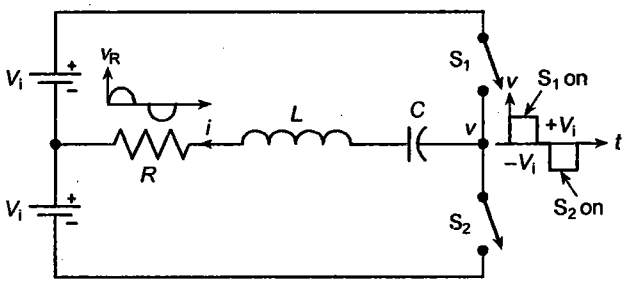
and

$$|G(s)| = \left\{\frac{1}{1 + Q^2[u - (1/u)]^2}\right\}^{1/2}, \qquad \text{where } u = \frac{\omega_s}{\omega_o} \tag{9.8}$$

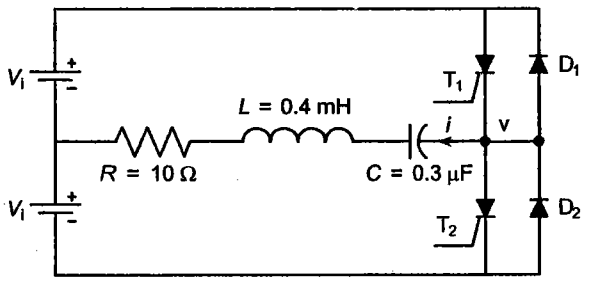
Since these converters are often switched at a variable frequency condition, the impedance of *RLC* series circuit varies and depends upon the switching frequency. It becomes minimum at ω_0. A term, quality factor (Q) is defined to measure the frequency sensitiveness of the impedance. It will be seen later that the voltage drop (high voltage stress on L and C) also increases with Q. The quality factor for a series *RLC* circuit is given by

$$Q_s = \frac{\omega_0}{2\alpha} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} \tag{9.9}$$

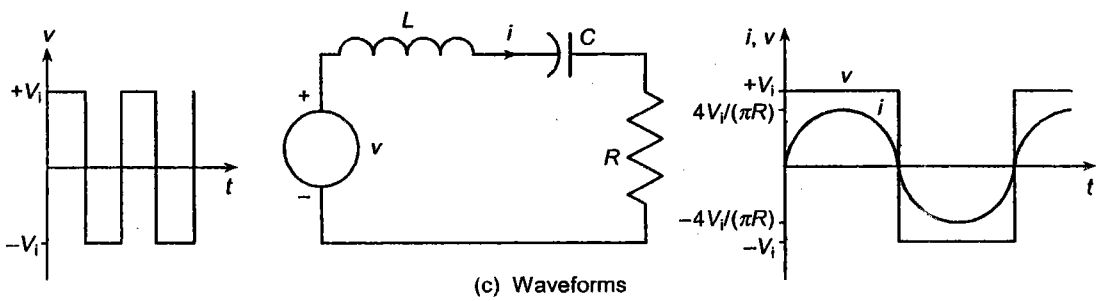
The switching is often done at off-resonance condition and the switching angular frequency, $\omega_s \neq \omega_0$. When $\omega_s < \omega_0$, $X_C > X_L$, the capacitive reactance dominates and the load current tends to lead. Similarly, it tries to lag when $\omega_s > \omega_0$ and $x_L > x_C$). The zero-crossing of the load current and fundamental voltage do not coincide. Figure 9.5 shows thyristor (SCR) based practical series resonant circuits.



(a) Circuit topology



(b) A practical circuit



(c) Waveforms

Figure 9.5 Series *RLC* resonant converters.

DETERMINATION OF L AND C

At the resonant frequency, the impedance of inductor and capacitor exactly cancels each other and the admittance becomes equal to $1/R$. The rms value of fundamental component (sinusoidal) of the square wave (load voltage) is $(2\sqrt{2}\ V/\pi)$. The load or the input current is purely sinusoidal (ideally) which is given by

$$i(t) = \frac{4V}{\pi R} \sin \omega_o t \tag{9.10}$$

For any voltage source, the voltage drop across R is largest at resonance frequency. Also, it is evident from Fig. 9.4d, the load or output voltage becomes higher than the input voltage at $\omega_s = \omega_o$.

Example 9.1 A series *LC* resonant converter is operating at 20 kHz with 10-Ω load and 100-V peak (square wave) voltage. Find the values of L and C: (i) the output power is controllable up to 25% of the maximum output and (ii) the frequency control is restricted to 20% below ω_o. Also, find the maximum voltage stress on L and C, and their maximum energy storage capacity.

Solution A simple *RLC* series resonant converter is shown in Fig. 9.5, where S_1 and S_2 are power semiconductor switching devices (e.g. SCR, MOSFET, IGBT, etc). The maximum value (or peak) of current is given by

$$I_{max} = \frac{V_{max}}{R} = \frac{100}{10} = 10 \text{ A} \quad \text{and} \quad \omega_o = 2\pi f_o = 40\pi \times 10^3 \text{ rad/s}$$

At resonance condition, maximum current flows. The maximum power output is given by

$$P_{max} = I^2R = \left(\frac{I_{max}}{\sqrt{2}}\right)^2 R = \left(\frac{100}{2}\right) \times 10 = 500 \text{ W}$$

Also, the peak or maximum value of the sinusoidal voltage is

$$V_{max} = \frac{4V_i}{\pi} = 100 \text{ V}$$

Which gives the input dc voltage (fundamental), $V_i = 78.54$ V. To reduce the power output to 1/4 (or 25%), the effective impedance increases to twice and admittance reduces to a half. Thus the current reduces to a half to reduce power to 1/4 (as $P = I^2R$). Since $Q_s = \omega_o/(2\alpha)$, from (9.4) the admittance is given by

$$Y(s) = \frac{1}{R} \frac{2\alpha s}{s^2 + 2\alpha s + \omega_o^2}$$

$$= \frac{1}{R} \frac{(1/Q)(s/\omega_o)}{(s/\omega_o)^2 + (1/Q_s)(s/\omega_o) + 1}$$

$$= \frac{1}{R} \frac{1}{1 + Q_s(s/\omega_o) + Q_s/(s/\omega_o)}$$

Since the frequency reduces to $0.8\omega_o$, the angular switching frequency, $\omega_s = 0.8\omega_o$, $s = j0.8\omega_o$, and $f_s = 0.8f_o = 0.8 \times 20 = 16$ kHz. The admittance at this condition is given by

$$Y(s = j0.8\omega_o) = \frac{1}{R}\frac{1}{1 + jQ_s[0.8 - (1/0.8)]}$$

The effective value is given by

$$|Y(s = j0.8\omega_o)| = \frac{1}{R\sqrt{1 + Q_s^2[0.8 - (1/0.8)]^2}} = \frac{1}{R\sqrt{1 + 0.2Q_s^2}}$$

Also, at this condition, the impedance is $2R$ and admittance is $1/(2R)$. Therefore, equating with the above equation, it gives, $Q_s = 3.87$. Also, $Q_s = \omega_o L/R$, which gives

$$L = \frac{QR}{2\pi f_o} = \frac{3.87 \times 10}{40\pi \times 10^3} = 0.308 \text{ mH}$$

Since, $\omega_o = 1/\sqrt{(LC)}$, which gives

$$C = \frac{1}{L\omega_o^2} = \frac{1}{0.308 \times 10^{-3}(40\pi \times 10^3)^2} = 0.2 \text{ μF}$$

The maximum voltage appears across the capacitor and inductor at resonance condition depends upon Q (v_L or v_C becomes higher than the input voltage, V_i).

$$V_{C(max)} = I_{max}\frac{1}{\omega_o C} = I_{max}Q_s R = 10 \times 3.87 \times 10 = 387 \text{ V}$$

$$V_{L(max)} = \omega_o L I_{max} = Q_s R I_{max} = 3.87 \times 10 \times 10 = 387 \text{ V}$$

Also, the maximum energy stored in inductor (E_L) or capacitor (E_C), at the resonance condition, is given by

$$E_C = E_L = \frac{1}{2}L\left(\frac{I_{max}}{\sqrt{2}}\right)^2 = \frac{1}{2}(0.308 \times 10^{-3})\left(\frac{100}{2}\right) = 7.7 \text{ mJ}$$

9.2.2 Parallel Resonant Circuits

It is dual of the voltage source *RLC* converter as discussed in the previous section. At the resonance condition, the impedance looks like purely resistive to the fundamental component of I_o (Fig. 9.6). The impedance becomes maximum at the switching frequency, $\omega_s = \omega_o$ and the load voltage waveform becomes almost sinusoidal, i.e. ($v_R = v_C$) (see Section A1, Fig. A5 in Appendix). The parallel *LC* network offers infinite reactance or impedance at the resonance condition. Also, v_R is in phase with i. The frequency sensitiveness of the impedance is measured by the quality factor of a parallel circuit, which is given by

$$Q_p = \omega_o RC = \frac{R}{\omega_o L} \tag{9.11}$$

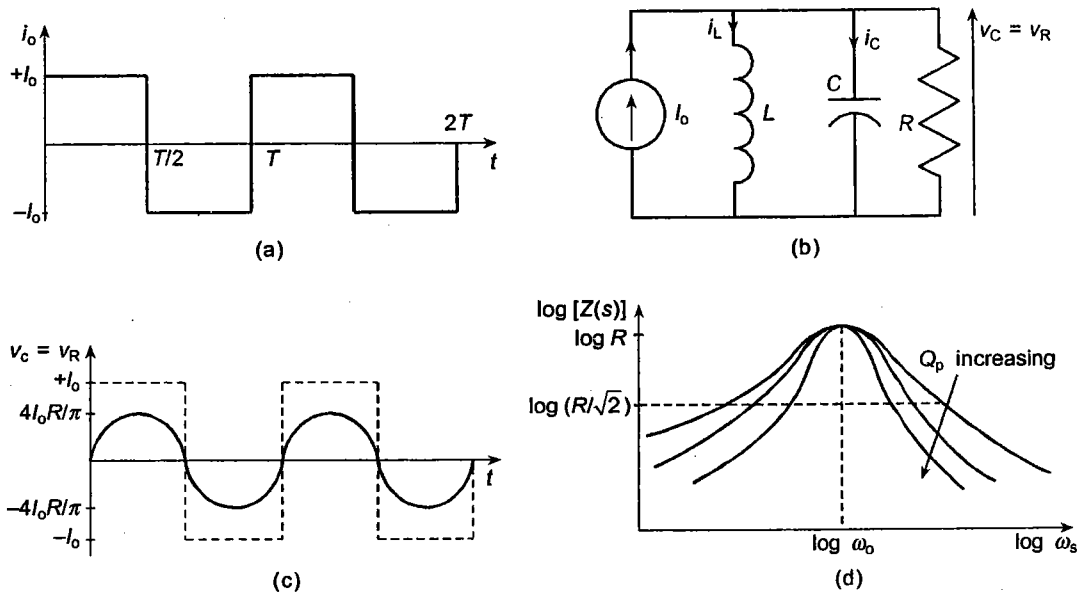


Figure 9.6 Characteristics of a parallel *RLC* circuit based converter.

The total impedance is given by

$$Z(s) = R\frac{s/(Q\omega_o)}{1 + \frac{s^2}{\omega_o^2} + \frac{s}{Q\omega_o}} \tag{9.12}$$

It is evident from Fig. 9.6d, $Z(s)$ varies with the switching frequency (ω_s) hence the power output of the load. For $\omega_s < \omega_o$, the inductive reactance is less than the capacitive reactance. Therefore, i_L dominates over i_C and the parallel *LC* circuit behaves as an equivalent inductor in parallel with the load resistance, R. Similarly for $\omega_s > \omega_o$, the circuit behaves as an equivalent capacitor in parallel with R. The gain of the parallel *RLC* circuit is given by

$$G(s) = \frac{\frac{R/j\omega C}{R + (1/j\omega C)}}{j\omega L + \frac{R/j\omega C}{R + (1/j\omega C)}} \tag{9.13}$$

$$= \frac{1}{1 - \omega^2 LC + (j\omega L/R)}$$

$$= \frac{1}{1 - \left(\frac{\omega}{\omega_o}\right)^2 + \frac{j(\omega/\omega_o)}{Q_p}}$$

or

$$|G(s)| = \frac{1}{\sqrt{(1-u^2)^2 + (u/Q_p)^2}} \tag{9.14}$$

Also, $|G(s)|_{max} = Q_p$, appears at $u = 1$ or $\omega_s = \omega_o$.

9.2.3 Parallel-loaded Resonant LC Converters

The operating principle is same as that of the series loaded-resonant converters. However, the capacitor voltage of the *LC* converter appears across the load (Fig. 9.7). A simple series *LC* resonant converter operates in buck mode only and the output voltage can be increased (near $f_s = f_o$) or decreased. It acts as a voltage source and several independent isolated dc outputs are possible.

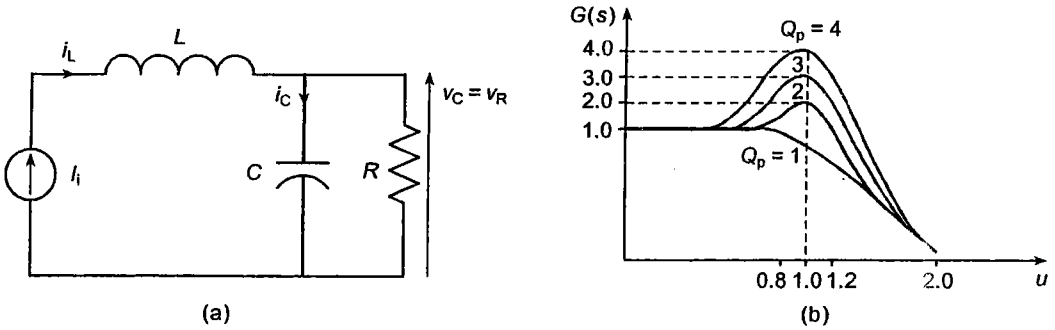


Figure 9.7 A parallel loaded *LC* resonant converter.

9.3 CLASSIFICATION OF RESONANT CONVERTERS

There are large number of circuit topologies for PWM based conventional dc-to-dc and resonant converters (see Fig. A14 and A15 of Appendix). These converters are versatile and capable of converting dc-to-dc, dc-to-ac, ac-to-dc and ac-to-ac. The resonant converters can be categorized as follows:

1. Self-commutating or load-resonating converters
2. Resonating switch ZVS/ZCS converters
3. Resonating dc link converters
4. Resonating ac link converters.

9.3.1 Self-commutating or Load Resonating Converters

In this case, both series and parallel *LC* resonating circuits are used and the oscillating voltage is allowed to appear across the load (or current to flow through the load). The switching frequency

(ω_s) is controlled around ω_0 to control the power input. Thus the circuit impedance varies and power output decreases at off-resonance conditions. There are several types of self- or load-resonating converters, used in both dc-to-dc and dc-to-ac converters. The series and parallel load resonating converters can be further classified as

(a) Series/parallel resonant converters with unidirectional switches
(b) series/parallel resonant converters with bidirectional switches.

Moreover, they may be used as a converter-rectifier (dc-to-dc converter) as well as an inverter (dc-to-ac converter).

SERIES RESONATING CONVERTERS WITH UNIDIRECTIONAL SWITCHES

The load (R) with resonating LC parameters forms series RLC under-damped circuit (Fig. 9.8). Analysis of such circuits is discussed in Section A6 of Appendix. When T_1 is triggered with an initial voltage on the capacitor, $v_C = V_{C2}$ (upper plate negative), a current i_1 flows. The current is almost sinusoidal (as damping factor is small), which is given by

$$i_1 = \frac{V_i - (-V_{C2})}{\omega_r L} e^{-at} \sin \omega_r t \tag{9.15}$$

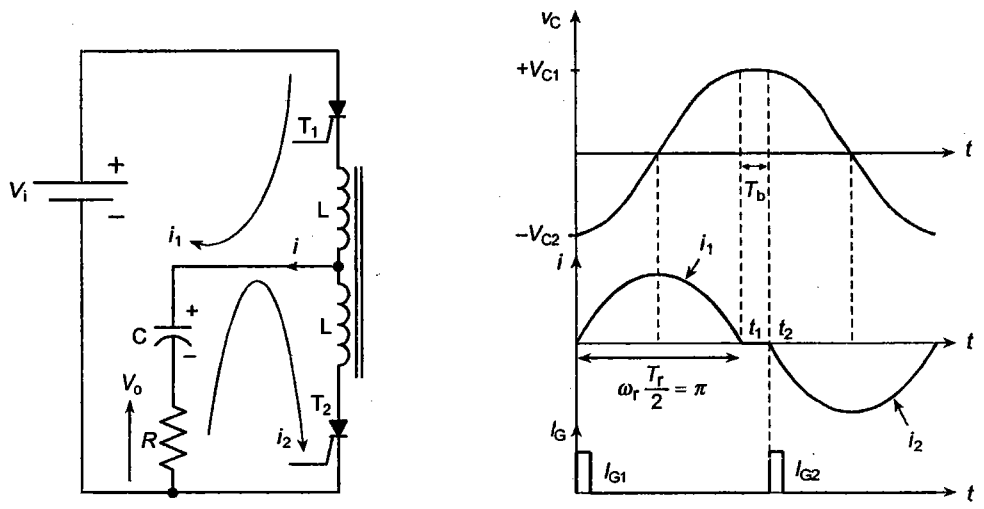


Figure 9.8 Series resonant inverter.

The oscillating current flows only during the first half-cycle and thereafter commutation of SCR takes place (anode current reaches to holding current level). An idle period, called the *blanking period* (T_b), is necessary between the conduction periods of two SCR. The damping exponential term (e^{-at}) does not dominate in the first half cycle of switching and therefore the current is almost sinusoidal in the first half-cycle. The damping term can be easily neglected which gives

$$i_1(t) = \frac{V_i + V_{C2}}{\omega_r L} \sin \omega_r t \tag{9.16}$$

The capacitor voltage is given by

$$v_C = \frac{1}{C}\int i_1\,dt = -\frac{V_i + V_{C2}}{\omega_r L}\cos\omega_r t - V_{C2}$$

At the end of the half-cycle,

$$t = t_1, \qquad \omega_r t_1 = \omega_r \frac{T_r}{2} = \pi, \qquad v_C = V_{C1}$$

Therefore,

$$V_{C1} = \frac{V_i + V_{C2}}{LC} + V_{C2} \tag{9.17}$$

When the thyristor T_2 is triggered, the capacitor discharges through the *RLC* circuit. Let the time reference shifts to this condition, i.e. $t = t_2$. The voltage equation is given by

$$Ri_2 + L\frac{di_2}{dt} + \frac{1}{C}\int i_2\,dt = 0 \tag{9.18}$$

The current response is given by

$$i_2 = \frac{V_{C1}}{\omega_r L}e^{-at}\sin\omega_r t \cong \frac{V_{C1}}{\omega_r L}\sin\omega_r t \tag{9.19}$$

and

$$V_{C2} = \frac{V_{C1}}{LC} + V_{C1} \tag{9.20}$$

From (9.17) and (9.20), we get

$$V_{C1} = -V_i - V_{C2} \tag{9.21}$$

A blanking period $(t_2 - t_1)$ is required for thyristors to avoid conduction overlap. Otherwise, it may cause a short-circuit condition due to simultaneous conduction of both thyristors. Normally, the blanking period varies from 12 μs to 25 μs depending upon the turn-off period, t_q of an SCR (inverter grade). Therefore, the operating frequency of such converters is restricted up to 10 kHz.

Example 9.2 A thyristor based resonant *RLC* inverter has following parameters: R = 1Ω, L = 0.1 mH, C = 10 μF, t_q =12 μs. Find the maximum switching frequency for non-overlap operation of the inverter.

Solution The angular frequency,

$$\omega_r = \left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)^{1/2} = \left(\frac{10^{12}}{100\times 10} - \frac{10^8}{4}\right)^{1/2} = 31.23 \text{ k-rad/s}$$

Then f_r = 4.97 kHz and T_r = 0.201 ms. The thyristors turn-off twice in a cycle. The minimum switching period is given by

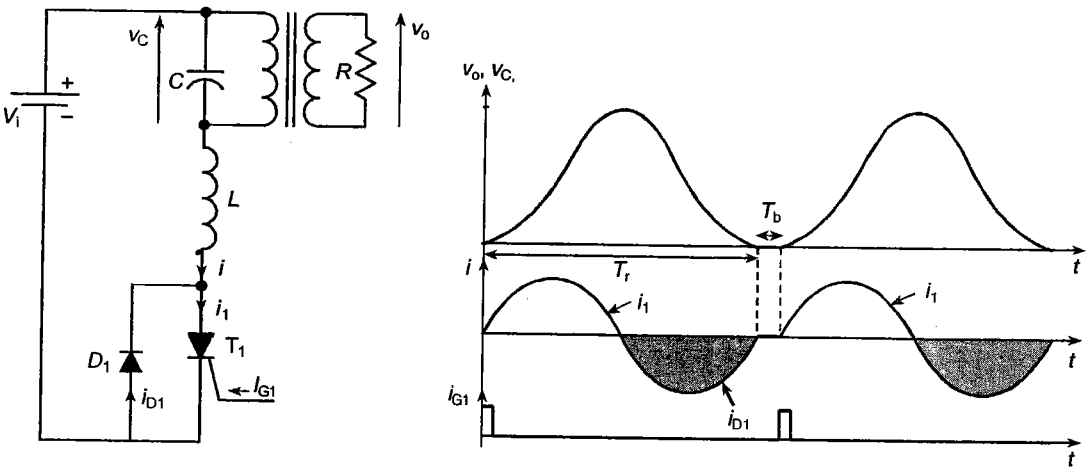
$$T_r + 2t_q = 0.201 + 2 \times 0.012 = 0.225 \text{ ms}$$

Therefore, the absolute maximum switching frequency for this converter is given by

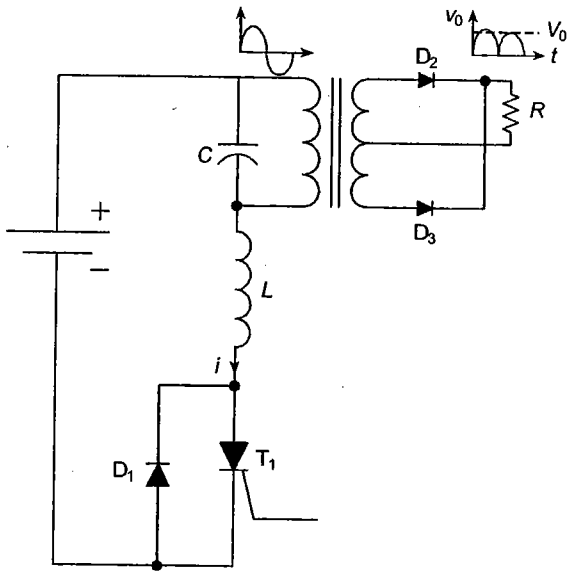
$$f_{s(max)} = \frac{1}{T_r + 2t_q} = \frac{1}{0.201 + 0.024} = 4.44 \text{ kHz}$$

Parallel Loaded Resonant Converters with Bidirectional Switches

In this case the oscillating current is allowed to complete one cycle (Fig. 9.9). Therefore, the capacitor voltage increases from zero and it reduces back to zero at the end of each time-period of the oscillation ($T_r = 2\pi/\omega_r$). When T_1 is triggered with a gate signal, the oscillating current starts flowing ($i_1 = i_A$) and the commutation of SCR takes place when the current tries to reach almost zero



(a) Inverter mode

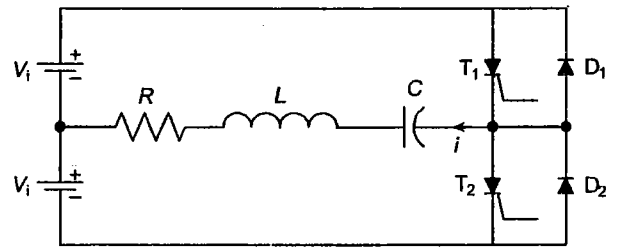


(b) Rectifier mode

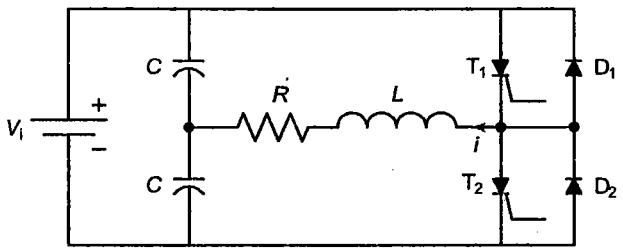
Figure 9.9 A series LC-parallel load resonant converter circuit.

level (holding current level). Thereafter, the direction of current reverses and the diode, D_1 conducts, capacitor gets discharged completely at the end of each time period. At the end of conduction of i_1, since the reversing current ($i = i_{D1}$) immediately finds another path (through D_1), it does not force a negative current through T_1. Therefore, the reverse voltage across T_1 due to conducting D_1 is small ($\cong$ 1V). Any inductance in the path of diode (e.g. connecting wire or lead) may further reduce the voltage drop across the SCR. Therefore, it should be avoided for the successful commutation of SCR. Normally, the reverse-conducting thyristor (RCT), where an asymmetric SCR and fast-recovery diode are fabricated together, is best for series resonant converters. Here, the blanking period is not necessary and T_1 can be triggered immediately at $t = T$. (as T_1 cannot conduct while D_1 is still conducting because the cathode of SCR is almost at its anode potential). The output voltage may be rectified using conventional rectifier circuit to generate a dc output voltage. Figure 9.9b shows a mid-point uncontrolled converter circuit used for this purpose.

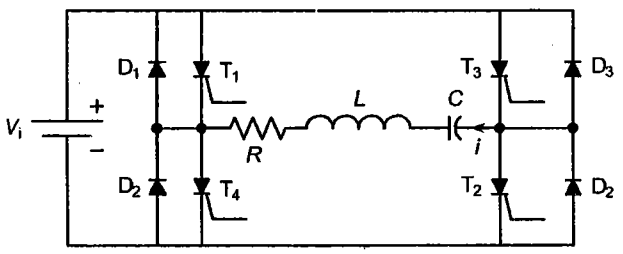
Figure 9.10 shows the other bridge circuit configurations. These converters may operate both in non-overlap and overlap modes (Fig. 9.11). In non-overlap mode, the oscillation of current through the diode is allowed to complete and then the thyristor or switch is triggered. In case of overlap mode, a thyristor is triggered before the current through the diode ceases to zero. In this



(a) Half-bridge with two dc sources

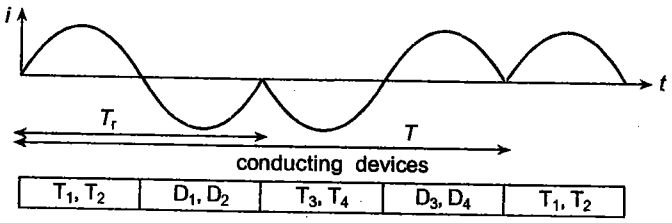


(b) Half-bridge with one dc source

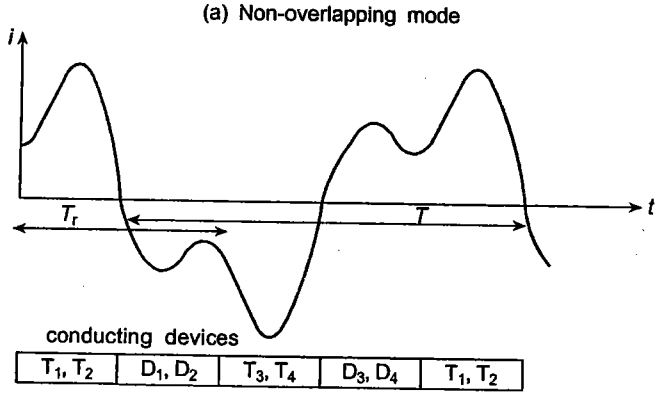


(c) Full-bridge

Figure 9.10 Half and full-bridge configurations of series resonant converters.



(a) Non-overlapping mode

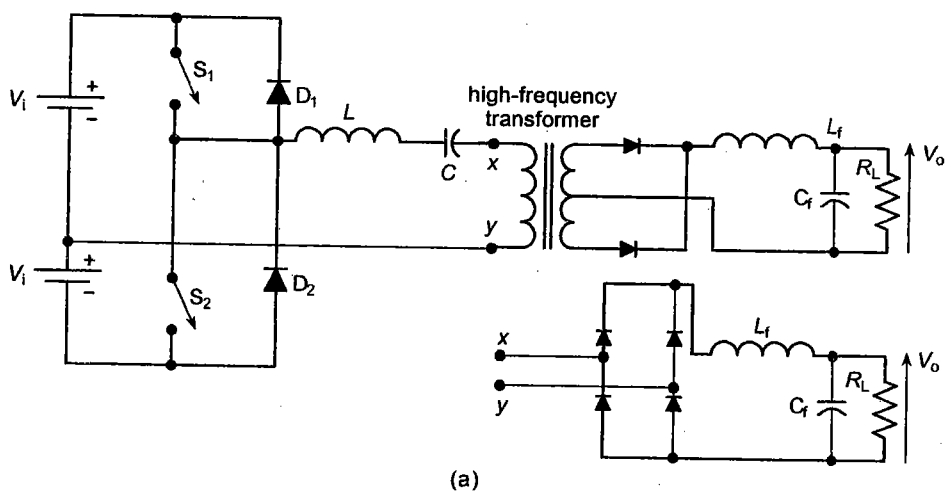


(b) Overlapping mode

Figure 9.11 Waveforms of full-bridge configrations.

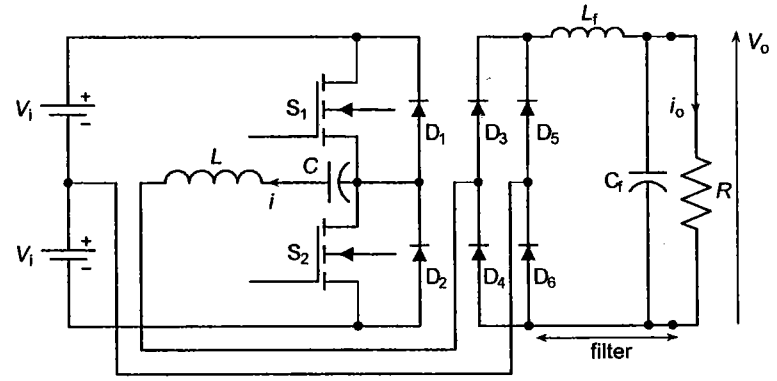
case due to overlapping, the time period of one complete cycle (T) is less than that at the resonance condition. Therefore, the operating frequency of series resonant inverter and its output power increase. The frequency and the power density (power handling capability) of the converter can be increased by replacing the SCR by BJT, MOSFET or IGBT.

If the load is connected through a diode bridge and a filter circuit, the above mentioned converters become series resonant dc-to-dc converters, as shown in Fig. 9.12. It is

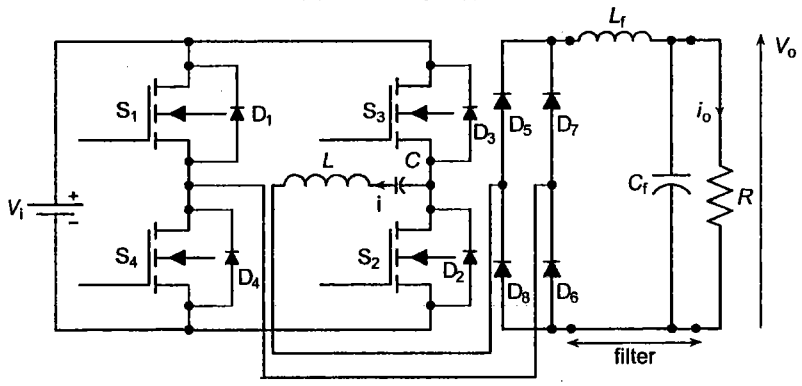


(a)

Figure 9.12 (*Cont.*)



(b) Half-bridge type



(c) Full-bridge type

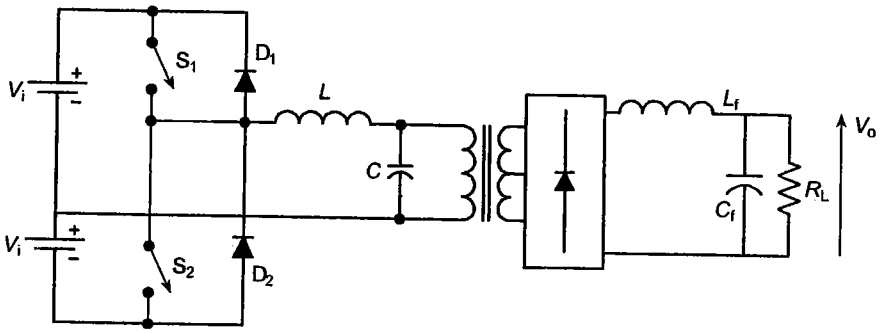
Figure 9.12 Series resonant dc-to-dc converters.

evident that the load resistance appears in series with the *LC* resonating circuit (through the diode bridge). For an isolated load, a centre-tapped transformer with two diodes is used, instead of a diode bridge. The L-section filter easily removes ripple due to high switching frequency. At dc side, normally electrolytic capacitors are used due to its high capacitance density (small size). Thus the output voltage (V_o) is assumed to be constant. For the need of high power density, an SCR is replaced by a fast switching device (e.g. MOSFET). Neglecting the voltage drop across L_f, the voltage drop across *LC* is $\pm(V_i - V_o)$.

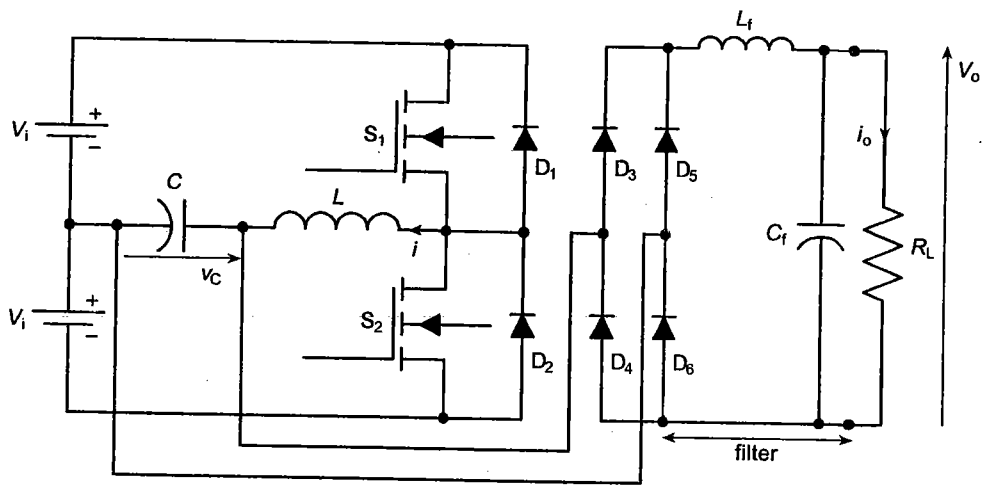
Figure 9.13 shows different parallel-loaded bidirectional circuit topologies for a resonant converter. The operating principle is same as the previous cases except that the load appears across the capacitor.

Class-E, LC Resonant Converters

It is a highly efficient, low-EMI, single-switch, resonant converter. Normally the efficiency of converters are above 95%. Since a large inductor is required, it is used for low-power applications (less than 100W), e.g. in high-frequency electronic ballast circuit for compact fluorescent lamps (CFL). However, it generates a high-peak voltage and current associated with the switch and large voltage and current through the resonant LC parameters. It is operated at a frequency slightly



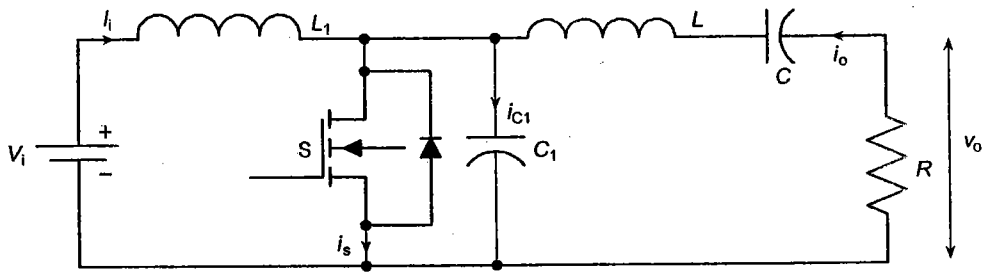
(a) Circuit topology for isolated load



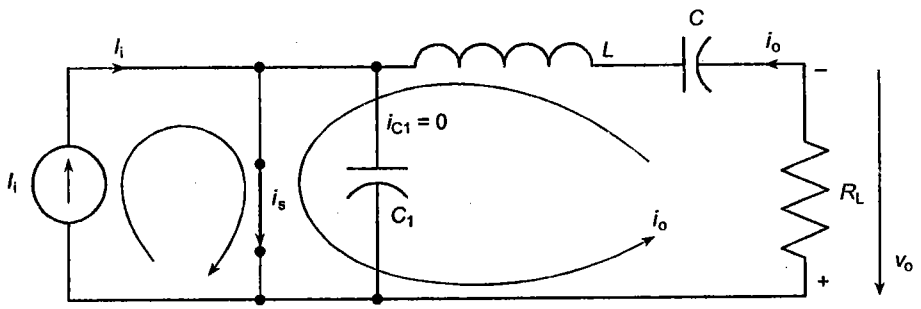
(b) A MOSFET based converter for non-isolated loads

Figure 9.13 Parallel-loaded resonant half-bridge type dc-to-dc converters.

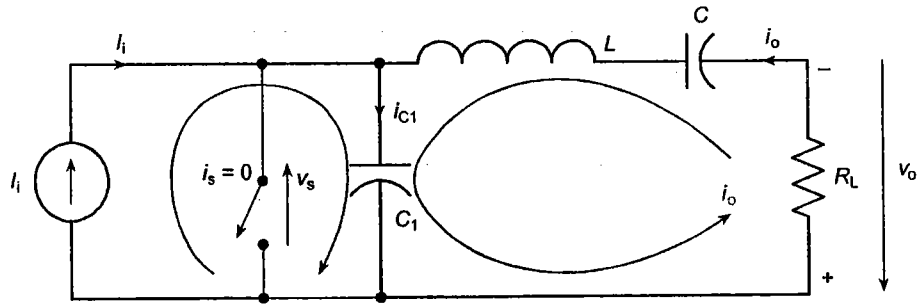
higher than the resonant frequency. The circuit diagram and the switching mechanism are shown in Fig. 9.14. The input or inductor current (I_i) is assumed to be constant due to large value of L_1. Therefore, it is shown by a constant current source. When the switch is turned on, the current through the switch is $I_i + i_o$ (mode 1). When the switch turns off, this current charges the capacitor, C_1 (mode 2). A slow voltage rise takes place across the switch. Now, C_1 is a part of the resonating network, L ($C + C_1$) and oscillation begins. The capacitor current (i_{C1}) becomes zero (at the peak voltage across it) and thereafter the direction of flow reverses (mode 3). The converter is designed for a low-damping ratio ($\xi \leq 0.07$) and a high-quality factor ($Q \geq 7$), which results in almost sinusoidal load current (i_o). A slight variation (increase) in switching frequency ($\omega_s > \omega_o$), reduces the output voltage significantly. The optimum duty-ratio is found to be 50% which results in maximum power capability. Moreover, at this condition the maximum value of switch current and voltage, $I_{s(max)}$ and $V_{s(max)}$ are found to be $3I_i$ and $3.5V_i$, respectively.



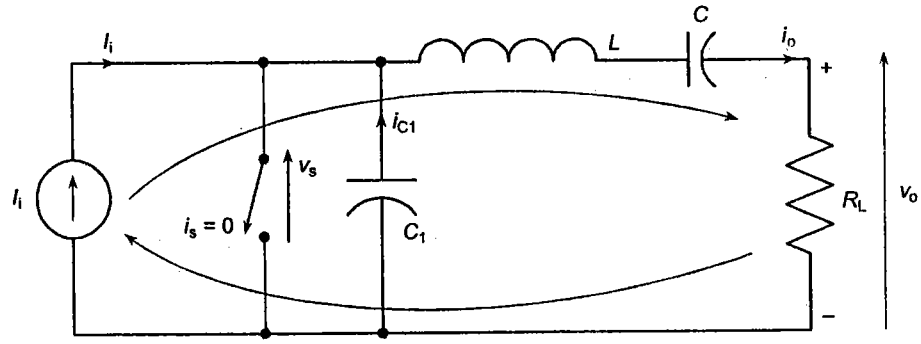
(a) Circuit diagram



(b) Mode 1

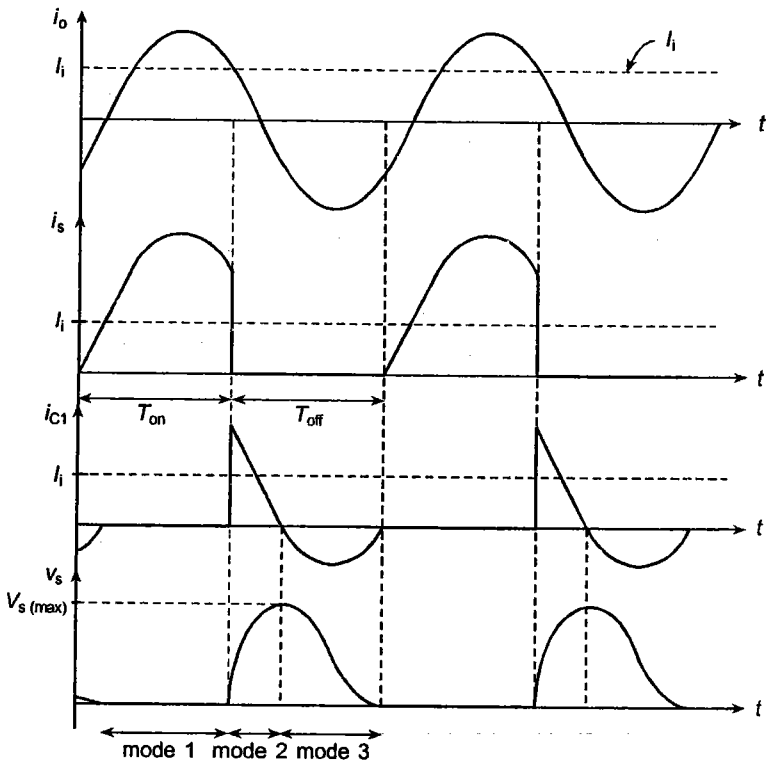


(c) Mode 2



(d) Mode 3

Figure 9.14 (*Cont.*)



(e) Waveforms

Figure 9.14 Class E-resonant converters.

Design considerations At maximum efficiency, the relation between various circuits parameters are given by

$$L_1 = 0.4\frac{R}{\omega_s}, \quad C_1 = \frac{2.165}{R\omega_s}, \quad \omega_s L - \frac{1}{\omega_s C} = 0.353R \tag{9.22}$$

With the help of a rectifier circuit at the output, it can act as a resonant dc-to-dc converter.

9.3.2 Resonant-switch Converters

Resonant switch converter topologies are developed by adding resonant elements (*LC*) to a PWM (or TRC) square-wave converter (as discussed in Chapters 7 and 8). The main function of the resonant switch converters is to reduce switching losses of the devices (MOSFET, IGBT, etc.) by operating these devices in zero-current switching (ZCS) or zero-voltage switching (ZVS) condition. Thus the current or voltage waveform becomes quasi-sinusoidal (half-wave) instead of square-wave in the dc-to-dc or dc-to-ac PWM converters. Therefore, these converters are basically quasi-resonant converters. The efficiency becomes high due to reduced losses in switching devices and EMI reduces due to sinusoidal wave shape. However, voltage and current stresses on devices and on-state conduction losses (due to high current) increase. The allowable load current and frequency variation for voltage control are limited. If the variation in frequency is desired for the

output control, it makes the filter design difficult. There are large number circuit topologies of resonant switch converters based on different PWM dc-to-dc converters as shown in Figs. 9.15 and 9.16. These converters can be divided into three broad categories. Configurations of both the half-wave and full-wave converters are also given as shown in Figs. 9.15 and 9.16.

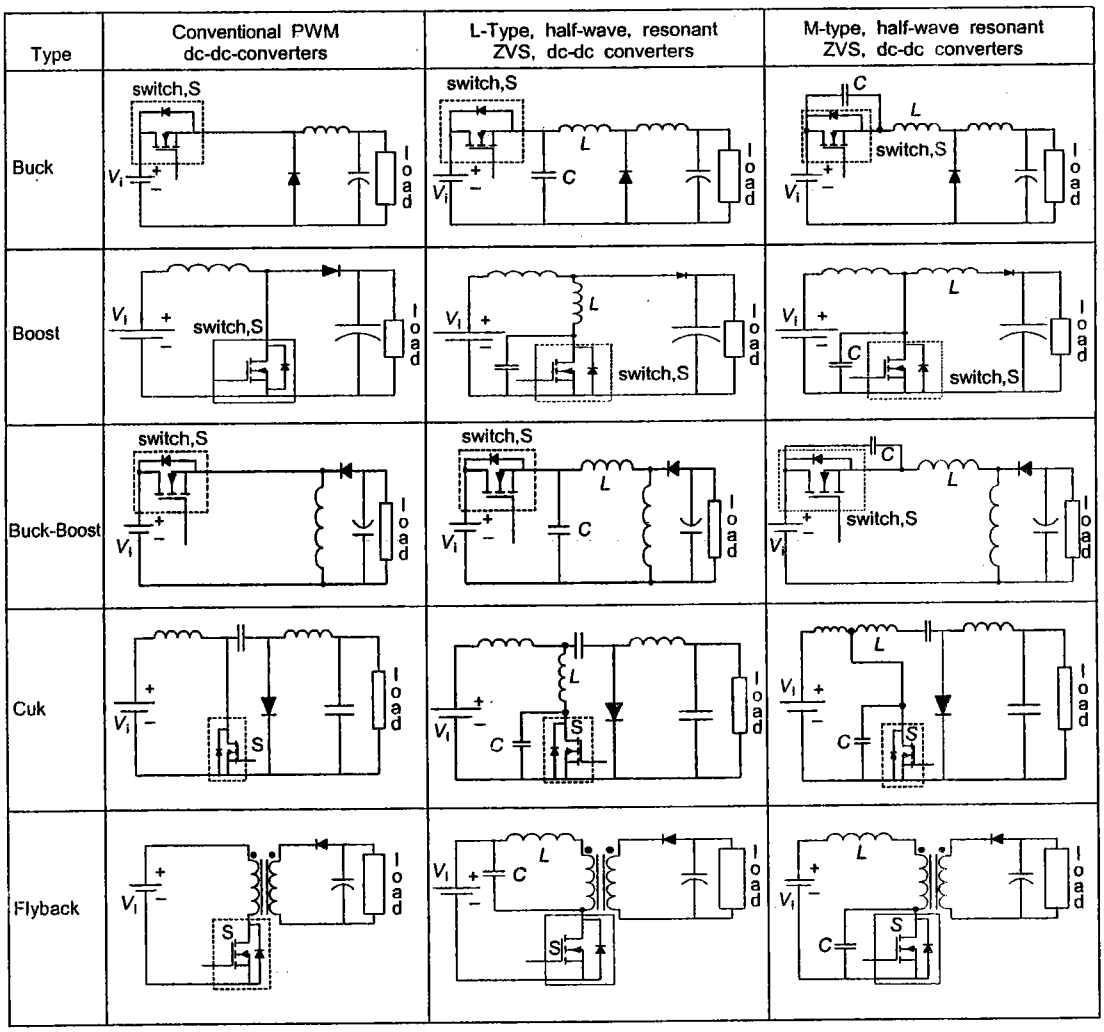


Figure 9.15 Different configuration of ZVS resonant converters. *Note:* (i) Full-wave configurations (for both, *L* and *M*) are possible by inserting an external-diode in series with the switch (S), to make the body-diode of the switch (device) ineffective. It makes four different configurations of each type of resonant converters. (ii) *C* and *L* are components of the resonant-switch.

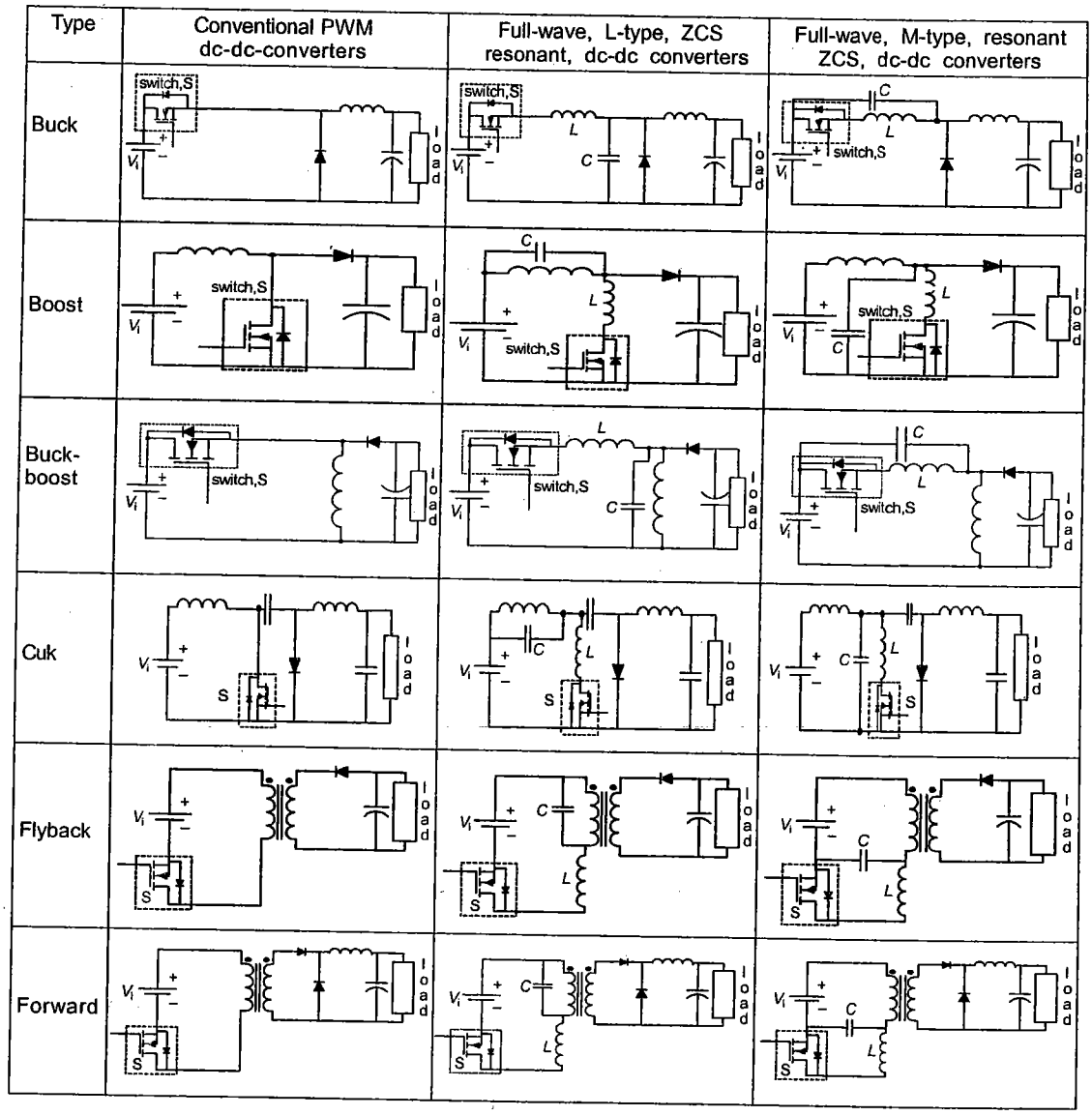
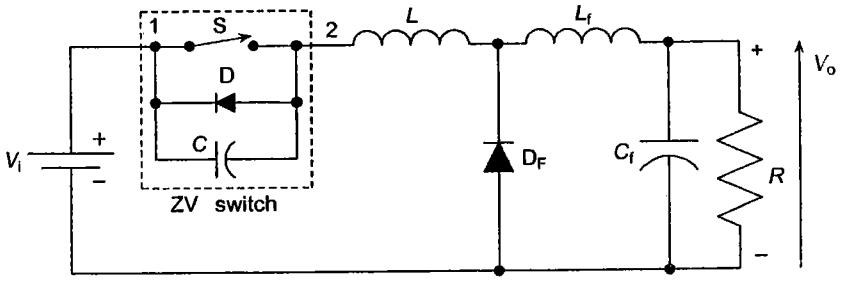


Figure 9.16 Different configuration of ZCS resonant converters. *Note:* (i) Half-wave configurations (for both, *L* and *M*) are possible by inserting an external-diode in series with the switch (S), to make the body-diode of the switch (device) ineffective. It makes four different configurations of each type of resonant converters. (ii) *C* and *L* are components of the resonant-switch.

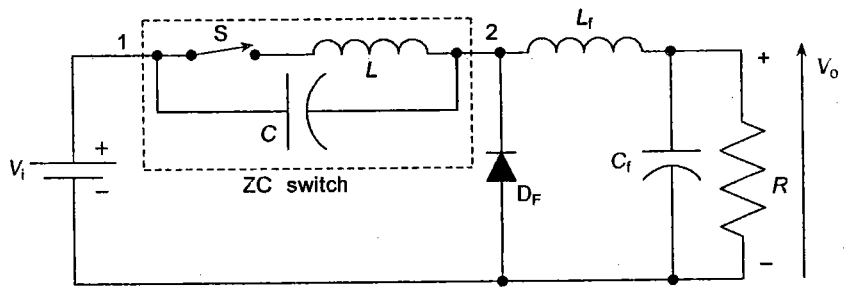
(a) *Zero-voltage switching* (ZVS) *topology*: Here the switch turns on and turns off at zero voltage. The switch is in parallel with the resonant capacitor and in series with the inductor (Fig. 9.17a). Moreover, there are half-wave and full-wave configurations (Fig. 9.15).

(b) *Zero-current switching* (ZCS) *topology*: Here the switch turns on and turns off at zero current. The resonant capacitor is in parallel with the switch and resonant inductor (Fig. 9.17b). Both half-wave and full-wave configurations are available (Fig. 9.16).

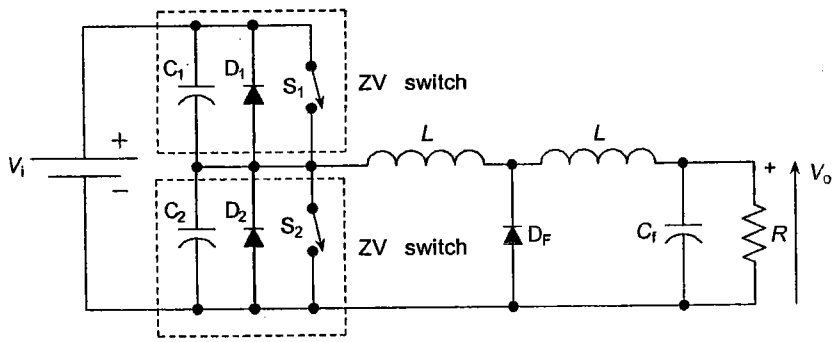
(c) *Multi-resonant ZVS topology*: It has combination of more than one ZVS topology (Fig. 9.17c).



(a) ZVS



(b) ZCS

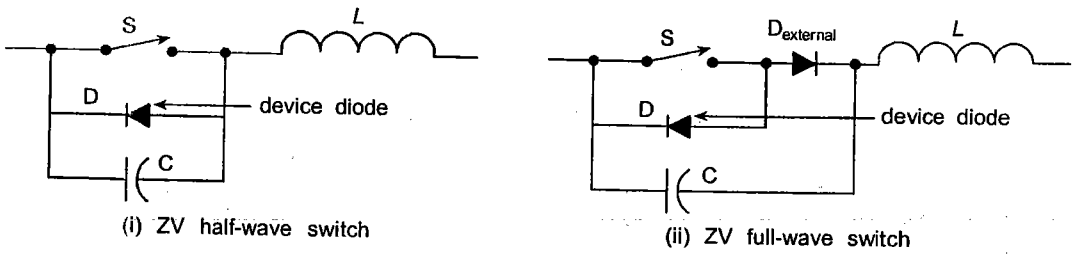


(c) Multi-resonant ZVS converters

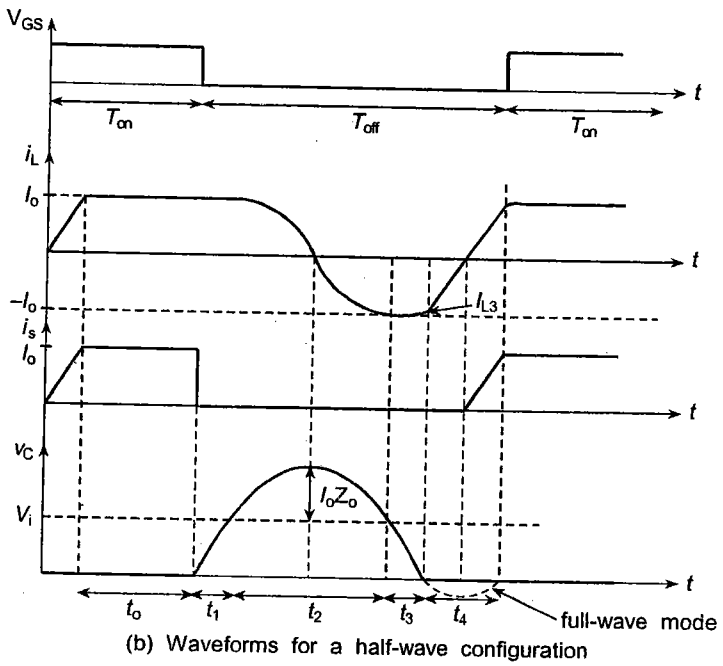
Figure 9.17 Circuit topologies of resonant switch converters.

ZVS Resonant-switch Converters

In this case, the switching device turns on and turns off while the voltage across it remains zero. Therefore, the switching loss is ideally zero. EMI is also small during the switching transition. The system can incorporate parasitic circuit elements and the converter can withstand a short-circuit condition. Figure 9.17a shows a ZVS resonant buck converter where the switch of a simple buck converter configuration is replaced by a zero-voltage resonant switch. It is a combination of an LC circuit and a switch. Normally, an anti-parallel diode is also fabricated with the switching device (e.g. a MOSFET), then the converter of this configuration is called a *half-wave converter* (Fig. 9.18a). If an additional (external) diode is connected in series with the switch (which makes the device anti-parallel diode ineffective), it is called a *full-wave configuration*. In this case, the voltage across capacitor (or switch) is allowed to become negative during the process of oscillation. Normally, the filter inductor (L_f) is sufficiently large, therefore I_o is considered to be constant. During the on period (T_{on}), a gate signal is provided to switch the device, as shown in Fig. 9.18b (e.g. V_{GS} for a MOSFET). The output voltage due to high value of C_F is considered to be constant ($v_o = V_o$).

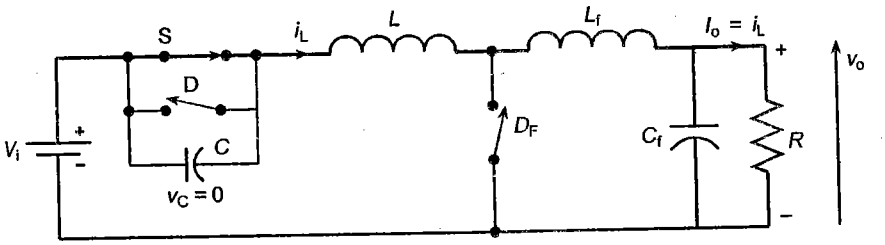


(a) Configurations

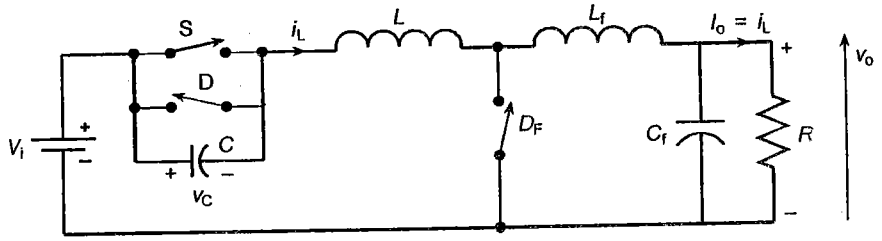


(b) Waveforms for a half-wave configuration

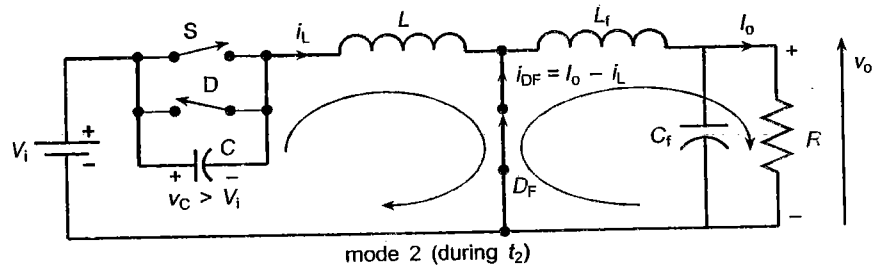
Figure 9.18 (*Cont.*)



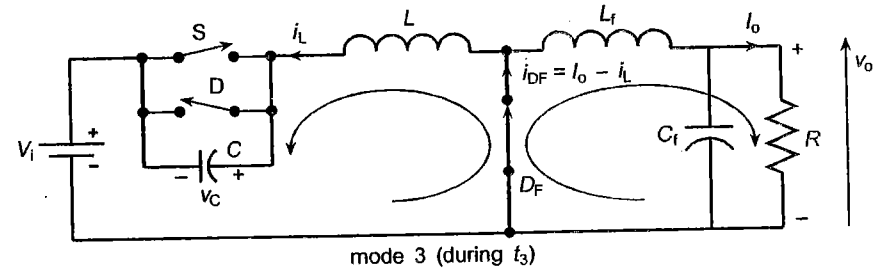
mode 0 (during t_o)



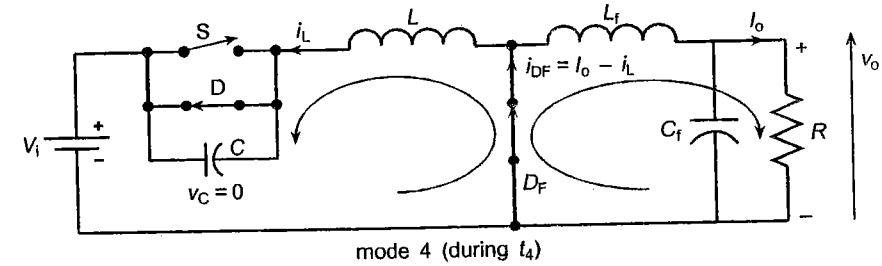
mode 1 (during t_1)



mode 2 (during t_2)



mode 3 (during t_3)



mode 4 (during t_4)

(c) Different modes of switching of ZVS converters

Figure 9.18 ZVS converters with half-wave switch.

During mode 0 or t_o period, the switch is on and a constant load current, I_o, flows through the switching device and both the inductors, as shown in Fig. 9.16c. When the switching device turns off at the end of t_o, the voltage across the device due to C, does not jump to V_i level, rather it increases gradually from the zero level. Since the turn-off takes place at zero-voltage condition, that is why, it is called zero-voltage switching (ZVS). The load current remains constant due to the large value of L_f. At the beginning of T_{off} period (mode 1), the capacitor C, gets charged at a constant current (I_o). When v_C exceeds V_i level, D_F becomes forward biased and conducts. The inductor current, i_L flows in V_i, D_F, L, C loop. Now, L and C resonate in this circuit up to the end of t_2 (mode 2). At the end of t_2 direction of current reverses. The difference of i_L and I_o flows in D_F (mode 2). From middle of t_2 and during entire t_3 period, i_{DF} is sum of I_o and i_L. The oscillation of current continues during t_3 but v_C ultimately reduces to zero. In full-wave mode, v_C becomes negative due to continuation of the resonating current beyond t_3. However, in half-wave mode (which is common), at the beginning of t_4, the diode, D conducts across the switch and v_C remains zero during the entire t_4 period. The conduction of D ends when i_L become zero but D_F continues to conduct ($i_{DF} = |I_o - i_L|$). Then, the switch turns-on at zero current and zero voltage conditions for the next cycle (mode 4) and i_L rise linearly till it reaches to I_o level. The magnitude of I_o is maintained by i_{DF} (according to the difference of I_o and i_L). For the sake of simplicity of analysis, the time reference is considered to be at the begining of each period or mode. During mode 1, the capacitor is charged with a constant current (I_o), therefore, the capacitor voltage rises linearly which is given by

$$v_C = \frac{1}{C}\int i\,dt = \frac{I_o}{C}t, \qquad 0 < t < t_1 \tag{9.23}$$

At the end of this mode, $t = t_1$, and $v_C = V_i$. Therefore, $v_C = V_i = I_o t_1/C$. Also, with this initial condition ($v_C = V_i$), oscillation starts at the beginning of the t_2. Thus from (A29) of Appendix,

$$v_C = I_o\sqrt{\frac{L}{C}}\sin\omega_o t + V_i, \qquad 0 < t < t_2$$

It may be noted that during t_2, the direction of i_L reverses. Now, it tries to reduce the voltage across C. However, the polarity of C remains same during t_2 and t_3. At the beginning of the t_3, $v_C = V_i$ and $i_L = -I_o$. Again from (A29),

$$v_C = V_i - I_o\sqrt{\frac{L}{C}}\sin\omega_o t, \qquad 0 < t < t_3 \tag{9.24}$$

The peak of v_C that appears across the switch is given by

$$V_{C(max)} = I_o\sqrt{\frac{L}{C}} + V_i, \qquad t = \frac{t_2}{2} \tag{9.25}$$

The inductor current, i_L is given by

$$\begin{aligned} i_L &= I_o\cos(\omega_o t), \qquad 0 < t < t_2 \\ &= -I_o\cos(\omega_o t), \qquad 0 < t < t_3 \end{aligned} \tag{9.26}$$

The half-wave oscillation period, $t_2 = \pi\sqrt{(LC)}$. At the end of t_3, $v_C = 0$, therefore, from (9.24),

$$V_i = I_o\sqrt{\frac{L}{C}}\sin\left(t_3\sqrt{LC}\right)$$

Also at the end of t_3, $i_L = I_{L3}$. The expression for t_3 and I_{L3} can be obtained as

$$t_3 = \sqrt{LC}\sin^{-1}\left(\frac{V_i}{I_o}\sqrt{\frac{C}{L}}\right)$$

and

$$I_{L3} = -I_o \cos \omega_o t_3 \tag{9.27}$$

During t_4 period, i_L rises linearly from I_{L3} to I_o and it is given by

$$i_L = I_{L3} + \frac{V_i t}{L} \tag{9.28}$$

At the end of t_4, its value is given by

$$t_4 = (I_o - I_{L3})\frac{L}{V_i} \tag{9.29}$$

Although the period, t_2 is constant for a resonant circuit but t_3 is load dependent. The switch must not be turned on before t_3, otherwise C discharges through the switch. Thus ZVS and ZCS at turn-on condition cannot be achieved. In general, ZVS converters are used for constant loads. The operation of this circuit is adversely affected by the parasitic junction-capacitance of D_F. When the diode is about to turn-off (during linear stage), parasitic oscillations occur between this parasitic capacitance and the resonant inductor (L). Moreover, another demerit is the high-peak voltage that appears across the switch and it may be 4 or 5 times the input dc voltage. This voltage depends upon the load current. The device voltage rating or SOA has to be selected accordingly.

Example 9.3 Design a ZVS, step-down or forward (buck) resonant converter. The converter specifications are given as: load current, $I_{o(min)} = 2$ A, $I_{o(max)} = 10$ A, $V_o = 24V_{dc}$, switch or device allowable voltage limit, $V_{s(max)} = 500$ V, resonant frequency, $f_o = 0.5$ MHz and the dc input voltage regulation = ±20%.

Solution The maximum and minimum value of load resistances are, $R_{max} = 24/2 = 12\ \Omega$, and $R_{min} = 24/10 = 2.4\ \Omega$. The peak device voltage $[V_{s(max)} = (V_i + I_oZ_o)]$ increases with the load. As the load current varies several times, $V_{s(max)}$ also varies accordingly. Thus, characteristics impedance ($Z_o = \sqrt{L/C}$) should be minimized to reduce $V_{s(max)}$ and it should be maximized to increase the load range. The worst-case, peak voltage occurs at maximum input voltage, $V_{i(max)}$ and maximum load current, $I_{o(max)}$ (or minimum load resistance, R_{min}). The limiting value is $V_{i(max)} = I_{o(min)}Z_o$ for ZVS. Therefore, a term conversion ratio is defined, which is given by

$$M = \frac{V_o}{V_{i(max)}} = \frac{V_o}{I_{o(min)}Z_o} = \frac{I_{o(min)}R_{max}}{I_{o(min)}Z_o} = \frac{R_{max}}{Z_o}$$

Let $M = 0.3$, then $Z_o = R_{max}/M = 12/0.3 = 40\ \Omega$, which gives, $L = 1600C$. Also, the time period at resonance condition,

$$T_o = \frac{1}{f_o} = 2\pi\sqrt{LC} = \frac{10^{-6}}{0.5}$$

It gives, $L = 0.01265$ mH and $C = 0.008\ \mu$F. Also, $V_{i(max)} = 24/0.3 = V_o/M = 80$ V. The nominal voltage, $V_{i(nom)}$ can be found from the equation of voltage regulation, which is given by

$$\frac{V_{i(max)} - V_{i(nom)}}{V_{i(nom)}} = 0.2$$

Then

$$V_{i(nom)} = \frac{V_{i(max)}}{1.2} = \frac{80}{1.2} = 66.67\ \text{V} \quad \text{and} \quad V_{i(min)} = (1 - 0.2)V_{i(nom)} = 53.4\ \text{V}$$

The maximum voltage across the switch,

$$V_{s(max)} = V_{i(max)} + I_{o(max)}Z_o = 80 + 10 \times 40 = 480 \text{ V}$$

Therefore, V_s is within the allowable range (i.e. 500 V).

There are several design considerations. First, the resonant converter is half-wave type or full-wave type. Second, the input and output conditions, viz., (i) $V_{i(min)}$ and $I_{o(min)}$, (ii) $V_{i(min)}$ and $I_{o(max)}$, (iii) $V_{i(max)}$ and $I_{o(min)}$, and (iv) $V_{i(max)}$ and $I_{o(max)}$. Let us consider, a half-wave resonant converter with $V_{i(min)}$ and $I_{o(max)}$ condition, $V_{i(min)} = 53.4$ V, $I_o = 10$ A.

The linear charging period of the capacitor,

$$t_1 = \frac{V_{i(min)}C}{I_o} = \frac{53.4 \times 0.008 \times 10^{-6}}{10} = 0.0427 \text{ μs}$$

The resonating period for half-wave ($\omega_o t_2 = \pi$) and $t_2 = T_o/2 = \pi/(2\pi f_o) = 1$ μs. The constant discharging period of capacitor,

$$t_3 = \sqrt{LC}\sin^{-1}\left(\frac{V_{i(min)}}{I_o}\sqrt{\frac{C}{L}}\right) = 0.318 \times 10^{-6}\sin^{-1}(5.34 \times 0.025) = 0.0426 \text{ μs}$$

For an ideal inductor, the energy dissipation (stored) over a cycle is zero. For a constant average value of load current ($i_L = I_L$),

$$\text{Energy} = \int v_L i_L \, dt = \int v_L \, dt = 0$$

Since $L << L_f$ (neglecting L in comparison to L_f), then

$$\int_0^{T_{on}} v_{Lf} \, dt = \int_0^{T_{off}} v_{Lf} \, dt$$

or

$$(V_{i(min)} - V_o)\, T_{on} = V_o T_{off}$$

or

$$T_{on} = \frac{V_o}{V_{i(min)} - V_o} T_{off} = \frac{24}{53.4 - 24} 3.44 = 2.8 \text{ μs}$$

We also have,

The minimum switching time period, $T_s = 3.44 + 2.8 = 6.24$ μs

The maximum switching frequency, $f_s = 160.25$ kHz

At the end of t_3 period, the time elapsed after the beginning of the oscillation is $(t_2 + t_3)$. Therefore,

$$I_{L3} = I_o\cos[\omega_o(t_2 + t_3)] = 10 \cos [2\pi \times 0.5 \times 10^6(1 + 0.0428)10^{-6}] = -9.9 \text{ A}$$

During t_4, the inductor current rises linearly ($v_L = di/dt$). Therefore,

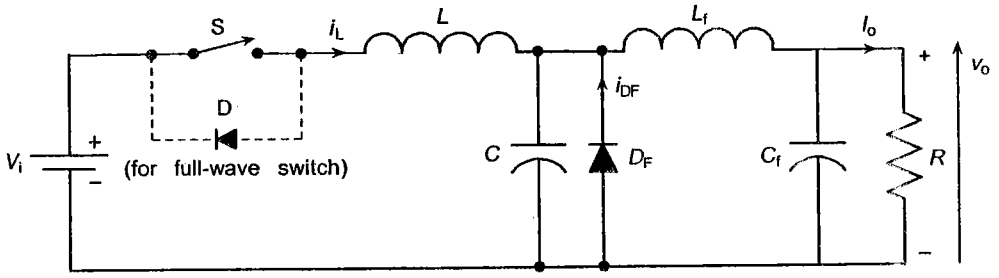
$$t_4 = \frac{(I_o - I_{L3})L}{V_{i(min)}} = \frac{(10 + 9.9)(12.65)}{53.4} = 4.71 \text{ μs}$$

The switch turns-on at the mid of t_4 period, otherwise, the current-reversal (now positive after $t_4/2$), will start resonating oscillation with the capacitor. Therefore, the total off-period,

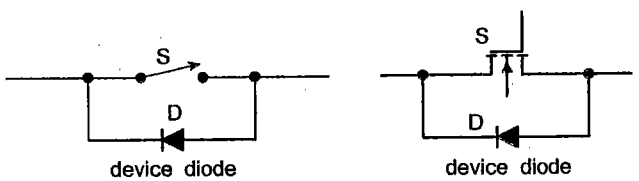
$$T_{off} = t_1 + t_2 + t_3 + \frac{t_4}{2} = 3.44\ \mu s$$

ZCS Resonant Switch Converters

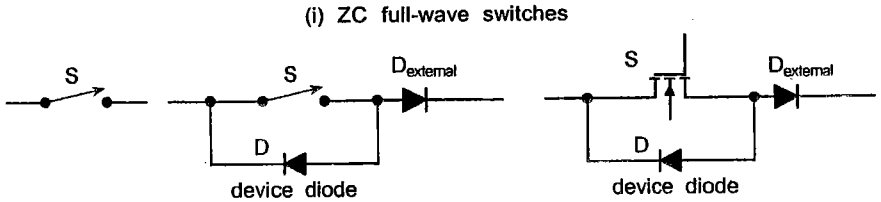
In this case, the turn-off loss of the switching device is almost eliminated. The operating frequency of converter varies from 1 MHz to 2 MHz which is less than that of ZVS converters. Figure 9.19a shows a ZCS resonant buck converter, where the switch of a simple buck converter is replaced by a ZCS circuit (LC resonant circuit and switch). Normally, an anti-parallel diode (D) is also fabricated across the switching device (e.g. a MOSFET), as shown in Fig. 9.19b. When this type of switch is used, then it is called a *full-wave* configuration (where the current reversal is possible). To make the anti-parallel diode of the device ineffective, an external diode is connected in series with the switch. It blocks the reverse current and it is called a *half-wave* configuration. Also, the inductance of the filter inductor is very high ($L_f >> L$). Therefore, the inductor voltage (v_{Lf}) becomes equal to $V_i - V_o$, during the entire on-period of the device. Similarly, the output voltage is considered to be constant due to high value of C_f ($v_o = V_o$).



(a) Circuit for half-wave



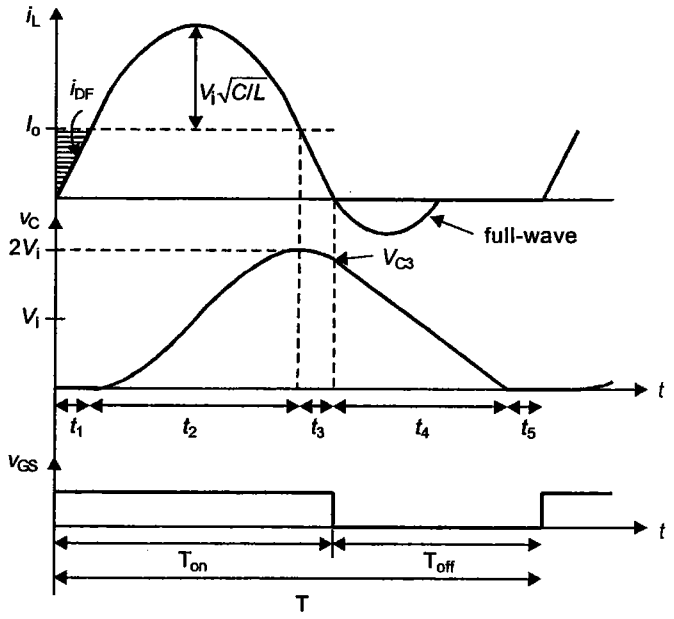
(i) ZC full-wave switches



(ii) ZC half-wave switches

(b) Switch configurations

Figure 9.19 (*Cont.*)



(c) Waveforms of a half-wave configuration

Figure 9.19 Half-wave ZCS resonant converters.

Before the switching of the devices or switch ($t < 0$ or during t_5), D_F was conducting and diode current, $i_{DF} = I_o$. When the switch is turned on at $t = 0$, i_L rises linearly ($i_L = V_i t/L$). The difference of I_o and i_L flow through D_F ($i_{DF} = I_o - i_L$). The voltage across C remains zero during the entire conduction period of D_F (including t_5). When i_L becomes equal to I_o, i_{DF} becomes zero and D_F turns off at the end of t_1. Now, during t_2, L resonate with the capacitor, C. The voltage across the capacitor begins to build up. As discussed in previous case, the time reference is considered to be at the begining of each period for the purpose of analysis. During t_2, the inductor current and the capacitor voltage are given by

$$i_L = V_i\sqrt{\frac{C}{L}}\sin\omega_o t + I_o \quad \text{and} \quad I_{L(max)} = I_o + V_i\sqrt{\frac{C}{L}}$$

Also,

$$v_C = V_i(1 - \cos\omega_o t) \quad \text{and} \quad V_{C(max)} = 2V_i, \quad \text{at } t = t_2 = \pi\sqrt{LC} \tag{9.30}$$

During t_3 period, the voltage across capacitor and the current through inductor are given by

$$i_L = I_o - V_i\sqrt{\frac{C}{L}}\sin\omega_o t$$

$$v_C = 2V_i\cos\omega_o t \tag{9.31}$$

At the end of t_3, $v_C = V_{C3}$, the resonating current, $i_L = 0$. Thus from the current equation

$$I_o = V_i \sqrt{\frac{C}{L}} \sin \omega_o t_3$$

or

$$t_3 = \sqrt{LC} \sin^{-1}\left(\frac{I_o}{V_i}\sqrt{\frac{L}{C}}\right) \tag{9.32}$$

During t_4 period, the switch is off. The capacitor voltage decreases almost linearly as it supplies a constant load current (I_o). Therefore, at the end of t_4, $v_C = 0$

$$I_o = C\frac{dv_C}{dt} = C\frac{V_{C3}}{t_4}, \qquad t_4 = \frac{V_{C3}C}{I_o}$$

At the beginning of t_5, v_C tends to become negative due to the resonating LC circuit. Therefore, D_F conducts and the load current, I_o flows through D_F. The peak resonating current must be higher than I_o for a half-wave ZCS converter. For a full-wave configuration (having an anti-parallel diode with the switch), i_L continues to flow during t_4 and the converter becomes insensitive to the variations of R (load).

Example 9.4 The input unregulated dc voltage to a ZCS resonant converter varies from 70 V to 100 V. The output load current varies from 2 A to 10 A at 24 V. Find the peak values of the switch (MOSFET) current and the capacitor voltage, where the resonant frequency is 1 MHz.

Solution For the worst case (lower input voltage and higher load current),

$$Z_o = \sqrt{\frac{L}{C}} = \frac{V_i}{I_o} = \frac{80}{10} = 8\ \Omega \quad \text{and} \quad L = 64C$$

Also,

$$f_o = \frac{1}{2\pi\sqrt{LC}} = 10^6$$

The worst case above equations gives, $C = 0.02$ μF and L = 1.27 μH. The peak current for the worst case,

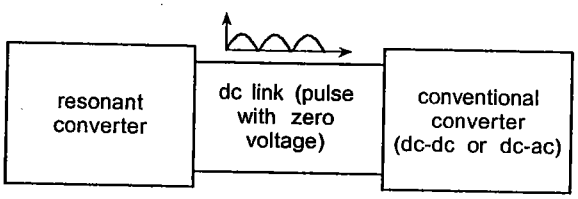
$$I_o + \frac{V_i}{Z_o} = 10 + \frac{80}{8} = 20 \text{ A}$$

The peak capacitor voltage, $V_{C(max)} = 2V_i = 200$ V.

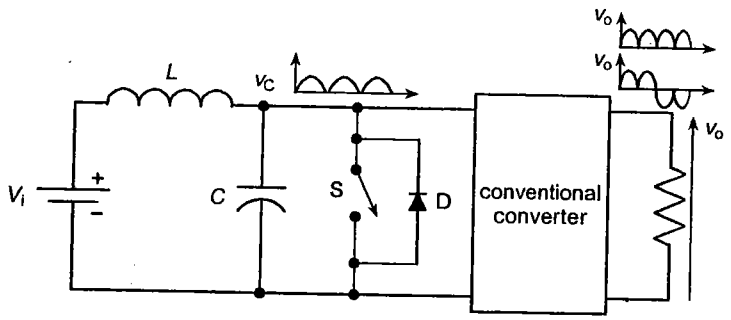
9.3.3 Resonant dc Link Converters

This is a modification of ZVS method based converters. In this case a resonant circuit is introduced in between a PWM converter and a final stage conventional converter (rectifiers and inverters). The switching losses are reduced to zero (ideally) obtained by holding the dc bus voltage at zero volts for the duration of switching transient. The dc bus is made oscillatory, ensuring that the voltage remains at zero volts for sufficient time. It enables a lossless switching to take place (for the final stage converter). The losses are restricted only by device on-state, storage and off-state periods, which are smaller than the switching losses.

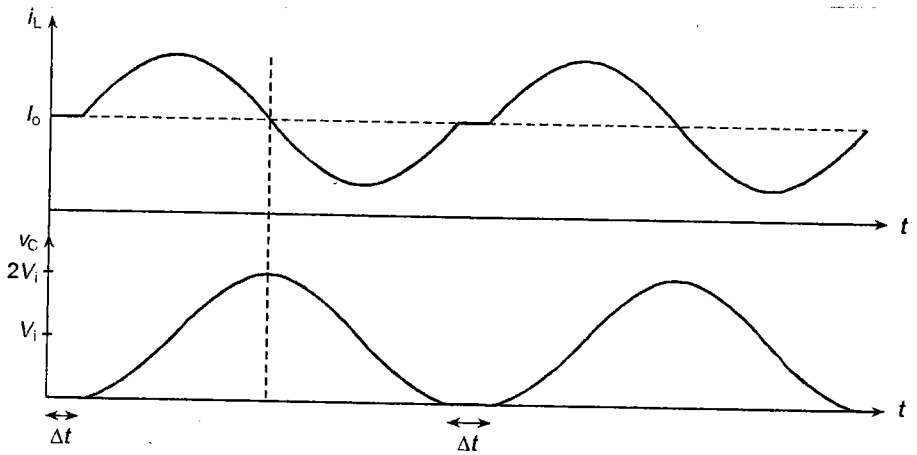
Figure 9.20 shows the functional block diagram, an equivalent circuit and relevant waveforms. It consists of a simple LC resonant circuit. The capacitor voltage remains at zero level



(a) Block diagram



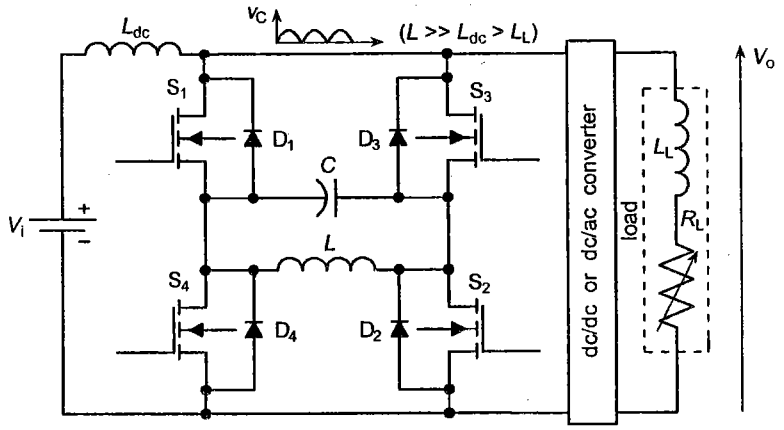
(b) Basic circuit topology (parallel loaded)



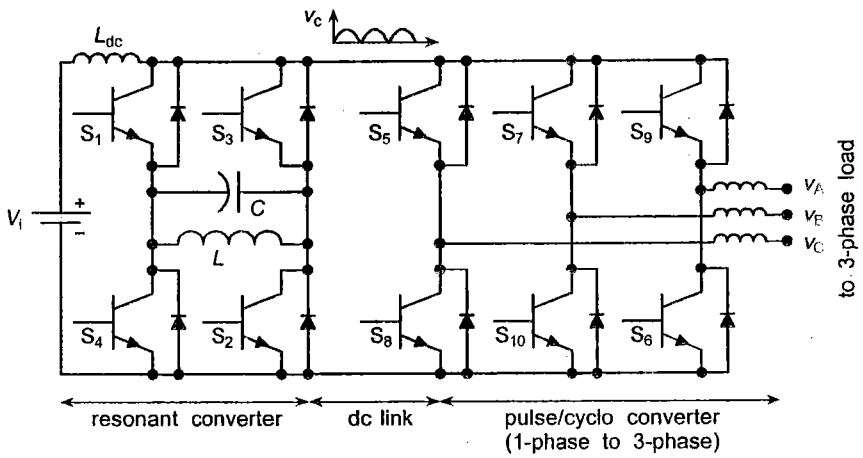
(c) Waveforms

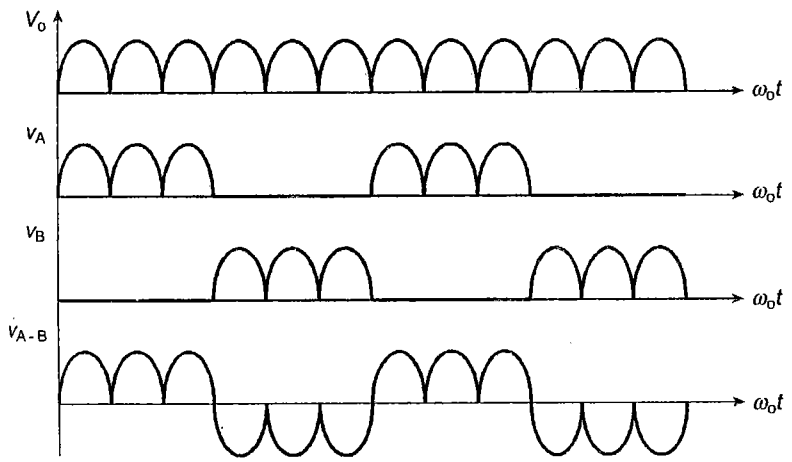
Figure 9.20 Operating principle of resonant dc link converters.

for sufficient period (Δt), where the switching of the devices in the converter of final stage takes place. It is evident that it is a case of ZVS configuration. Different number of half-cycles is also controlled, as in case of integral cycle control or cycloconverters, to get a rectifier or inverter voltage output of adjustable voltage and/or adjustable frequency (Fig. 9.21). Sometimes high-frequency ac signal generated by a resonant converter is reconditioned in the group of two pulses to control positive, negative or zero output voltage, as shown in Fig. 9.22.



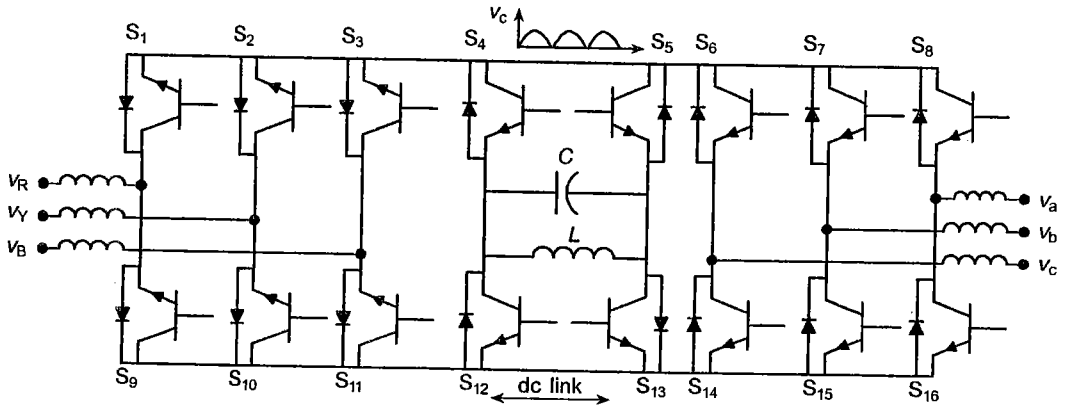
(a) A basic circuit of current source dc link resonant converter using full or H-bridge.



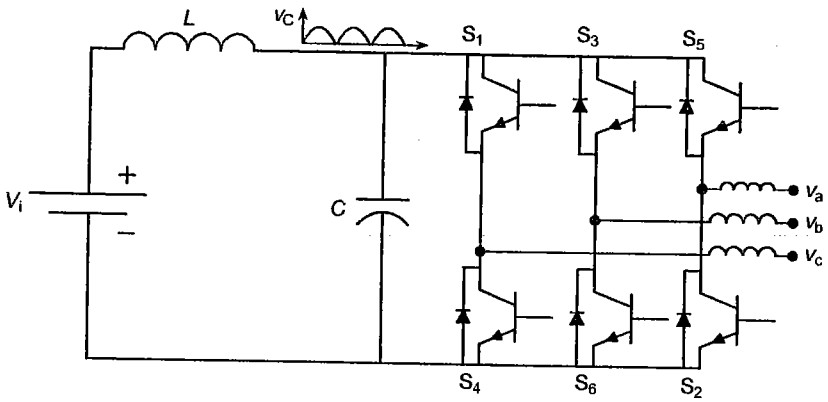


(b) Generation of low-frequency ac waveforms from integral pulses of resonant dc link (using discrete PWM)

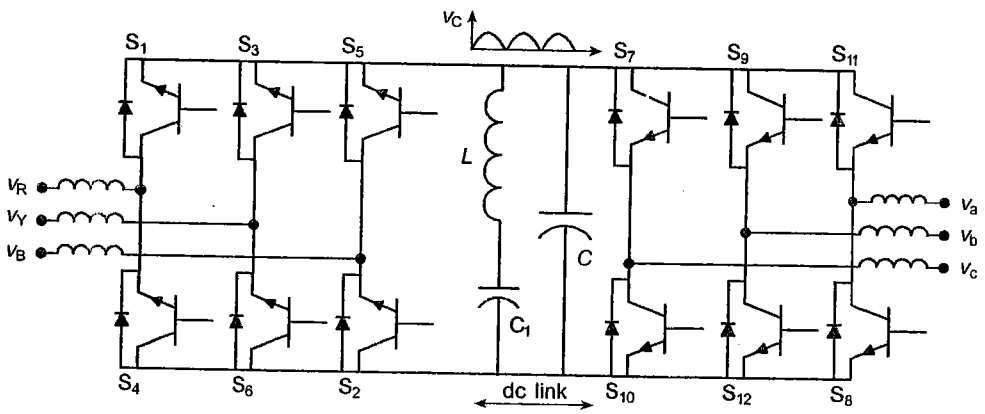
Figure 9.21 (*Cont.*)



(c) Three-phase-ac-to-three-phase-ac supply using resonant dc link converter topology

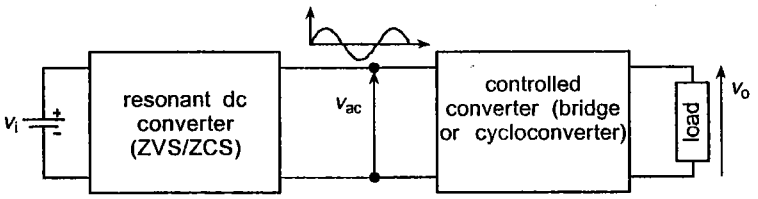


(d) A resonant dc link three-phase inverter

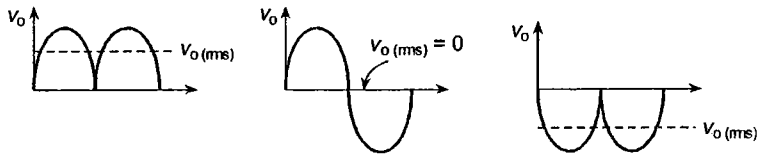


(e) Three-phase-ac-to-three-phase-ac supply using a resonant dc link inverter

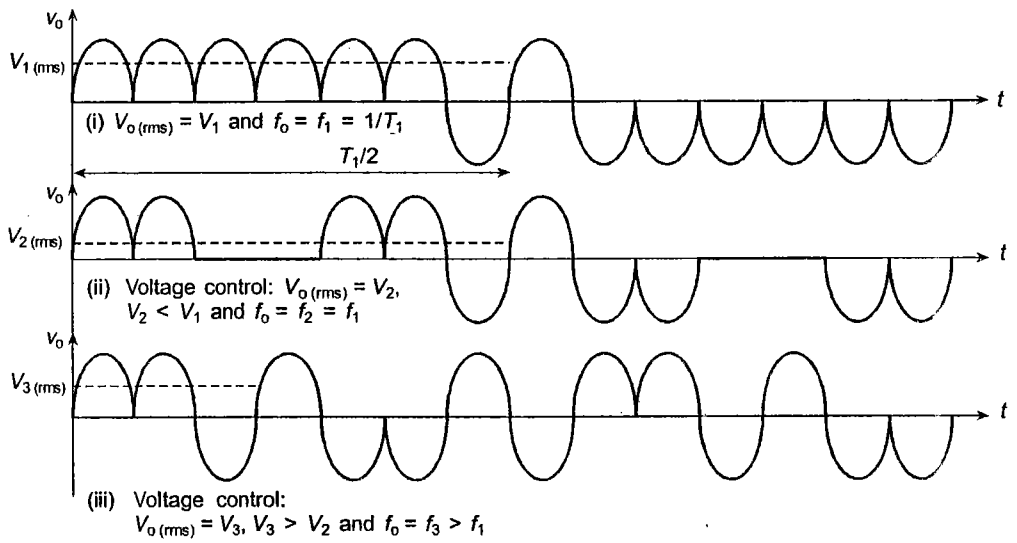
Figure 9.21 Different number of half-cycles.



(a) Block diagram



(b) Voltage control strategy



(c) Waveforms for voltage and frequency control

Figure 9.22 High frequency ac link resonant converters.

9.3.4 Resonant ac Link Converters

It is dual of resonant dc link converter (Fig. 9.22). Instead of a dc pulse or rectified pulse at dc bus, ac bus is used (Fig. 9.22a). The resonant converter that generates these ac pulses could be load-resonant converter or a resonant-switch converter. The final voltage control and wave shaping are done using the conventional converter at the final or output stage. If the desired output voltage is dc, a single-phase bridge configuration using thyristors/MOSFET/IGBT will suffice. If the final output is ac, then a single-phase or three-phase (according to the need) cycloconverter can be used. Figure 9.22b shows how the rms values are controlled. Both voltage and frequency can be easily controlled using cycloconverters, as shown in Fig. 9.22c.

SUMMARY

Resonant converters are highly efficient dc-to-dc and dc-to-ac converters. In case of converters with PWM control, the switching devices experience high voltage and current stresses. Therefore, the switching losses are significant. In case of resonant converters, *LC* resonating circuit is operated at or near resonant frequency which generates almost sinusoidal current and/or voltage waveforms. The switching devices operate (turn-on and turn-off) at ZVS or ZCS condition. Thus the switching losses and EMI reduce drastically. Since fast switching devices (MOSFET, IGBT, etc.) are available, these converters operate at very high resonant frequency (tens of kHz to several MHz). At this condition, the requirements of *L* and *C* parameters in resonant circuit and filter circuit drastically reduce.

In case of resonant load converters, the switching of an under-damped *RLC* load at resonance frequency causes oscillation of current (or voltage) and the current becomes almost sinusoidal. In case of ZVS or ZCS resonant circuits, switches of simple dc to dc converters are replaced by a switch and *LC* resonant circuit. Thus PWM strategy is replaced by a combination of PWM and LC resonant circuit. There are several other configurations which are basically ZVS, ZCS or their combinations. In case of dc link converters, the output of a resonant converter is again supplied to another converter (conventional) to get the desired output (dc or ac at desired voltage and/or frequency). Final stage voltage and frequency control are achieved by the second converter that may be a single or three-phase converter. Both duty-ratio and frequency control are applied for these converters to obtain the desired output. Integral number of half-cycles is controlled for frequency and the output voltage.

REVIEW QUESTIONS AND PROBLEMS

1. What are the advantages of resonant converters?
2. How do snubber circuits reduce voltage stress and switching losses in a switch?
3. What are demerits of resonant load series converters?
4. How is the output voltage controlled in the resonant converters?
5. Often frequency control is not recommended in resonant dc-dc converters, why?
6. What are merits and demerits of Q-factor in resonant converters?
7. What are advantages of a reverse-conducting thyristor (RCT) in resonant converters?
8. What are merits of class-E resonant converters?
9. What do you mean by full-wave and half-wave configuration of resonant switch converters?
10. What are major demerits of ZVS resonant switch converters?
11. How are voltage stress on switches reduced in ZVS resonant switch converters?
12. What are merits of dc link resonant converters?

13. Why are dc link resonant converters ideally loss-less?

14. With the help of output voltage waveforms, show different cases of the adjustable output dc voltage, for a high frequency link resonant converter.

15. What are limitations of a ZCS resonant switch converter for its proper functioning?

16. Among full-wave and half-wave configurations of ZCS resonant switch converters, which one is preferable and why?

17. Analyse a half-wave ZVS buck resonant converter for maximum input voltage and maximum load current, where V_o = 24 V, I_o = 3.5 A to 10 A, f_o = 500 kHz, M = 0.3, input dc voltage regulation = ±20%.

18. Analyse a half-wave ZVS buck resonant converter for minimum load current where V_o = 24 V, I_o = 2 A to 10 A, f_o = 2 MHz, V_i = 100 V, dc input voltage regulation = ±30%.

19. A series resonant LC converter is operating at 40 kHz with 10 Ω load and 100 V peak voltage. Find the values of L, C and the maximum amplitude of the third harmonic load current at 1/4th maximum output power, where the frequency control is restricted to 20% below ω_o. (*Hint:* The third harmonic voltage of a square wave is 1/3 of the fundamental.)

10

UPS and SMPS

10.1 INTRODUCTION

High-quality, regular and uninterrupted power supply is a basic need of power consumers. However, the power quality (voltage level, frequency, harmonic free-voltage, etc.) deteriorates and supply is affected due to outage and blackout. Although there are certain limits of the quality of power supplied by power generation companies, but in poorly maintained distribution system, power outage and blackout (no power at all) are very common. Moreover, some equipment (e.g. computers, hospital equipments including pre- and post-surgery medical care systems, process control systems, communication systems) requires better quality of power than conventional equipments. Such equipments are called *critical* equipments. These equipments are sensitive to power supply for their proper functioning. Therefore, the quality of the power supplied must meet certain specifications. This requires conditioning (power quality control) and uninterruptible power supply. Therefore, uninterruptible power supply (UPS) is needed for such equipments for satisfactory and reliable operation of these systems. Normally, these equipments are computer based systems or electronic control and measuring systems. In general, a regulated dc power supply is needed for linear/analog or digital IC based electronic circuits and control systems. For this purpose, conventional or linear power supplies are available. It is an ac-to-dc converter, where output dc voltage is maintained. Normally, it contains transformer, diode (rectifier) bridge and a transistor based voltage regulator circuit, as discussed in Chapter 7. A compact rectifier stack and an IC based voltage regulator circuit are available, which reduce the size and complexity of the power supply circuit. However, the linear or conventional power supply suffers from several drawbacks. The size and the weight of the mains frequency transformer (50 to 60 Hz) are much more than the size and the weight of the high-frequency transformers used for the same application. Moreover, the voltage regulator circuit, in fact, acts as an adjustable resistance in series with the load (R_L) to control the output voltage (V_o). The transistor of the regulator circuit acts in the active region. A sufficiently high large magnitude of the load current flows through the transistor and there appears a significantly voltage drop across it. It causes high power loss. Therefore, overall efficiency lies between 30–60%. Moreover, for several isolated output voltages

with different common (negative) terminals, seperate secondary winding and separate control circuit are required for each case. It increases cost and size of the linear power supply. Therefore switched-mode power supply (SMPS) is preferably used.

10.2

DISTURBANCES IN COMMERCIAL POWER SUPPLY

It is obligatory to maintain the standard quality of power supplied by a commercial utility (power supply). The required standard quality of power has following characteristics:

1. Pure sinusoidal voltage waveform (no harmonics)
2. Constant magnitude (rms) of the voltage
3. Constant mains frequency (50 or 60 Hz)
4. Balanced three-phase supply i.e. equal voltage of each phase and equal (120°) phase-difference
5. No short-time deviation from the above mentioned qualities (no spikes or no effect of transients).

Practically it is very difficult to maintain the above mentioned qualities in toto. Therefore, a deviation in these qualities up to certain extent is allowed. These deviations are different due to different types of disturbances in a power system.

10.2.1 Types of Disturbances

There are different types of disturbances which exist for both long as well as short durations. Following are different types of disturbances:

Voltage deviation A Poorly maintained distribution system very often experiences such problems. Low supply voltage (under-voltage condition) is common specially during the peak hours. If the supply voltage is higher than the nominal voltage, it is called *over-voltage* condition. If it exists for a few cycles only then it is not a serious problem.

Frequency deviation This is another bad quality of poorly maintained power supply. A frequency deviation even up to ±5% is common. It highly affects the performance of ac motors (e.g. magnetizing current, speed and torque of induction motors) and ac systems.

Voltage spikes It is a sharply rising voltage pulse superimposed over supply or mains voltage. It appears for very short duration. It is mainly due to switching transient voltage of circuit breakers or due to lightning strokes.

Harmonics A distorted supply voltage waveform contains high-order harmonics (Fig. 10.1a). It is usually odd and may be even in some cases (when the positive half-cycle is not same as the negative half-cycle of voltage waveform). Normally, non-linear loads of bulk consumers cause voltage harmonics. Switched-mode power supply (SMPS) and electronic ballast circuits for vapour lamps and CFL also introduce harmonics in the line current.

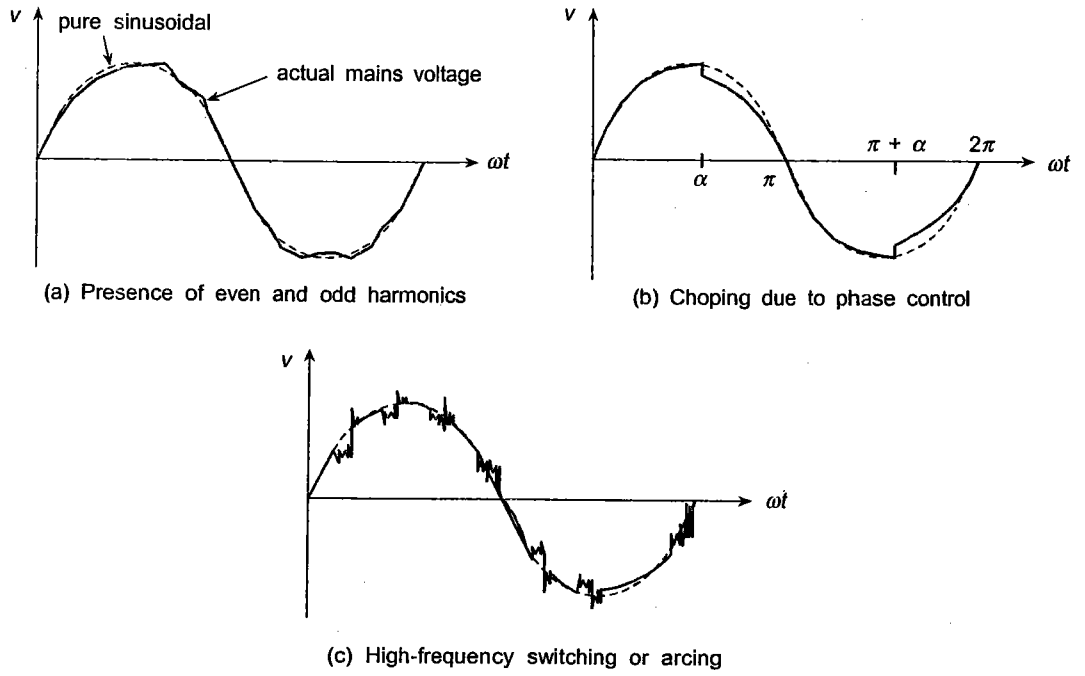


Figure 10.1 Distortions in supply voltage waveforms.

Chopped distorted voltage It is a deviation of voltage waveform from a purely sinusoidal wave shape. Switching or chopping of supply voltage and then re-switching, once or repeatedly, cause chopped and ringing voltage waveform. A thyristor based phase-control of load voltage (e.g. ac regulator switched at α, Fig. 10.1b) or a high-frequency ac voltage chopper may be the cause of such distortions (Fig. 10.1c). Sometimes, electric arc furnaces and welding transformers also introduce such distortions.

Electromagnetic interferences (EMI) It is a high-frequency noise or interference introduced in the supply line due to lighting, switching of power network, switching of high-frequency converters, voltage spikes of the spark plug of automobiles, etc. It may be due to electromagnetic effect (flux linkage) of other circuits or radiated signals from the other circuits. The later is called *radio-frequency interference* (RFI). It is a high frequency, cyclic series of spikes or noise injected to an electric line by means of radio-wave energy. Switching of power semiconductor devices (thyristors etc.) generates EMI over a wide spectrum. The interference may also propagate through conduction, where the interference current enters through the power supply connection. The effect is more adverse near the source of interference and for frequency range between 450 kHz to 30 MHz for interference voltage, and between 30 to 1000 MHz for interference field. For conducted RFI voltage, the effective frequency range of interference is between 50 kHz to 15 MHz.

Power outage and blackout This is an unacceptable quality of a matured power supply (utility). However, this happens, on regular basis, with a poorly maintained, irresponsible type of commercial power utility. Power outage is failure/disconnection of power for a short period of

time without prior notice. Blackout is also common with this type of poorly maintained utility. The failure/disconnection of power happens for a few hours to several days.

From the above discussion, it is evident that some disturbances are man-made and some are acts of God, which are beyond the control of human beings including the commercial utility. Therefore, to mitigate these conditions, a power conditioning unit is necessary for critical loads and systems.

10.2.2 Power Quality and Power Conditioners

Among the above mentioned disturbances, some disturbances cannot be eliminated at all, some can be reduced partially and some can be eliminated completely. The power outage, blackout and frequency deviation cannot be done away with power conditioners. For this purpose, inverters, UPS and/or stand by power supply are required. Normally, battery based UPS/inverters are used for a short duration backup period and diesel-generator (DG) set is used for a longer period.

The deviations from the ideal characteristics (or clean power) are allowed or acceptable to a certain extent only. For example, 5% *total harmonic distortion* (THD), i.e. deviation of supply voltage waveform from a pure sinusoidal waveform, is allowed. Moreover, the third harmonic or any other harmonic (up to 19th) should not be more than 3% (a harmonic below 0.6% is neglected, according to International Electrotechnical Commission, IEC). A frequency deviation of 0.5 Hz is allowed but the rate of deviation should not be more than 1 Hz/second. Normally, critical equipments can tolerate large voltage variations for very short duration, and sustained small variation from the nominal values. For example, according to the recommended practice for emergency and standby power systems (IEEE standard), a sustained (>30 cycles) voltage variation between +6% and −13% from the nominal voltage is acceptable. For a short period, the allowable limits are:

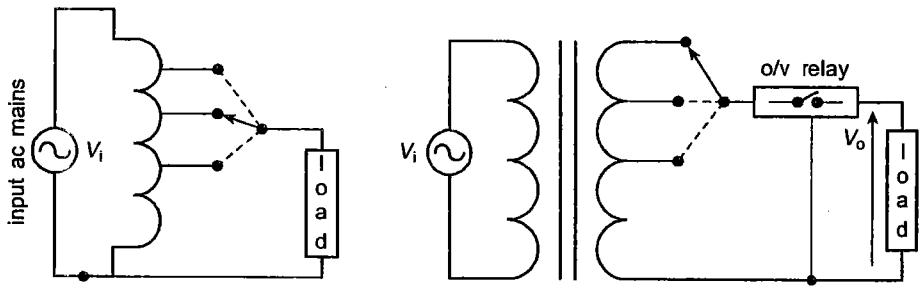
+15% to −35%:	for 1–30 cycles of ac voltage
More than 300%:	for 1% of a cycle (≅200 μs for 50–60 Hz)
More than 350%:	for 0.1% of a cycle (≅20 μs for 50–60 Hz)

Manufacturers of the critical loads and systems (e.g. SMPS of computers) also specify the limiting conditions of their products. Following devices or equipments are used to regulate or condition the power supply to the desired level and to protect the load from abnormal or undesirable conditions.

Voltage Deviations

There are several systems used to regulate the ac supply voltage which is at under voltage or over-voltage condition. These equipments are called *voltage regulators* or *voltage stabilizers*. Different types of voltage regulators or conditioners are discussed below:

Tap-changing transformers It is a simple and low-cost system. It varies from fraction kVA range for domestic appliances to hundreds of kVA distribution transformers. But the control is not fast if it is operated manually (Fig. 10.2). An automatic version is also used for low-power applications (voltage stabilizers). An autotransformer tap-changing arrangement is cheaper than a two-winding transformer arrangement. The output ac voltage is sinusoidal but the control is in steps. In both cases (automatic and manual), a fine control of the output voltage is not possible. Further, for a sudden rise in the input voltage (over-voltage), a contactor (electro-mechanical reed relay, EMR) switch is used which disconnects the supply. In case of a simple contactor type arrangement, there is blanking of the voltage supply to the load during the change of tappings.



(a) An auto-transformer arrangement (b) A two-winding transformer with over-voltage (o/v) protection.

Figure 10.2 Voltage control by tap changing.

Servo-voltage stabilizers Here the output of an auto-transformer is controlled by changing the position of the contactor by a servo-motor. Normally, it is used for a higher-power output (5 kVA and above). There is automatic control of the output voltage. Although very accurate, smooth and fine control of the output voltage without any distortion in the waveform is possible but the system does not respond to the sudden change in the input voltage. Moreover, the cost, weight, and size of the voltage stabilizer is high.

Constant-voltage transformers (CVT) It is a three-winding transformer whose ac voltage is regulated by the ferro-resonance principle. At a higher input voltage, the winding T_3 works under magnetic saturation, therefore, its inductance is low (Fig. 10.3). It draws a higher current and therefore voltage drop across T_1 increases. Both T_1 and T_2 windings act as linear inductors (unsaturated condition) and a reduced voltage reaches at the output (during over-voltage condition, when V_i is more than the desired rated or nominal voltage, V_n). During under-voltage condition ($V_i < V_n$), T_2 comes out from the saturated condition to the linear condition. Therefore, its inductance increases which causes a resonance with the capacitor and a high voltage appears across T_2 hence at the output. A small change in V_i pushes T_2 into or out of the resonance condition. For increasing the output voltage, an additional capacitor is added to change the (early) resonance condition.

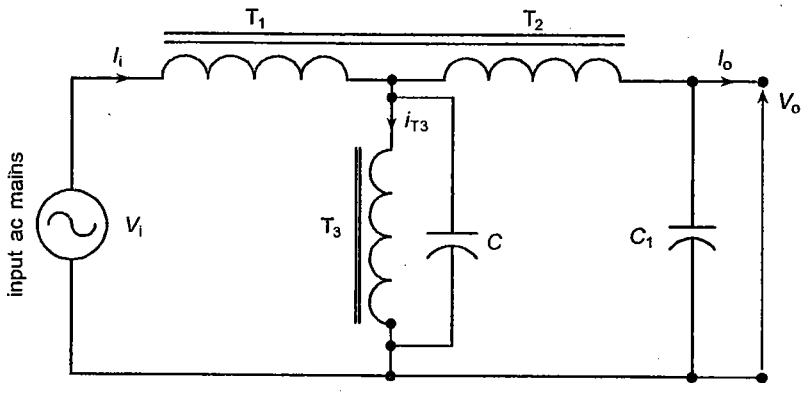
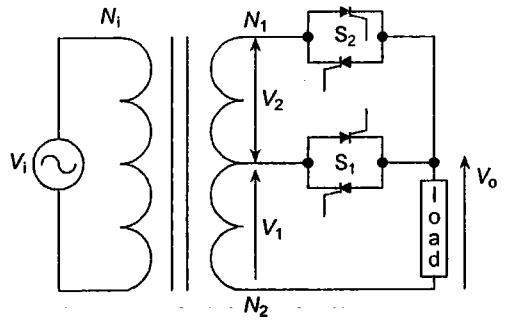


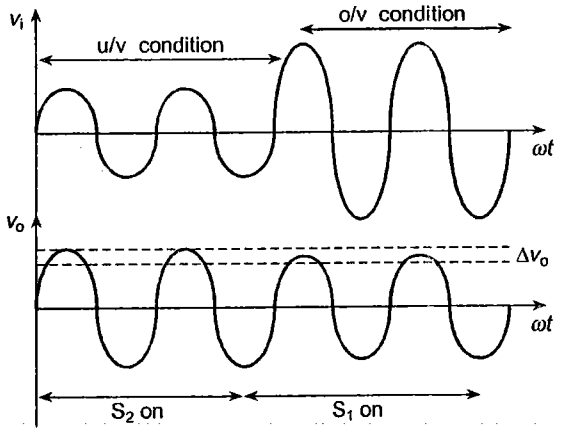
Figure 10.3 A constant voltage transformer (CVT), ac voltage regulator.

The output voltage control in CVT is almost instantaneous. It shapes good quality of voltage waveform, suppresses harmonics and maintains the output voltage constant (rms value). However, its size, weight, cost and losses are high. Moreover, it generates noise (EMI) due to saturation of core and also limits the starting current of the load.

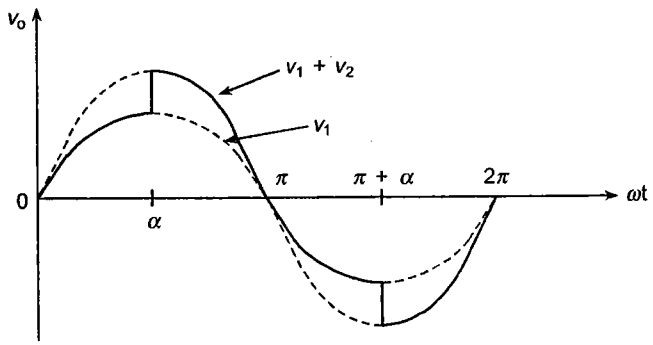
Electronic tap-changers It works on the same principle of tap-changing transformers. The contactor switch is replaced by thyristor (SCR or triac) based switches (Fig. 10.4a). Let $N_1 < N_i < N_1 + N_2$ then V_i greater than V_1 and less than $(V_1 + V_2)$ i.e. $V_1 < V_i < (V_1 + V_2)$, for a higher input voltage ($V_i > V_n$), switch S_1 operates (S_2 remains off), $V_o = V_1$ and $V_o < V_i$. For the lower-input



(a) Circuit diagram



(b) Voltage control in steps at under-volage (u/v) and over-voltage (o/v) with step control



(c) Fine voltage control using phase control switching

Figure 10.4 An electronic tap changer ac voltage regulator.

voltage, S_2 operates (S_1 remains off), $V_o = (V_1 + V_2)$ and $V_o > V_i$. These switches operate at zero-crossing instants. Therefore, the switching angle is zero ($\alpha = 0$) and V_o (rms value) is controlled in steps but it retains the input voltage waveforms (sinusoidal). Sometimes large number of tappings is used to reduce the steps of the output voltage control. Alternatively, a fine voltage control is possible at the cost of the sinusoidal voltage wave-shape or introduction to higher order harmonics, as shown in Fig. 10.4c. A fine voltage control, for $V_1 < V_o \leq (V_1 + V_2)$, is achieved by

keeping S_1 on (between $\omega t = 0$ to α and $\omega t = \pi$ to $\pi + \alpha$), while S_2 is closed (between α and π and $\pi + \alpha$ and 2π). For resistive load, the rms value of the output voltage is given by

$$V_o = \left[\frac{V_1^2}{\pi}\left(\alpha - \frac{1}{2}\sin 2\alpha\right) + \frac{(V_1 + V_2)^2}{\pi}\left(\pi - \alpha + \frac{1}{2}\sin 2\alpha\right)\right]^{1/2}, \quad \text{for } V_i < V_n \quad (10.1)$$

and

$$V_o = \left[\frac{V_1^2}{\pi}(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]^{1/2}, \quad \text{for } V_i > V_n \quad (10.2)$$

Although V_o (rms value) is precisely controlled but the main drawback is the distortion in voltage waveform due to ac regulator (α control). With the help of a level detector, the control circuit of ac voltage regulator acts quickly. It is an automatic voltage control system where a fine voltage control is achieved.

PWM ac regulators It is a multiple-pulse ac chopper. The number of pulses and the width of the pulses in each half-cycle controls the magnitude of the output voltage (rms value). It is a compact and low-cost system (as discussed in Chapter 5).

VOLTAGE SPIKES

It is sharp positive or negative non-repetitive voltage pulses superimposed over the supply voltage that exist for a short period of time. There are several devices used to suppress spikes in supply voltage as discussed below:

Isolation transformers It is used to isolate the load circuit from the input circuit. The load circuit becomes electrically isolated and magnetically linked with the source. It offers comparatively a large impedance (transformer winding leakage reactance at high frequency) to the voltage spikes. Thus it suppresses the spikes (which carries a higher-order harmonics in the waveform).

Snubber circuits (RC type) These offers a low-impedance path to divert the voltage spikes (as discussed in Chapter 2). Thus spikes do not reach the critical load.

Metal-oxide variastors (MOV) These are also used to bypass a high-voltage pulse or spikes. It offers a low-impedance path when the input voltage spike crosses the threshold voltage level (as discussed in Chapter 2).

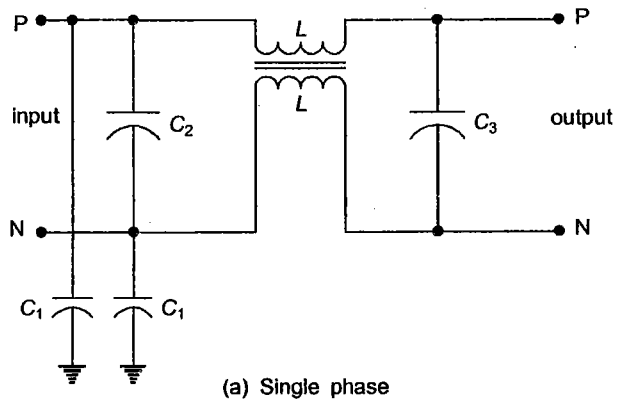
Transformers of voltage regulators It also suppresses the spikes as the transformer impedance comes in series with the load. The transformer winding leakage inductances offer more reactances (impedance) to a higher harmonics and voltage spikes.

HARMONICS

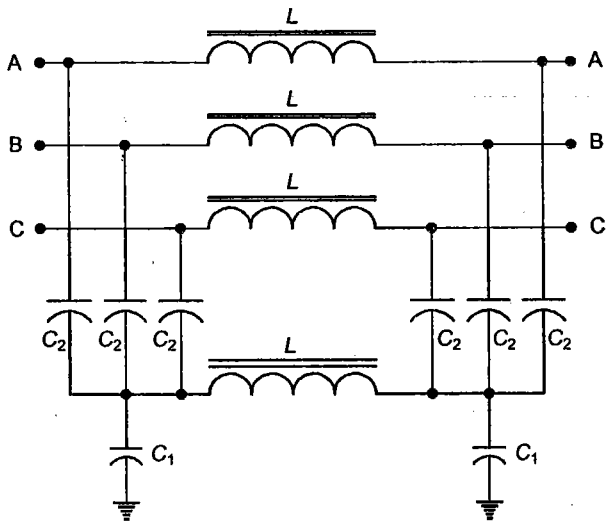
Normally the distorted waveforms of the output voltage carries higher-order harmonics. When a positive half-cycle waveform is same as the negative half-cycle waveform, only odd harmonics are present. Both active and passive filters are used to remove a particular or series of several harmonics. As discussed above, the transformer winding reactances appear in series with the load. Therefore, it offers a higher impedance to a high-order harmonics. Neglecting the transformer winding resistance (which is small), the winding reactances are $n\pi f\,(L_1 + L_2)$. Thus there will be a considerable voltage drop in the nth harmonic component across the transformer, where L_1 and L_2 are winding leakage inductances.

EMI AND RFI

To suppress these interferences, RFI filters are used. These are low-pass LC filters which blocks or attenuates high-frequency components of supply voltage or suppress voltage spikes (Fig. 10.5). The filter-parameters depend upon the current it handles.



(a) Single phase



(b) Three-phase

Figure 10.5 RFI filter circuits.

10.3

UNINTERRUPTED POWER SUPPLIES (UPS)

Some critical (or sophisticated) loads like computer, communication equipments, bio-medical instrumentation systems, surgical and post-surgery medical equipments, etc., require a continuous and good-quality power supply. These systems/loads cannot tolerate large transients, power

outage, over or under voltage, large harmonic contents and fluctuations in the line frequency. The allowable supply voltage variation is ±3% of its nominal value. The total harmonic distribution (THD) in the supply voltage should not be more than 5% while the third or any harmonic content should not exceed 3% limit. The tolerable supply frequency range is ±0.5 Hz. To meet all the above conditions without power failure even for a moment, UPS is employed to feed such critical loads. Normally, UPS incorporates a few or all the features of power conditioners to generate or supply clean power of the required quality.

The UPS can be broadly classified into two groups: off-line type and online type. These two are further classified as:

(a) Off-line, preferred type
(b) Off-line, interactive type
(c) On-line inverter, preferred type.

In off-line UPS, the ac mains directly supply the power to the critical loads and simultaneously charge the battery which is kept as back-up supply. The inverter is synchronized with the mains and is operative only under mains failure (or at abnormal condition of the supply, e.g. over-voltage or under-voltage conditions). The changeover takes place within 1/4 cycles. These types of UPS are cheaper and the control system is simple. On-line UPS are costlier than its counterpart. In this configuration, irrespective of the input or mains conditions (over-voltage, under-voltage, frequency too high or too low, etc.), the power is continuously supplied to the critical load through the inverter of the UPS.

10.3.1 Off-line, Preferred UPS

The block diagram of the major component of this type of UPS is shown in Fig. 10.6. Independent battery charging and inverter circuits are used. A regulated ac voltage is supplied to the load using an automatic voltage regulator (AVR). Normally, the phase control technique is used to control the ac voltage. The same devices of ac regulator act as a static transfer switch S_1. It is a thyristor (SCR or triac) based switch. When the mains supply is available, battery (Ni–Cd, Pb–

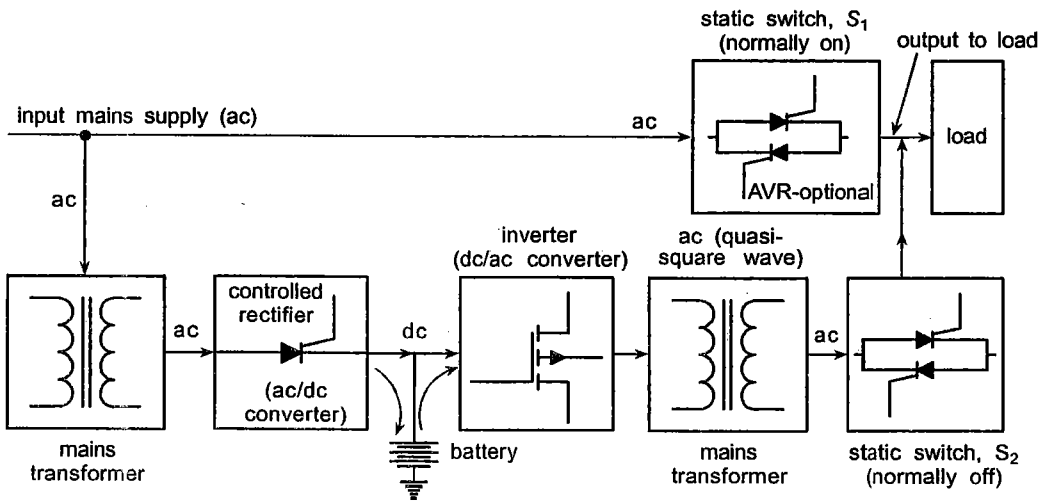


Figure 10.6 Block diagram of an off-line preferred UPS.

acid, etc.) is charged through an ac-dc converter and a charge controller. During power failure, static switch (S_2) operates and battery supplies power to the load through PWM inverter. Normally, single-pulse, quasi square-wave ac voltage is generated by an inverter of off-line UPS. The changeover of the supply from S_1 to S_2 should complete within 1/4 cycles so that the operation of the load is not disturbed. The back-up time depends upon the battery capacity and its charge condition prior to the power failure. For a reliable operation, one switch is turned on while the other switch is turned off. This is necessary for re-switching of S_1, when the power supply is restored. Because a thyristor or an SCR based static switch while conducting, takes about half-cycle to turn-off (by natural or line commutation at the end of each half-cycle). The transfer of power from inverter to mains or vice versa is not instantaneous. Therefore, MOSFET/IGBT based fast microelectronic switches are available for instantaneous or fast transfer. *Alternatively, two MOSFET/IGBT can be connected back-to-back in series. However, it increases the cost of the UPS.

10.3.2 Off-line, Interactive UPS

The block diagram of an off-line, interactive type UPS is shown in Fig. 10.7. The power is supplied to the load through the static transfer switch (S_1), the line conditioner and an automatic voltage regulator (AVR). Normally tap-changer arrangement is used in AVR. A power conditioning unit (PCU) or a inverter/battery charger unit works as a converter-rectifier (ac-dc). When the input mains supply is available, it charges the battery through the charge controller. In the event of power failure, S_1 turns off. Now PCU starts working as an inverter, feeding the load. It is

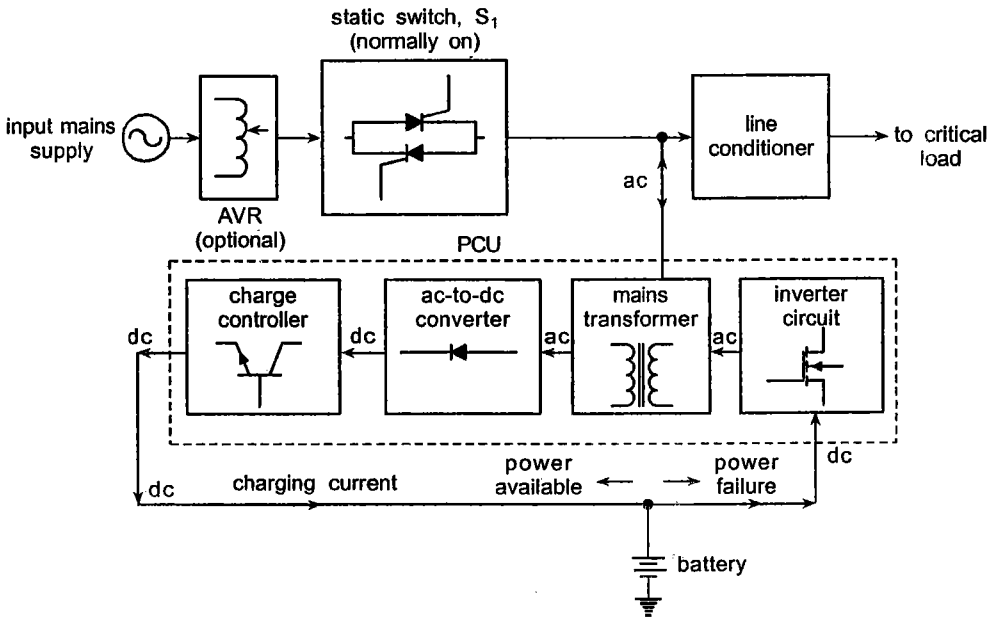


Figure 10.7 Block diagram of a low cost off-line interactive UPS.

*Refer to Fig. A10 in Appendix.

the cheapest UPS, where instead of an independent charging circuit, an inverter cum charger circuit is used. Actually, the mains-frequency transformer is common in charing and inverter circuits. Thus the cost and size of the UPS reduces.

10.3.3 On-line Preferred UPS

In this type of UPS system, no changeover is required (Fig. 10.8). In addition to the charging of a battery, the mains supply power to the load through the inverter continuously. As soon as the mains are disconnected, or power failure takes place, the battery instantly supplies the power to

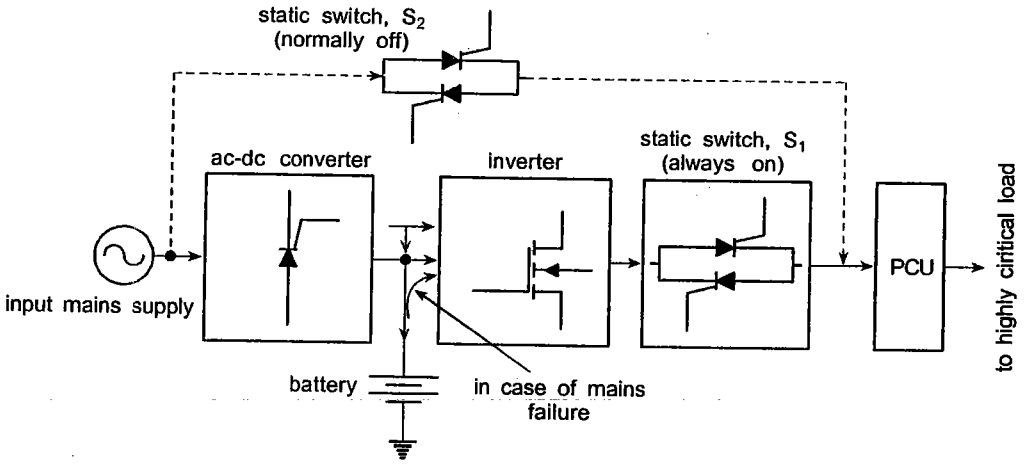


Figure 10.8 Block diagram of an online preferred UPS.

the load. Therefore, power supply to the load continues without any interruption. The proper control of multiple-pulse PWM inverter provides a perfect sinusoidal stabilized ac supply to the load. In the event of inverter failure, the mains can be diverted to the load through the static switch (S_2). Similarly in case of overload, short-circuit or fault condition of load, S_1 turns off and the supply is disconnected to the load. It is called *shutdown of UPS*. In this UPS, the power rating of the ac-to-dc converter (charger circuit) is large, as it has to supply full power to the inverter as well as an additional power required to charge the batteries. Normally, a PCU is used to obtain clean power. The distortion in the voltage waveforms (THD) is normally less than 5%. Moreover, instead of a linear power supply (using transformer with SCR bridge), a MOSFET/IGBT based dc-dc converter is also used to charge the battery and to supply dc power to the inverter circuit. It reduces size and weight of UPS and the input line power-factor greatly improves.

10.4 STORAGE BATTERIES

A *storage battery* is a very important part of inverter systems. It is a work horse of the standby power supply and UPS. For low power and short back-up period, sealed maintenance-free (SMF)

batteries are used. Although, SMF batteries are costlier in comparison to the normal lead-acid batteries but SMF batteries have longer life (about 4–6 years). While lead-acid batteries are commonly used for high power and longer back-up periods. These are both parallel plate type automotive batteries as well as tubular batteries. The capacity of batteries is expressed in ampere–hour (AH) rating. It is a product of constant discharge current and the duration after which batteries voltage falls below the final discharge voltage (V_{dis}). Normally, a term, C/10 is used for it. C/10 stands for capacity/10 or AH rating/10, which represents a current (AH/10) for 10 hours causing the battery to reach V_{dis} level. For tubular batteries and batteries for electric vehicles for high-density energy storage/recovery system), C/4 and C/3 terms are used, respectively. It represents a higher allowable limit (AH/4 or AH/3) for a fast release of energy in 4 and 3 hours, respectively. The depth of discharge (DOD) is also an important term that is related with the life of batteries. For inverter/UPS operation, C/10 rating is used for charging and discharging (or release of energy). For example, a 12-V, 180-AH battery can be charged at 18 A for 10 hours and accordingly the stored energy can be tapped from it at the most, at the same rate (maximum 18 A) and up to the same period (maximum 10 hours). In this case, DOD = 10% (18 A is 10% of 180-AH rating). An increase in charging current (for quick storage) and discharge current (more power tapping) cause heating of the plates or tubes of the batteries. It reduces its life cycle (number of charging and discharging cycle). Moreover, it is evident from Fig. 10.9 that a reduced depth of discharge (also charging) increases the life of batteries. Tubular or semi-tubular lead–acid batteries have better life than its counterpart (automotive batteries with parallel plates). However, different types of batteries are available and under development for high-specific energy (Watt-Hour/kg). These are specially being used for electric vechiles (EV) but their costs are high. Apart from lead–acid (specific energy = 45 WH/kg) and nickel–cadmium (60 WH/kg), these are nickel–iron (60 WH/kg), sodium–sulphur (130 WH/kg), sodium–nickel–chloride (120 WH/kg), nickel–zinc (80 WH/kg) and lithium–aluminum–iron–(di)–sulphide (120 WH/kg), etc.

Fuel cell based EVs are also being used where a fuel cell converts chemical energy from oxygen and hydrogen directly into electric energy. Similarly high-speed flywheels are also being used as energy storage unit.

Proper selection of battery and its capacity for particular applications (inverter, UPS, etc.) depends upon the nature of load, capital investment, back-up period, efficiency of inverter, etc.

Example 10.1 Two 12-V, 180-AH, 25-plate automotive batteries are supplying power to a load through a dc-to-ac PWM inverter. Find the maximum allowable or safe power that can be supplied from the batteries.

Solution According to the C/10 formula, the maximum sustained current released from the batteries should be 180 AH/10 = 18 A. Therefore, the maximum sustained power supplied by the batteries

$$P_{max} = 2 \times 12 \text{ V} \times 18 \text{ A} = 432 \text{ W}$$

The back up period will be 10 hours. However, higher power can be tapped from the batteries at the cost of its life (see Fig. 10.9).

Example 10.2 Design a standby inverter/UPS based power supply for 230-V, 2.5-kW, 50-Hz, 0.8-PF load for a half-hour back-up period. The input dc bus voltage is 120 V.

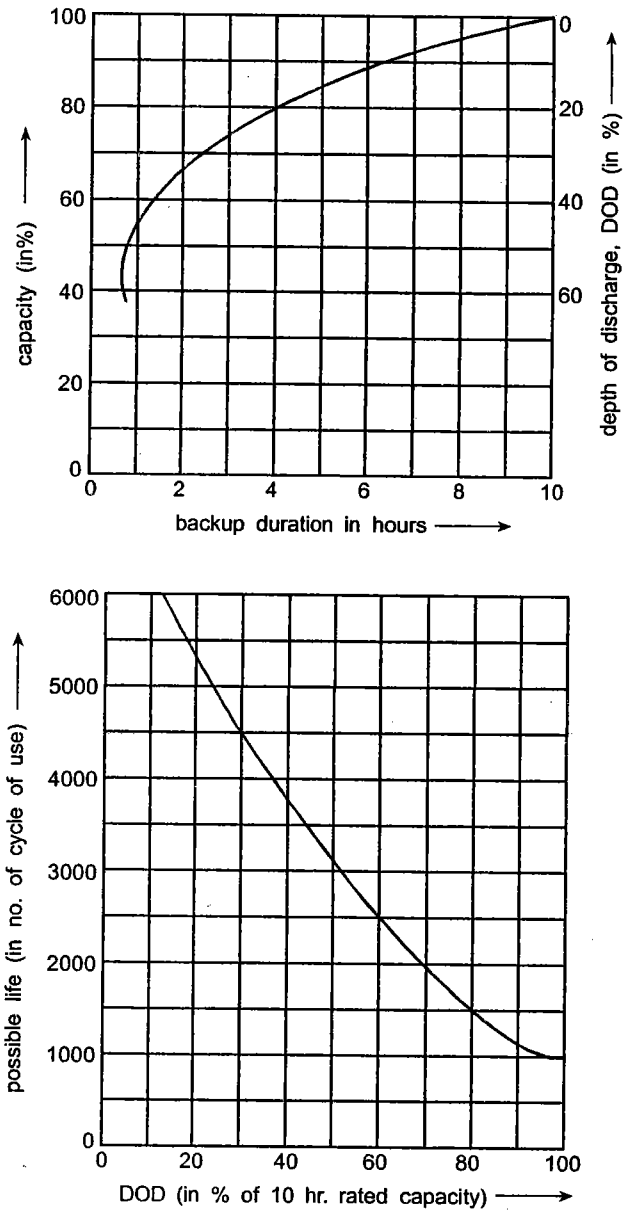


Figure 10.9 Characteristics of lead–acid batteries (both plate and tubular type).

Solution The required kVA rating of the inverter = kW/PF = 2.5/0.8 = 3.125 kVA. Let the efficiency of an MOSFET/IGBT based inverter is 85%. The power supplied by the battery is the input to inverter, which is given by

$$P_{bat} = \frac{kW}{\eta} = \frac{3.125}{0.85} = 3.677 \text{ kW} \cong 3.7 \text{ kW}$$

Let ten storage batteries of 12 V each, are connected in series, then the dc bus voltage = 10 × 12 V = 120 V. The output current of batteries = 3.7 kW/120 V = 30.8 A.

According to the C10, each battery should have 30.8 A × 10 H = 308 AH capacity. Therefore, lead–acid (automotive, parallel plate type) batteries can be used. Normally, it is available in 180-AH, 150-AH, 120-AH, 100-AH, and 80-AH capacities. Therefore, instead of one, two batteries of 12-V, 150-AH capacity (2 × 150 AH = 300 AH) can be used in parallel or two parallel strings of 10 batteries each, can be used. Then total number of batteries will be 20. Total cost of batteries @ Rs. 4000 for 150-AH lead–acid battery = 20 × 4000 = Rs. 80,000.

Alternatively, ten tubular lead–acid batteries with 120-AH capacity can be used (C4 = 120/4 = 30 A). Total cost of batteries @ Rs. 6000 = 10 × 6000 = Rs. 60,000. Apart from the cost difference, tubular batteries have a longer life and more suitable for deep discharge (more release of energy).

10.5

SWITCHED-MODE POWER SUPPLIES (SMPS)

For medium to high power applications and for special applications like power supply of computers, instead of linear power supply, an SMPS is used. The SMPS was first developed in 1960 by NASA (USA) for space applications. Low-heat dissipation, high efficiency, small size and low weight of such converters offer the primary advantages. A linear power supply has 6 to 7 times size (and weight), 2 to 3 times lower efficiency and 3 to 10 times cost in comparison to its SMPS counterpart of the same rating. Highly efficient (99%) dc-to-dc converters are practically being used in EV. Now, it is invariably used in all types of systems, requiring regulated dc power supply. An SMPS with 11000 A current rating is available in the market.

The basic building blocks of an SMPS are shown in Fig. 10.10. The input to the switching device is unregulated dc, which may be available from ac-dc rectifier (converter) and filter circuit. This dc voltage supply is chopped at high frequency to take up the fluctuations in the input voltage or the load conditions and to step-up or step-down the output voltage in comparison to the input voltage level. The output voltage signal is sensed using a control circuit and is fed back to the chopper to adjust the duty ratio (time ratio, i.e. PWM control) to get a constant smooth dc voltage output. The high frequency chopping is done so that cheap, light weight and efficient filter elements can be used to eliminate the ripples in the dc supply. Normally, a high-frequency, ferrite-core transformer is used, for isolation between input and output and among the different isolated output voltage of different level. It offers advantage of negligible hysteresis-loss because of almost linear B-H curve (thin hysteresis loop of ferrite). The advantages of an SMPS are:

- High efficiency (practically negligibly small power loss)
- Compact (light in weight and small in size)
- Ripple-free output (almost constant load current)
- Noiseless output (switching frequency above acoustic range ≥ 18 kHz)
- Electrical isolation (using transformer)
- Several isolated outputs and different voltage levels.

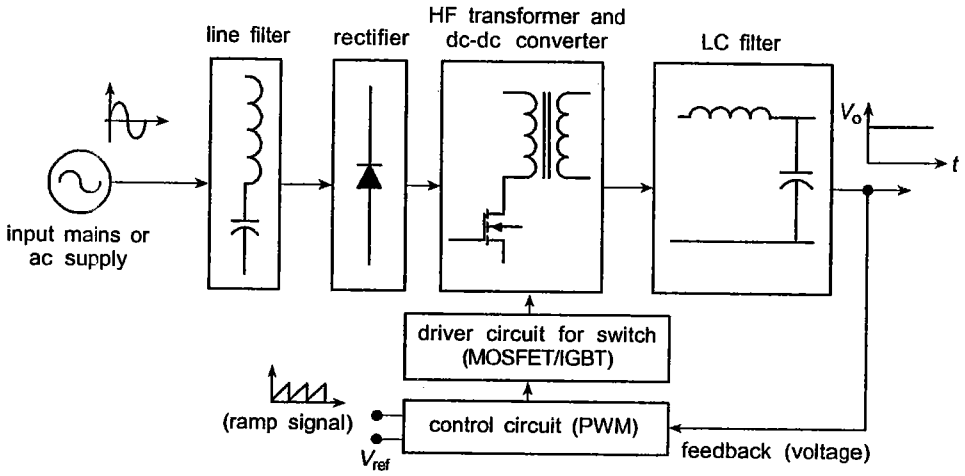


Figure 10.10 Block diagram of an SMPS.

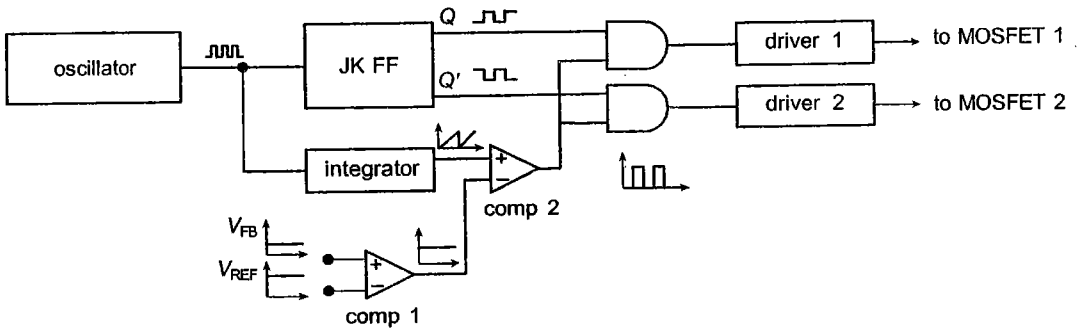
CONTROL METHOD

A feedback controlled dc-to-dc converter operates at a high frequency for an output dc voltage control. This is normally a forward or buck converter. From a fixed dc input voltage (V_i), adjustable output voltage (0 to V_i), can be obtained. When the switch is on, energy transfers from the dc source to the load through LC filter. During the off period, the load current, i_o, flows through the load and a free-wheeling diode. It may be continuous and discontinuous. For low-power applications, single ended, flyback converters are used. For high-power applications, balanced isolated converters are used.

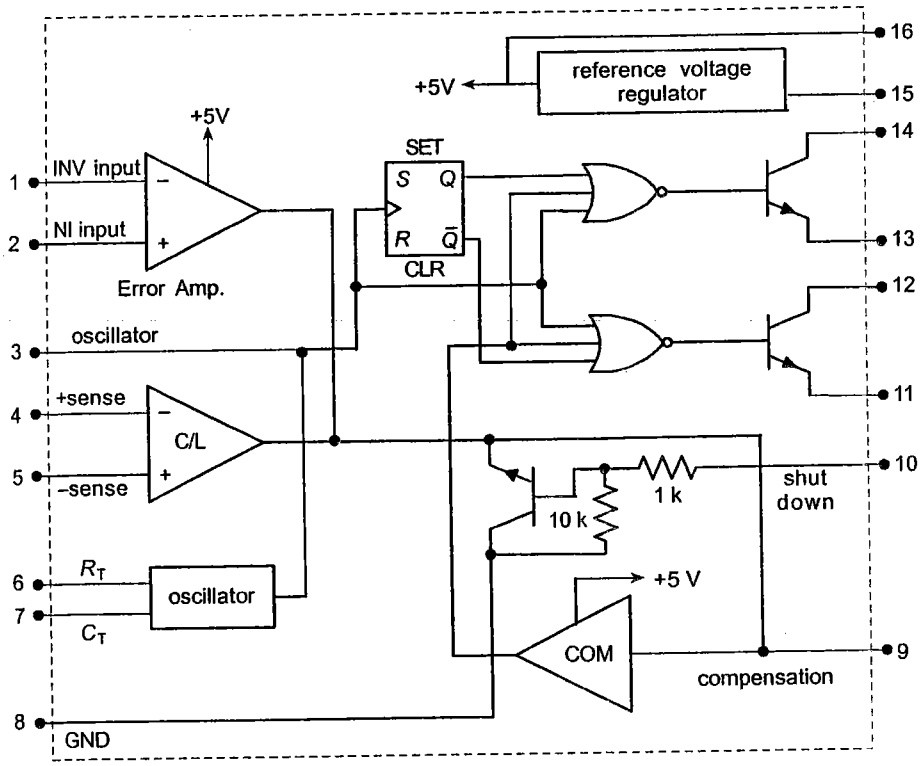
Flyback converters are used in buck-boost or in boost (or step-up) mode. An inductor choke (with air gap) is used to store energy in one part of the cycle and it releases the energy in another part. When the current passes through the primary windings, the secondary winding current is blocked by a diode. Therefore, works as an inductor (not as a transformer) and due to the presence of air gap, it stores maximum energy. When the switch is turned off, negative voltage (Ldi/dt at the secondary) due to reducing current of primary (di/dt negative) or collapsing field in the core, causes flow of the current in secondary winding. In this way, the energy transfer takes place from primary to secondary and the core does not get saturated.

A large number of IC is available for control of flyback and dc-to-dc converters. The basic principle of PWM is used to control the output voltage. These IC are used for both dc voltage (chopper and dc-dc converter) and ac voltage (dc-ac inverter). The duty-ratio or pulse width is controlled while the frequency is kept constant. Figure 10.11 shows the block diagram of the PWM control scheme, which is normally implemented in different custom-built IC. The basic principle can be explained with the help of the block diagram (Fig. 10.11).

A toggle or JK flip-flop (FF) reduces the frequency of the square-wave oscillator to a half. Therefore, Q and Q' remain high, alternately, for a half-cycle of the output voltage. The integrator generates a ramp voltage corresponding to the signal of the square wave. The comparator, COMP1 is a difference amplifier. It compares and amplifies the feedback voltage (V_{FB}). Its output is compared with the ramp signal in level detector, COMP2. The duration, for which the negative ramp signal remains high (with respect to the negative output of the COMP1), the output of



(a) PWM control scheme

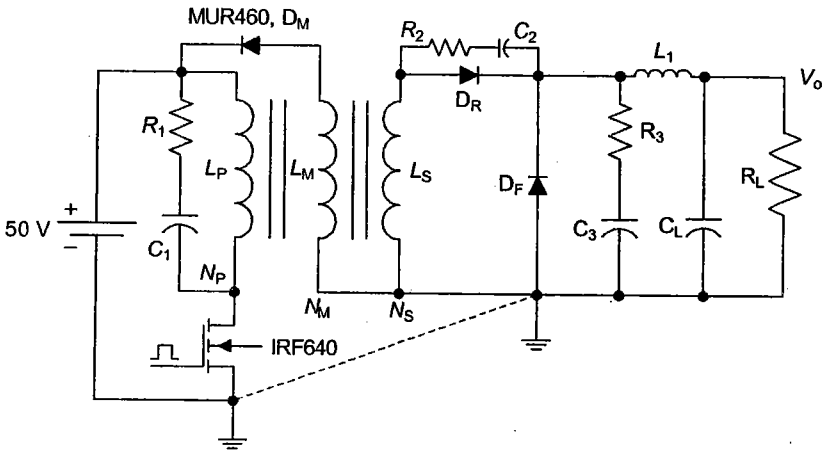


(b) Details of a PWM IC SG 1524

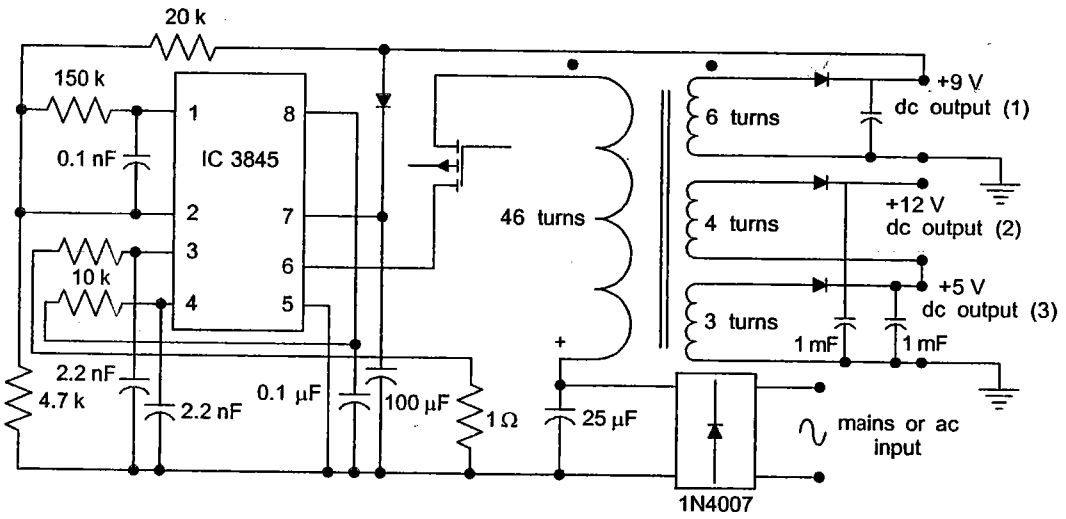
Figure 10.11 Block diagram of PWM control scheme.

COMP2 becomes high. Therefore, the variation of the output level of COMP1 changes the duty ratio of the pulse width of COMP2. With the help of two AND gates, alternately, these signals reach the driver 1 and driver 2 circuits for which Q and Q' become high, respectively. Figure 10.12 shows IC based SMPS and flyback converters.

Although the basic principle remains same but the PWM IC varies over wide range with respect to facilities and to meet special requirements of costumer and applications. There are



(a) A typical flyback converter circuit



(b) A flyback converter based SMPS

Figure 10.12 IC based SMPS and flyback converters.

several other facilities that are also incorporated, e.g. soft start, current-limiting protection, short-circuit or shut down and variation of oscillator frequency over a wide range. In case of balanced converters, the same process takes place with isolated output load, using a transformer.

10.6 POWER FACTOR CORRECTORS

The conventional diode or SCR based linear ac-to-dc converters are extensively used in UPS and resonant dc/ac link converters. However, these converters suffer from various serious drawbacks. Apart from the low-input power factor and ripples in the output, the harmonics in line current

cause punitive tariffs levied from utilities (e.g. for a converter of above 600-W rating). To overcome these drawbacks, huge passive filters will be required, which increase the size, weight and cost of ac-to-dc rectifiers. Alternatively, a power factor corrector (PFC) converter circuit is used. It is also called *PWM rectifier*, *synchronous link converter* or *synchronous rectifier*. The basic principle of the boost converter type PFC is shown in Fig. 10.13. The input or the line current drawn from the ac source follows the supply voltage (sinusoidal) waveform by PWM control of the switch. Thus the effective input power-factor becomes very close to unity. DC-to-dc converters with 99% PF is commercially available in the market. The pulse-width or the on-period is controlled on the basis of the average or peak value of the input current (i_i). For battery charging applications, the charging is fast as the charging current (output) is continuous over the

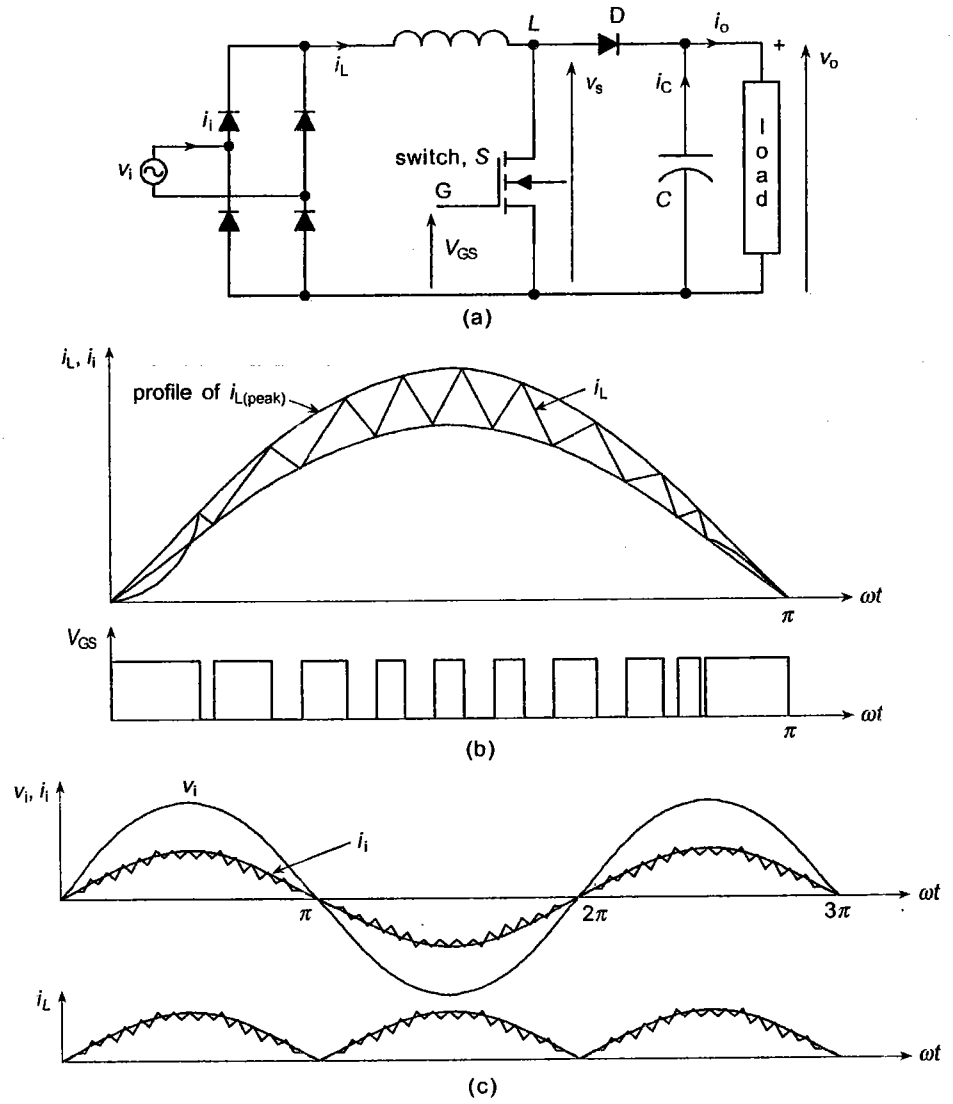
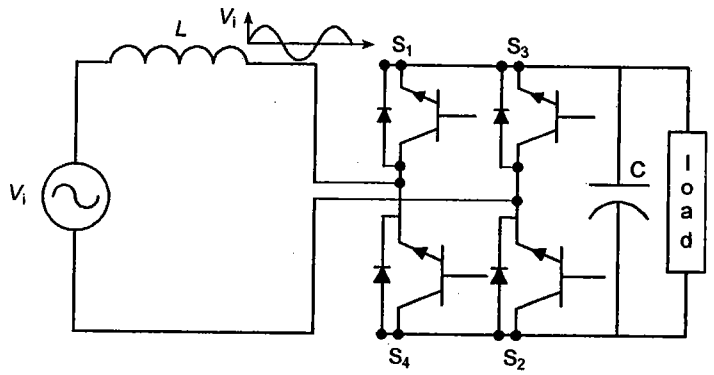


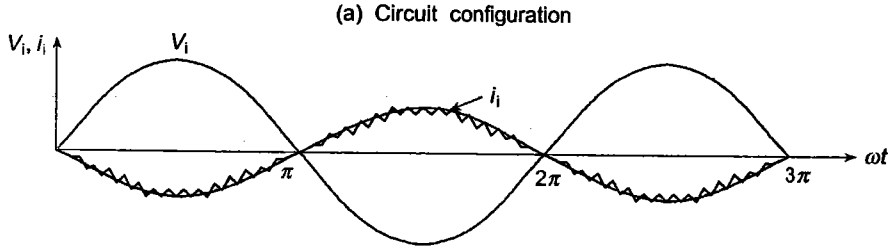
Figure 10.13 A boost converter based PWM rectifier or PFC circuit.

whole cycle. While in case of conventional linear rectifier circuits, the charging current flows only in a part of cycle (when the input voltage exceeds the battery voltage). Thus it takes more time to fully charge the battery.

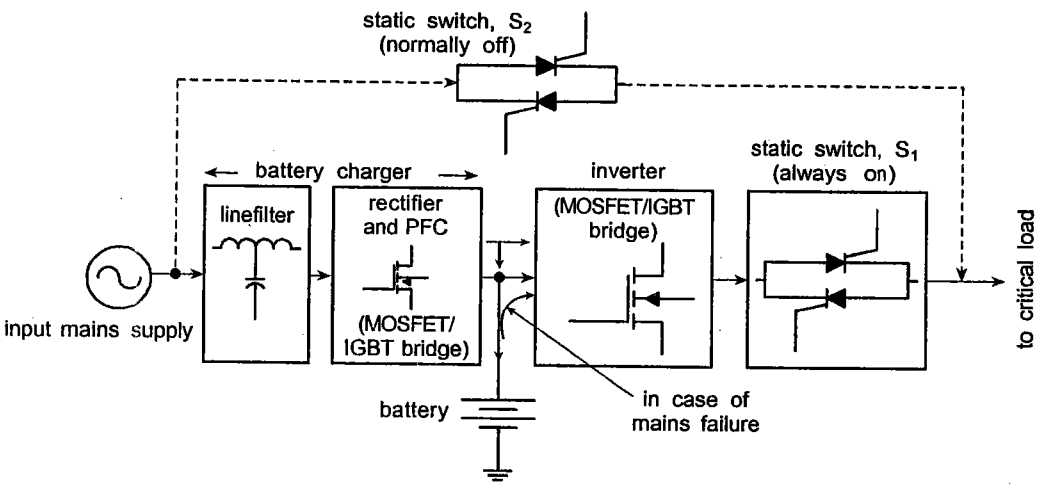
Figure 10.14 shows the application of PFC in a bridge circuit for 180° phase shift of the input current or regeneration condition. The phase angle of the input line current can be adjusted in between from 0° to 180° for a flexible power factor control (FACTS control). The application of a PFC is also shown in an online UPS (preferred type). The use of mains frequency transformer is



(a) Circuit configuration



(b) Phase angle control of input current for regeneration



(c) A battery charger without a transformer in an on-line preferred UPS.

Figure 10.14 Application of bridge PFC.

avoided which reduces the size, weight and cost of the charging circuit of UPS. Moreover, it is also used in resonant dc/ac link converters as discussed in Chapter 9.

10.7

HIGH-POWER PWM AUDIO AMPLIFIERS

The transistors (power BJT or power MOSFET), used in audio amplifiers for public address systems (PAS), operate in active region of its output v-i characteristics. At Q-point, both i_C and v_{CE} are high. Therefore, the power loss in the power transistors (e.g. 2N3055/2N3077 etc.) is significantly high and the efficiency of the amplifier is very poor. The same condition exists in linear dc power supplies, where the transistors of voltage regulator (e.g. IC 7812) operate in active region, as discussed in Section 7.6. In case of high-power audio amplifiers (several kW), the losses in the device (transistors) are unacceptable. The PWM technique is applied to reduce the losses (as the devices do not operate in the active region at all). Figure 10.15 shows the scheme of the PWM audio amplifier. The input audio signal is supplied to a pulse-width modulator circuit, which is a comparator circuit. A carrier signal (normally triangular wave) is compared with the input audio signal. The width of the sampled output voltage (ac) varies according to the magnitude of the input audio signal. The positive part of this signal is supplied for the gate of the upper-power MOSFET of the half-bridge, through the driver circuit (H_{input} of IR2010). Similarly, the negative part of the signal is applied to L_{input} for the lower-power MOSFET. The amplified output is discontinuous which is smoothened by a filter circuit. Since the frequency of carrier signal is very high (several hundred kHz), the requirement (magnitude) of filter circuit components reduces. Both half and full-bridge circuit topologies are used, as shown in Fig. A14 (in Appendix). Special gate drivers IC IR2010S and IR2013S are available from International Rectifier, which operate up to 400 kHz carrier frequency. IR2013S are normally used for very high power and for IRFP200 series of power MOSFET (e.g. IRFP 260N/254N/264N).

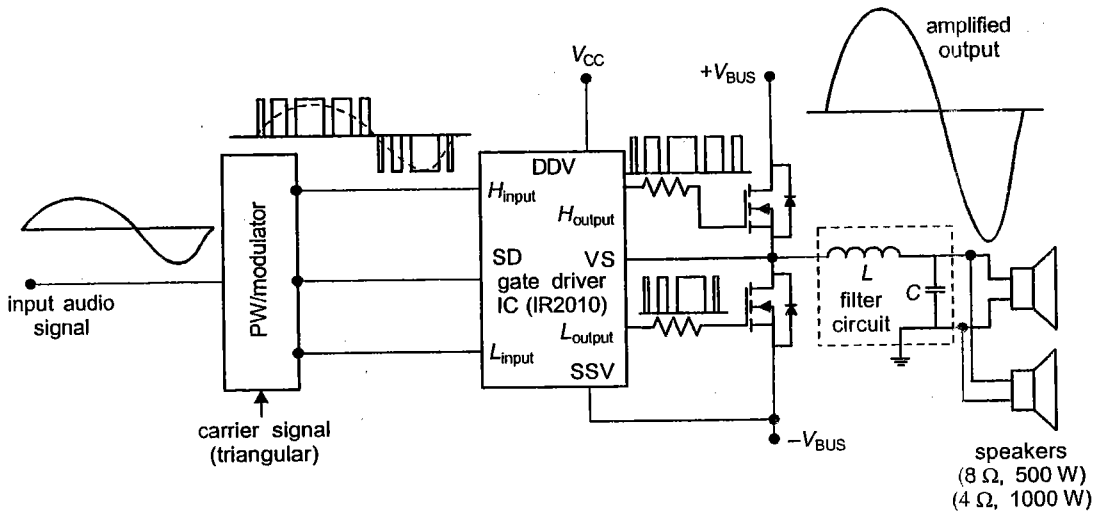


Figure 10.15 Very high power and high efficiency MOSFET based PWM audio-amplifier half-bridge circuit topology (PWM switching frequency up to 400 kHz and maximum modulation index, M = 85%).

SUMMARY

A high-quality clean power (free from spikes, harmonics and abnormal voltage level) is desirable. However, poor quality of power from commercial utility and disturbances in power line are common. Therefore, power conditioners are used to maintain high quality of power which includes ac voltage regulators, voltage spikes suppresors and filters. While uninterruptible power supply (UPS) is necessary for critical and sensitive equipments, e.g. computers and computer based systems, vital communication systems, medical equipments, etc. Both low-cost off-line UPS and online UPS are used. A linear regulated dc power supply has several demerits including low efficiency and high cost, weight and size, etc. Therefore, counterpart switched-mode supplies (SMPS) are used.

The performance of a UPS or a dc-to-ac inverter depends upon the battery storage system. The general performance of batteries and their lifecycle depend upon the nature of charging and discharging. Power factor corrector circuits are used to improve the power factor in UPS and SMPS are also discussed.

REVIEW QUESTIONS AND PROBLEMS

1. Why is an inverter/UPS based stand-by power supply preferred over a diesel-generator set?
2. What do you mean by a clean power?
3. What are the effects of distorted supply voltage waveforms?
4. What are the effects of frequency deviation? How are they removed?
5. Why are off-line interactive UPS cheap?
6. Why are on-line UPS costlier?
7. Why an inverter-battery based stand-by power supply is popular and not an EV?
8. What are effects of quick or fast charging (storage) or high-energy recovery (discharge) from battery?
9. What do you mean by the depth of discharge? How does it affect the life of a battery?
10. Why is a high-frequency transformer used in SMPS?
11. What are the merits of SMPS over its linear counterpart?
12. What are advantages of a unipolar fly-back converter?
13. Why are multiple switches, balanced, isolated dc-to-dc converters used in SMPS?
14. Show the relevant waveforms of a PFC/PWM rectifier with a buck converter. Compare its performance with a PFC, using a boost converter.
15. Find the allowable sustained power output of 12 V, 120-AH tubular battery.
16. What are the maximum back-up periods of 5-kW load, for both lead–acid (parallel plate type and tubular) batteries of the system discussed in Example 10.2? [*Hint:* Total capacity (tubular type) = $10 \times 12 \times 120 = 14.4$ kWH].

11

Device Protection and Magnetic Circuits

11.1 INTRODUCTION

As discussed in Chapter 10, if the power supplied from the power utility is not clean then abnormal conditions exist. Moreover, the load connected to the output of the converter also varies and it leads to overload as well as short-circuit conditions. Therefore, power semiconductor devices experience abnormal conditions both from the input side as well as from the output side or load. There are several requirements for the protection of power semiconductor devices in a circuit. If a device experiences over-load, over-voltage, high-voltage (or current) transients, high-device (junction) temperature or other abnormal operating conditions, the device may be degraded in performance or destroyed permanently. The device should be protected against abnormal conditions for satisfactory and reliable operation so that it faithfully adheres to the specified characteristics of the manufacturer. A fault current can cause a device failure while a transient over-voltage (or noise signal) may cause undesirable device turn-on. It is a normal practice to have some safety margin for selection of device of proper rating, related to the steady-state conditions of power electronic circuit. Further, all power semiconductor devices dissipate power as these are not ideal lossless devices. The heat transfer from the device becomes necessary. Therefore, heat sink and cooling arrangement for devices are employed. Sometimes, it is used simply to improve the performance of the device and efficiency of the converter. The temperature rise of the device (or junction) decreases voltage handling or withstands capability and increases the failure rate. It is important to note that the device failure or damage takes place due to temperature rise and not by heat, current, voltage or power dissipation.

It is evident from the previous chapters that inductors are used in filter, current limit and energy storage/recovery circuits. Similarly, transformers are used in isolating, forced current sharing, phase shifting and impedance matching circuits. Sometimes, the same transformer works as both inductor as well as transformer (flyback converters). Moreover, in case of resonant converters, very accurate value of inductance is necessary to achieve, or to operate near resonance condition. The above deliberations show that these magnetic components are an indispensable part of most of power electronic converters and circuits. As the required properties of these components vary over wide range, the knowledge about their design and fabrication becomes necessary.

11.2

PROTECTION OF DEVICES

A device has to be protected from over-current, over-voltage and noise or voltage transients. However, the most common among them is over-current fault.

11.2.1 Over-current Protection

This is the most common type of fault, the device experiences. This can be mitigated by the use of high-rating devices. However due to economy, the rating of device is chosen according to the normal requirements, not on the basis of the worst case. There are several reasons for over-current in power electronic circuits, which are:

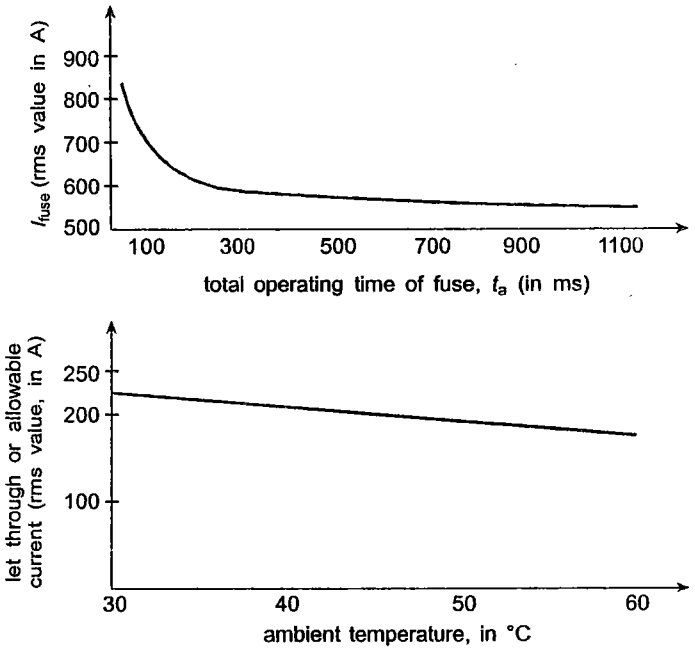
(a) short circuit of the load circuit (which is most common)
(b) sustained overload (due to starting in-rush current or stalled motor in an electric drive system)
(c) conduction of both devices of a leg, in a full- or half-bridge configuration.

Thyristors can be protected by fuse, relay and circuit breaker. Normally, for sustained overload in a close-loop control system, current-level comparators are used for detection and then suppression of gate signals of converter in a fault condition. For a weak supply system, sufficient impedance remains in the fault path and the current can be limited below the multi-cycle surge-rating of a thyristor. Thus the detection of a fault condition from the high-load (or over-load) condition becomes difficult. Similarly, for a negligible fault impedance, the prospective fault current (I_a) is high (Fig. 11.1). It is the fault current that would flow in the absence of a fuse. For a high value of I_a, the rise of fault current is too sharp and the conventional over-current protection scheme would be too slow. Therefore, a high-rupturing-capacity (HRC) fuse is needed to clear the fault within a few milliseconds. It should be noted that the ordinary rewirable fuse link (Kit-Kat) is the cheapest protective arrangement but it is too slow. Miniaturized circuit breakers (MCB) are also used in place of rewirable fuse link (sometimes both are used together). Both of them are suitable for overload or sustained fault current and not for the device protection under dynamic conditions.

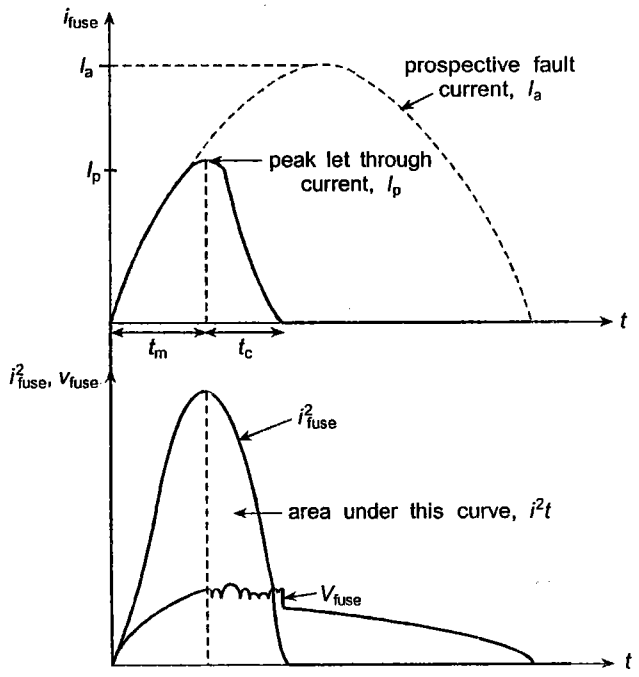
A short-time overload condition is allowed due to economic reasons and therefore power electronic circuits are not designed with device rating corresponding to the overload conditions. The fuse link used could be an HRC fuse or a semiconductor fuse. The cost of a semiconductor fuse is almost 40% of the device protected. As fault current increases, fuse blows and clears fault in a few tens of milliseconds. Even then, HRC and semiconductor fuses are adequate for diodes and thyristors only. For protection of different devices of transistor family (due to their fast-switching characteristics), these fuses do not suffice.

For protecting a device, the fuse can be connected in series with each device and/or with each line terminal. When a fault current flows, the fuse element starts melting due to the prospective fault current (I_a), as shown in Fig. 11.1. At $t = t_m$, melting of fuse element completes and arcing of fuse elements starts. The gradual increase in arcing resistance decreases the fault current and at the end of t_m, the fuse element ruptures itself. Sometimes snap of an inductive current (inductance of source or fault current path) generates spikes of voltage of high magnitude ($v_L = Ldi/dt$). If R is the resistance of the fault circuit, then energy fed to the circuit is given by

$$E = \int Ri^2 dt \tag{11.1}$$



(a) Characteristics of a 200-A rating semiconductor fuse (T350-200)



(b) Operating behavior of a fuse under fault condition

Figure 11.1 Operating characteristics of a HRC/semiconductor fuse.

If R remains constant, then i^2t is proportional to the energy fed at fault condition. The value of i^2t for the melting period (t_m) is called *pre-arcing* i^2t. It is responsible for melting of fuse. The *total* i^2t corresponds to the total operating time of the fuse (t_a), which is equal to $t_m + t_c$. Normally, manufacturers specify both pre-arcing as well as total i^2t value (for about 10 ms or half-cycle basis). For a short melting period (less than one millisecond), pre-arcing i^2t is only function of I_a and is independent of the supply voltage. The fuse coordination is done on this basis. However, if melting time is more than 5–10 ms, the time-current characteristics and total i^2t are normally used for fuse coordination. The pre-arcing i^2t varies considerably with system voltage, fault impedance (or current level), power factor of fault impedance and instant of initiation of fault on voltage wave. Thus total i^2t increases with increase in system voltage and decreases with supply frequency. Moreover, the fuse allowable current (let-through current) is rated in rms value. During the steady-state condition, the fuse must not operate in excess of its rms rating, while the peak let-through current (I_p) may be as high as 20 times the rated rms value of fuse current (Fig. 11.1).

A proper coordination between fuse and the device to be protected is important. However, difficulties arise in matching them because both have different thermal and electrical properties. However, the objective of the coordination is to ensure that the fuse let-through energy under fault condition should be less than the tolerable energy of the device (I^2t rating). Moreover, the fuse must continuously carry the device-rated current. Also, the peak arc voltage must be less than the peak voltage rating of the device (e.g. V_{DSM} of an SCR). Normally, a snubber circuit across the device protects it from high spark voltage generated by rupturing fuse at fault condition.

11.2.2 Over-voltage Protection

Over-voltage is one of the main causes of the device-failure. It may lead to mal-operation (undesirable turn-on or permanent destruction of the device due to breakdown by the reverse voltage). It is either a repetitive pulse or one-time impulse. Although it appears for a very short period of time (few micro-seconds) but it may result in a localized high-power dissipation in the device (formation of a hot spot), which could be fatal. Moreover, the voltage transient may inject noise into the low-voltage control logic circuit, causing spurious faults. Thus, over-voltage protection is achieved by diversion or dissipation of the impulse energy in an additional transient absorption circuit such that the device voltage does not rise above the safe voltage limit. A transient voltage pulse can be suppressed by various methods:

(a) *Transient voltage attenuation:* An LC low-pass filter can be used to block high-frequency voltage spikes.
(b) *Snubber circuits:* It offers a low-impedance path or alternative path for the current produced by spikes. Therefore the harmfull effects of spikes do not reach the load.
(c) *Voltage limiting devices:* A number of non-linear impedance devices are used, e.g. metal-oxide varistors (silicon-carbide and zinc-oxide varistors), reverse-selenium diodes and zener (or avalanche) diodes.

11.2.3 Crowbar Protection Circuits

Rewirable fuse links, HRC fuses, MCB and over-current relays or switchgears are not suitable to protect sensitive devices and systems. It is evident from the inverse current-time (or inverse definite minimum time, IDMT) characteristics of a fuse that operating time is highly dependent on the magnitude of fault current (Fig. 11.2). Thus for a slight over-load (or over-voltage) condition, a fuse

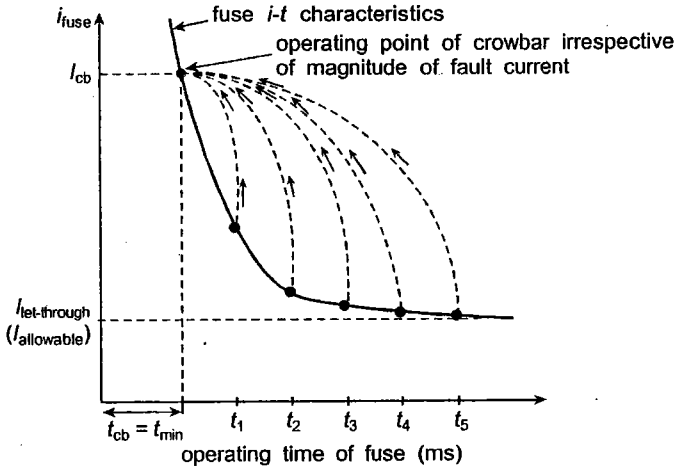


Figure 11.2 Operating characteristics of a crowbar circuit.

takes much more time (t_5) to blow than for a heavy fault current condition (t_1). With the help of a crow-bar circuit, both over-current and over-voltage protection are possible for both ac and dc circuits. An HRC fuse or a fast acting circuit-breaker is used with crow-bar SCR, as shown in Fig. 11.3. In this case (crow-bar arrangement), whenever a fault condition occurs (whether fault current is high or low), the control circuit senses and immediately gives trigger signal (trip signal) to

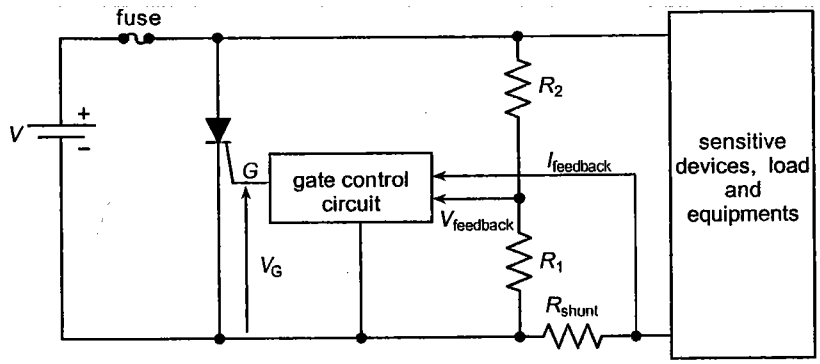


Figure 11.3 Crowbar protection scheme.

the crowbar SCR. The source is short circuited by very low impedances of fuse and SCR. Therefore, an enormously high short-circuit current (I_{cb}) causes blow of fuse and fast interruption of supply to the sensitive load circuit (independent of the magnitude of the actual fault or overload current). Thus the fuse operating time is very low (t_{cb}), almost equal to the definite minimum time.

11.2.4 Noise Protection

A power electronic circuit may receive radio-frequency interference (RFI) noise from the neighbouring systems. It could be a radiated RFI or conducted RFI. A sudden change in current (e.g. phase control of resistance load) causes large di/dt, hence large $d\phi/dt$ which induces emf in

neighbouring circuits (RFI). Its effect could be a simple undesirable switching to a device/system failure. The conducted noise can be attenuated to a safe level with the help of filter circuits, as discussed in Chapter 10. A good circuit layout and construction greatly reduces radiated RFI, e.g. minimum connection wires and loops, twisted wire pairs, placement of magnetic components, use of ground potential, shielding of whole circuit arrangement etc. Also zero-voltage switching (ZVS) and zero-current switching (ZCS) minimize *di/dt*, thus reducing radiations. However, it is always desirable that the device and the power electronic circuit should withstand certain noise hazard level. It is called *electromagnetic compatibility* (EMC) of the device and converters. Moreover, these converters should radiate minimum noise (electromagnetic interference, EMI). Therefore, manufacturers of power electronic systems specify these ratings.

11.3 THERMAL PROTECTION AND HEAT SINKS

All power semiconductor devices dissipate power. The power is generated in the device due to on-state, off-state and switching transition conditions. However, the switching power loss is considerable which is due to slow or non-simultaneous change of device voltage and current during turn-on and turn-off processes. The reliability and life expectancy of the device depend upon the maximum temperature experienced by the switching-junction. If the temperature exceeds, the junctions are lost (specially those blocking) due to thermally generated excess carriers (electron-hole pairs). In other words, the intrinsic carrier density (e.g. 10^{10} atoms/cc) of the device greatly exceeds (10^4 to 10^8 times) the doping density near junctions (e.g. 10^{18} atoms/cc). Thus the whole device becomes flooded with carriers. The depletion regions (where potential barrier forms) loses its characteristics and is shorted by excessive intrinsic carriers. Thus the device failure takes place; it could be of a permanent or temporary nature.

Although the intrinsic temperature of the device is quite high (e.g. 280°C for a silicon diode) but the maximum specified temperature of a data-sheet given by manufacturers is quite low (150°C) for safe and reliable working of the device. Moreover, the reliability (expected operating life-time) reduces significantly above 50°C. It reduces to half for each 10° to 15°C temperature rise at this condition. Therefore, metallic heat radiators are used to cool down the device body or surface, and hence the junction of the device. Blackened surface of heat sink increases the radiation thus improves cooling. For a bright, shiny or smooth surface, radiation decreases. Therefore, a derating of 10–15% is adopted. Similarly, heat convection by forced air circulation or cooling by liquid circulation improves heat transfer drastically. In general, this type of arrangement is almost necessary for devices of transistor family.

11.4 COOLING OF DEVICES

When a device conducts, a full-load current passes through the device and a small voltage appears across it. Thus power loss in the device due to on-state voltage and current takes place. Similarly during off-state, only small leakage current flows while the input voltage appears across the device. The power loss in the later condition is smaller. During the switching period, current

through the device and voltage across the device do not vary suddenly, but these take a finite time. As no device works as an ideal switch, the switching power loss becomes significant. For lower frequency below 100 Hz, it can be ignored. For fast-recovery diodes, it can be neglected even up to 1 kHz. Normally, the turn-off loss is more significant than that of turn-on, because the turn-off switching time is much more than the turn-on switching time. It generates heat at the blocking junction of the device. It may lead to increase in junction temperature beyond the permissible limit. Failure or degradation of device will occur if this heat is not removed from the junction. The damage is caused by temperature and not by voltage, current or heat. Therefore, a suitable cooling system (heat sink) is necessary to transfer the generated heat from the switching junction. Normally, 125°C junction temperature is used for the worst-case design. However, a highly reliable cooling system is designed for 100°C (or even below than it). Since the switching junction is inside the casing of the device, the generated heat transfers from the switching junction to the casing, casing to the heat-sink and finally from the heat sink to the atmosphere. For cooling of the devices, heat sink of standard sizes are commercially available or else it can be fabricated/moulded according to the requirements. Further, these heat sinks may be cooled down by natural air convection, forced air-cooling (using a fan), or by circulation of a coolant (liquid) in the heat sink. Apart from conduction with heat sink, cooling of devices (or casing) by radiation and convection are obvious.

11.4.1 Heat Flow by Conduction

Normally, heat flow takes place from the device to the atmosphere through different materials of different shape, size and thermal conductivity. All these materials, therefore, have different thermal and electrical properties. In general, heat flow takes place from the switching junction of the device to its casing and from casing to the heat sink through conduction. Since, there is similarity in electrical power flow in an electrical circuit to the heat flow in a medium, Ohm's law is often used for the model of heat flow. The temperature difference (ΔT), thermal resistance (R_θ) and the average power dissipation (P_d) are correlated with voltage drop (ΔV), electrical resistance (R) and electrical current (I), respectively. Thus the process of heat transfer is more conveniently analyzed in terms of thermal resistance. The thermal resistance between two points having temperatures T_1 and T_2 is given by

$$R_{\theta(1\text{-}2)} = \frac{T_2 - T_1}{P_d} = \frac{\Delta T}{P_d} \text{ °C/W (or K/W)} \tag{11.2}$$

where P_d is the rate of heat transfer, which is power dissipation of the device. Also, heat transfer or heat flow in a solid from a high-temperature end to a low-temperature end by conduction, under steady-state condition, is given by

$$P_d = hA\Delta T \tag{11.3}$$

and from (11.2) and (11.3),

$$R_{\theta(1\text{-}2)} = \frac{1}{hA} = \frac{w}{kA} \tag{11.4}$$

where A is the area involved in the heat transfer (or heat flow) and h is the heat transfer coefficient (it depends upon the heat transfer mechanism used and various factors involved in that particular system), k is the thermal conductivity and w is the thickness of the medium.

The heat generated due to average power dissipation of the device has to transfer from the junction to the atmosphere. Figure 11.4 shows the equivalent circuit with thermal resistances between junction to casing or body of the device ($R_{\theta(j\text{-}c)}$), casing to heat sink or cooling structure/ arrangement ($R_{\theta(c\text{-}s)}$) and heat-sink to atmosphere or open air, ($R_{\theta(s\text{-}a)}$). $R_{\theta(c\text{-}s)}$ depends upon package type of the device, mounting pressure as well as thermal-conducting grease (silicone grease) and/or thermal-conducting insulators (mica sheet, taflon, etc.) between casing and heat-sink. In the presence of silicon–grease, $R_{\theta(c\text{-}s)}$ decreases to 30% (approximately) and in the presence of mica sheet etc. it increases almost three times. $R_{\theta(s\text{-}a)}$ depends upon size, shape and cooling methods (e.g. natural or forced cooling) of heat sinks.

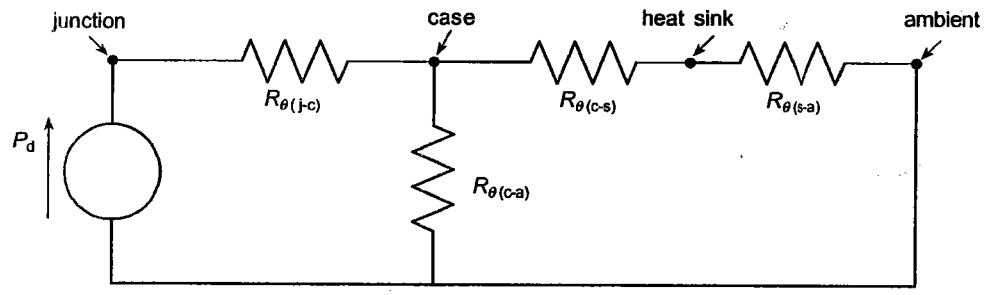


Figure 11.4 A thermal equivalent circuit for heat flow of a device.

11.4.2 Thermal Compounds and Insulators

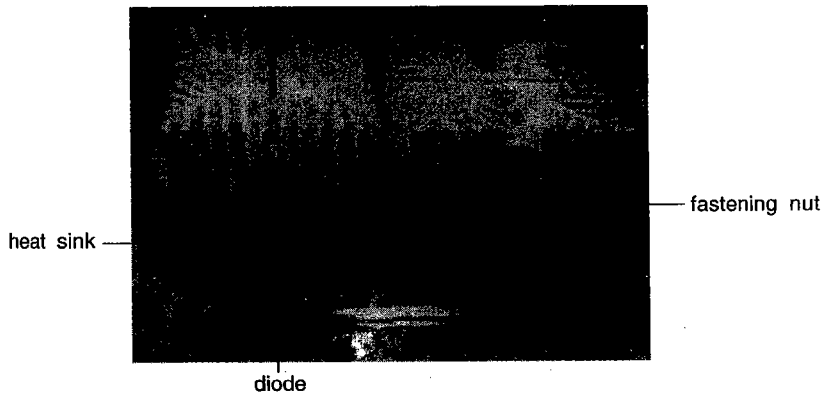
To improve contacts hence heat transfer, 'thermal joint compounds' or grease are used to fill air films, voids, scratches and imperfections between mating surfaces. The thermal compounds are a formulation of fine zinc particles in silicon oil.

Table 11.1 shows the effect of the compounds on $R_{\theta(c\text{-}s)}$. In case of lubricated (lubed) heat sinks, the $R_{\theta(c-s)}$ reduces drastically. The use of the compound is more effective when insulating washer is used. Normally it is made of mica, Teflon or Naylor which are thermally conducting and electrically insulating.

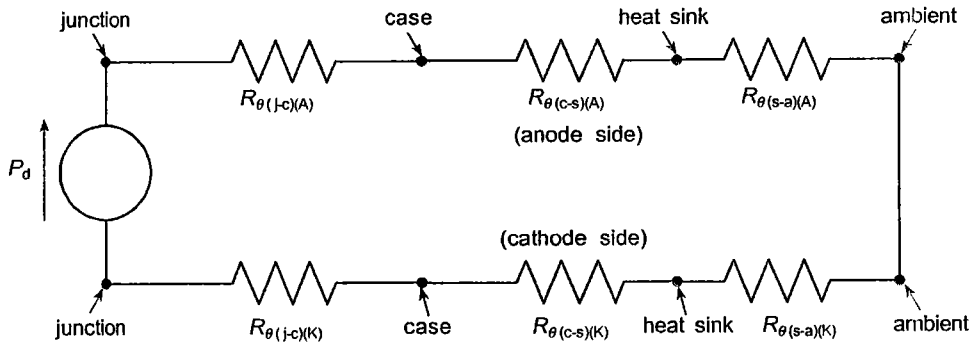
Table 11.1 Variation of Thermal Resistance with Casings

Casing package type	$R_{\theta(c\text{-}s)}$(°C/W) *(metal to metal)*		$R_{\theta(c\text{-}s)}$(°C/W) *(with insulator)*	
	Dry	*Lubed*	*Dry*	*Lubed*
T0-3	0.5	0.2	1.3	0.36
T0-66	1.5	0.5	2.3	0.9
T0-220AB	1.2	1.0	3.4	1.6
T0-126	2.0	1.3	4.3	3.3

In general, the surface of insulator is uneven. The use of thermal compounds reduces $R_{\theta(c\text{-}s)}$ to a half or one-third. Hockey-puck or press-pack type devices offer better cooling structure as heat transfers from both the sides of the device (e.g. anode and cathode), as shown in Fig. 11.5. Different custom-built, finned-type, aluminium heat sinks are commercially available. Fins increase the overall surface area, therefore, thermal impedance decreases. Figure 11.6 shows different shapes of custom-built heat sinks. Figure 11.7 shows the variation of $R_{\theta(s\text{-}a)}$ for different length (l) of the shape given in Fig. 11.6a.



(a) Two 5800 A, 400 V, mains frequency, hockey-puck diodes with heat sinks at both sides of the devices. (compare the size with the ball-pen in foreground)



(b) Equivalent thermal resistance circuit for a hockey-puck device

Figure 11.5 Hockey-puck or press-pack type devices.

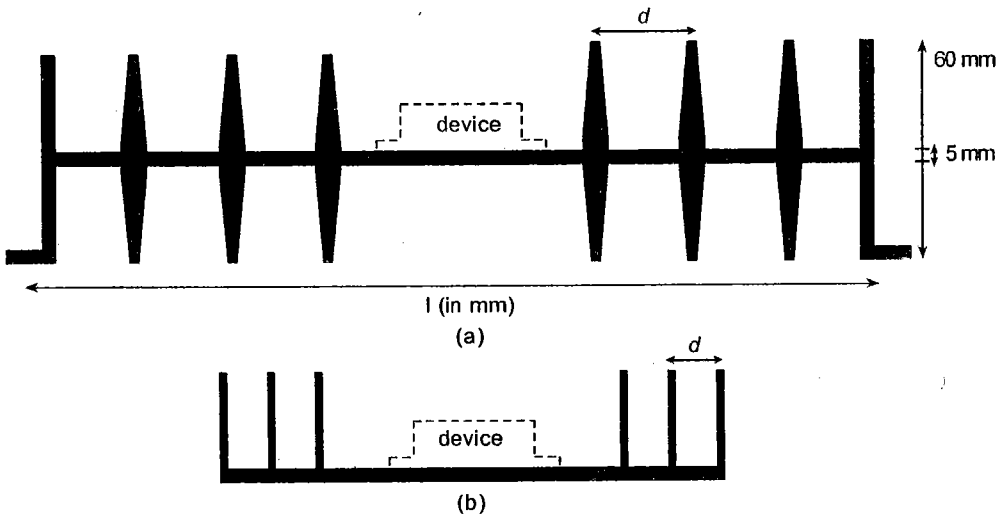


Figure 11.6 (*Cont.*)

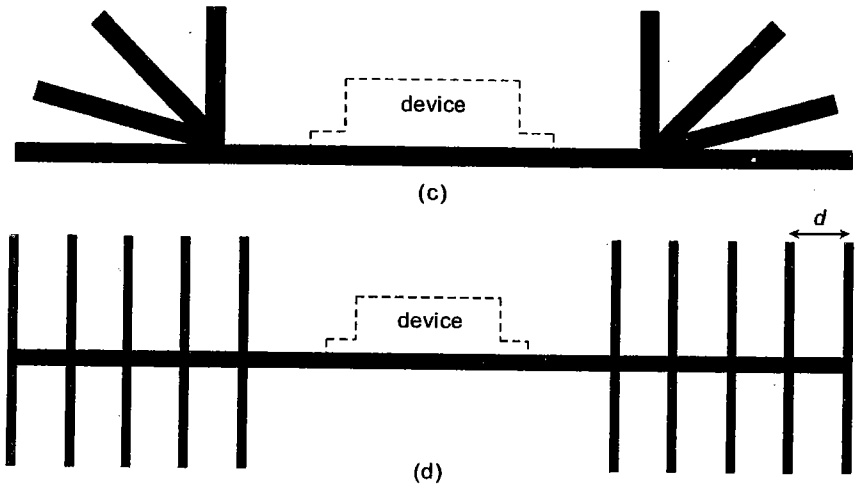


Figure 11.6 Different types of heat sinks.

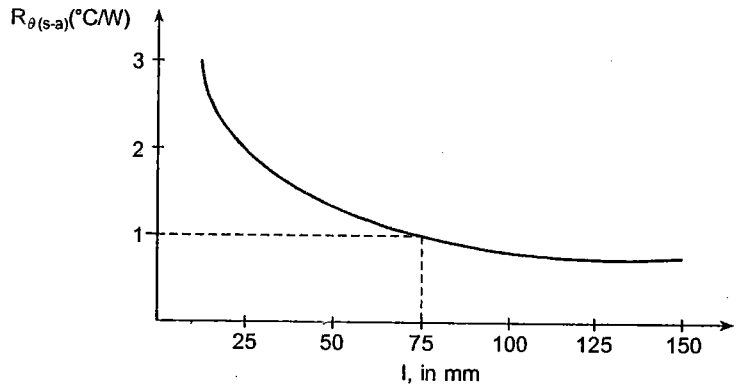


Figure 11.7 $R_{\theta(s\text{-}a)}$ with respect to length (l) of the heat sink shown in Fig. 11.6(a).

For a high-duty ratio pulse (more than 1 μs), the peak junction temperature is considered to be equal to the average junction temperature. The empirical formula will suffice. However, in case of highly inductive loads, it may cause current crowding condition leading to formation of hot spot hence second-breakdown (as discussed in *di/dt* rating of the thyristors in Chapter 2) and the concept of thermal design may be invalid. In such cases, accordingly, SOA of transistors (BJT, MOSFET, IGBT, etc.) or *di/dt* ratings of thyristors must be considered. Similarly, for a very-low duty-ratio, the peak junction temperature is important—not the average temperature. It necessitates the study of heat flow in dynamic condition.

If the casing is kept at sink potential, then silicon grease is used to avoid air film or aluminium oxide layer between the mating surfaces of casing and sink. Otherwise, these layers reduce heat transfer and $R_{\theta(c\text{-}s)}$ becomes high. Sometimes, the device is electrically insulated from the heat sink (e.g. devices at different potential, placed on same heat sink). Then mica sheet is put in between casing and heat sink but it reduces heat flow ($R_{\theta(c\text{-}s)}$ increases by 10–25%). Alternatively, for better cooling, mica sheet is not used and the heat-sink with device is isolated

from the chasis with an insulator (while both device and heat sink are at same potential and in direct contact with each other).

From Fig. 11.4, the total thermal resistance of the device junction to the atmosphere (open air) is given by

$$R_{\theta(\text{j-a})} = R_{\theta(\text{j-c})} + \frac{[R_{\theta(\text{c-s})} + R_{\theta(\text{s-a})}]\, R_{\theta(\text{c-a})}}{R_{\theta(\text{c-s})} + R_{\theta(\text{s-a})} + R_{\theta(\text{c-a})}} \tag{11.5}$$

For very low power dissipation (a few watts only), no cooling arrangement or heat sink is required, then $R_{\theta(\text{c-s})}$ and $R_{\theta(\text{s-a})}$ are neglected. Therefore, the effective thermal resistance is

$$R_{\theta(\text{j-a})} = R_{\theta(\text{j-c})} + R_{\theta(\text{c-a})} \tag{11.6}$$

However, in general, cooling arrangement (heat sink) is used for the device thermal protection. A direct heat transfer (radiation) from casing to air is small. Therefore, $R_{\theta(\text{c-a})}$ is large compared with the other parallel thermal resistance, $R_{\theta(\text{c-s})} + R_{\theta(\text{s-a})}$. Thus,

$$R_{\theta(\text{j-a})} = R_{\theta(\text{j-c})} + R_{\theta(\text{c-s})} + R_{\theta(\text{s-a})} \tag{11.7}$$

and

$$T_\text{j} - T_\text{a} = P_\text{d}\,[R_{\theta(\text{j-c})} + R_{\theta(\text{c-s})} + R_{\theta(\text{s-a})}] \tag{11.8}$$

An empirical formula for thermal resistance of a flat square plate (at 45°C ambient temperature), where one power dissipating device placed at the centre, is given by

$$R_{\theta(\text{s-a})} = 3.3\left(\frac{\sqrt{k_\text{c}}}{10\,wk}\right)^{1/2} + \frac{650\,k_\text{c}}{A} \tag{11.9}$$

where k_c is the correction factor, which is 1.0 for shining, horizontal surface and 0.43 for rough-black (or matt-black) vertical surface. A is the area of heat sink (in cm^2) and w is thickness of heat sink (in cm). Also, k is the thermal conductance of the heat sink (in W/cm-°C) which is 3.86, 2.0, 1.4, 1.1, 0.46, 0.27 and 0.006 for copper, aluminium, ceramics, brass, steel, aluminium oxide (Al_2O_3) and mica, respectively.

In general, matt-black aluminium heat sinks (painted) are used. Otherwise aluminium oxide (Al_2O_3) forms at the shining surface of aluminium heat sinks. Al_2O_3 has very poor conductivity (both electrical and thermal). Normally, $R_{\theta(\text{c-s})}$ is neglected for a good conduction between casing and heat-sink (when silicon–grease is used). General derating of about 50% and 15% are done in $R_{\theta(\text{s-a})}$, for each horizontal mounting as well as shining surface of the same heat sink, respectively. Manufacturers of devices provide data for $R_{\theta(\text{j-c})}$. Similarly, there are standard size heat sinks and their manufacturers provide $R_{\theta(\text{s-a})}$.

Table 11.2 Thermal Conductivity of Different Materials (k in W/cm-°C)

Materials	*At* 20°C	*At* 100°C
Silver (pure)	4.07	4.164
Copper (pure)	3.86	3.79
Aluminium (pure)	1.756	2.06
Tin (pure)	65.00	5.99
Stainless steel	19.30	0.46
Water	0.51	
Air	0.022	

Example 11.1 The casing temperature of a thyristor is at 70°C with one face (hot side) of a flat aluminium heat sink (sheet). The other side (cold side) of the heat sink is at 50°C. The thickness and the thermal conductivity of aluminium are 5 mm and 2 W/cm-°C. Find the rate of heat transfer through the heat sink.

Solution The rate of heat transfer or per-unit area heat transfer is given by

$$\frac{P_d}{A} = \frac{k}{w\Delta T} = \frac{2}{0.5(70-50)} = 200 \text{ mW/cm}^2$$

11.4.3 Transient Thermal Impedance

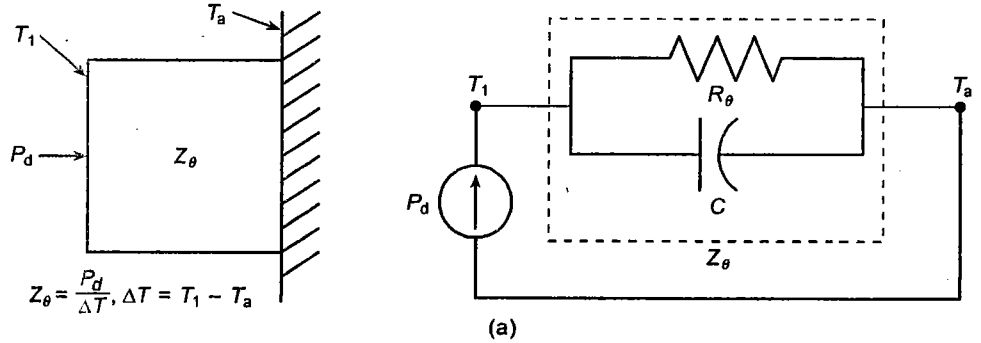
Up till now the temperature is considered for steady-state average power dissipation in the device only. However, a rectangular power pulse causes fluctuations in junction temperature. During transient overloads or when the load current increases suddenly, the instantaneous dissipation (p_d) in the devices may be higher than the average rating of the device. Consequently, the junction temperature-rise depends upon the duration of the surge or load current and the thermal properties of the device. For this purpose, heat capacity (C_s) of the device is also taken into consideration along with thermal resistance (R). The value of C_s is given by

$$C_s = C_v Ad = \frac{d\theta}{dT} Ad \tag{11.10}$$

where C_v is heat capacity per unit volume, A is cross-sectional area of heat flow and d is thickness in the direction of heat flow. Similarly, if the heat flow takes place through different materials, each segment can be represented by a thermal impedance, z_θ or an RC parallel branch, in equivalent electrical circuit model (Figs. 11.8a and 11.8b). Figure 11.8 shows the temperature profile or variation with different conditions of heat generation. The dynamics of the temperature are important when the device is forced to dissipate high level of power within very short period of time.

For very short pulses (<1 μs), the mass of silicon is important as sudden temperature rise confines near the junction. A wide pulse causes sustained power loss and heat generation in device. Thus heat transfer takes place to casing and heat-sink design becomes important.

Manufacturers of devices specify the thermal response or the variation of Z_θ with respect to either width of on-state pulse (Fig. 11.8c) or both duty-ratio (D) and frequency of operation (Fig. 11.8d).



(a)

Figure 11.8 (*Cont.*)

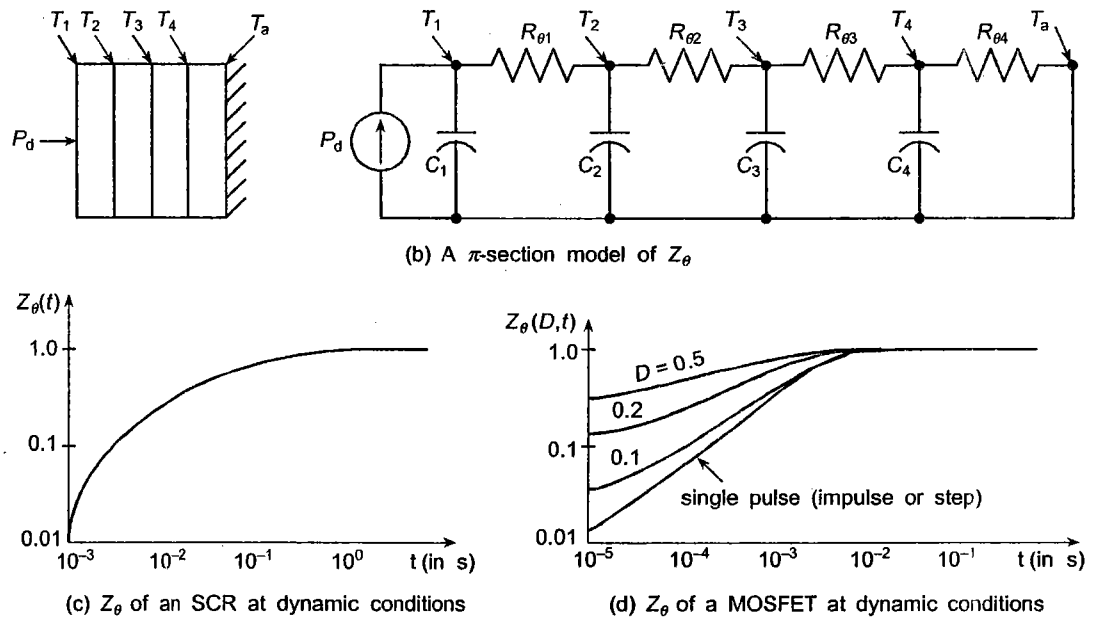


Figure 11.8 Equivalent circuit and dynamic characteristics of thermal impedance.

The temperature rise depends upon the duration of power pulse (power loss in device) as well as the frequency of operation, as shown in Fig. 11.9. For the same duty ratio, temperature rise is more in case of low-frequency switching as the on-period (T_{on}) of the device is longer. In case of a non-rectangular power pulse (e.g. quasi sinusoidal wave), an equivalent rectangular power pulse (p_d) with same peak and same average values may be considered for the calculation (Fig. 11.9c). Therefore, D is considered according to the equivalent rectangular power pulse.

Manufacturer provides data in the following form: *Device*: Diode D5807N, *Make*: Eupec, Germany. V_{DRM} = 600 V, $I_{FM(RMS)}$ = 9100 A, $I_{FSM(10ms)}$ = 70 kA, $\int i^2dt = i^2t_{(10ms@Tjmax)}$ = 24.5 × 10^3A^2-s, $I_{FM(AV)}/t_C$ = 5800/108 A/°C, $V_{T(@Vjmax)}$ = 0.7 V, $r_{T(@Vjmax)}$ = 0.04 mΩ, $R_{\theta(j\text{-}C)(180°sin)}$ = 0.01 mΩ, $T_{j(max)}$ = 180°C.

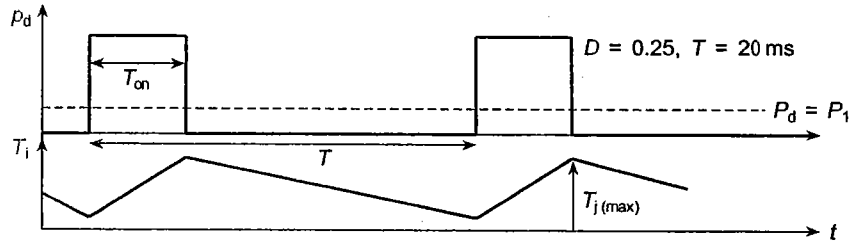
The on-state device loss at maximum junction temperature (worst case), with rated current, $I^2r_T = (5800)^2 \times 0.04 \times 10^{-3}$ =1345.6 W for 180° conduction of sinusoidal waveform. Also, at low or mains frequency (below 1 kHz), the switching loss of the device is neglected.

The step response of a first-order system is used to express the transient thermal impedance (due to the rectangular wave), which is given by

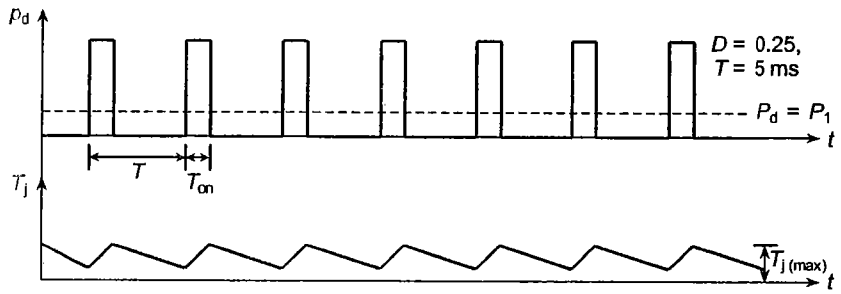
$$Z_\theta(t) = \frac{T(t)}{P_d} = Z_{\theta o}\left[1 - \exp\left(-\frac{t}{\tau_\theta}\right)\right] \tag{11.11}$$

where $Z_{\theta o}$ is the steady-state thermal impedance and τ_θ is thermal time constant. The thermal impedance of repetitive pulse can be determined from the single pulse value (z_θ), as:

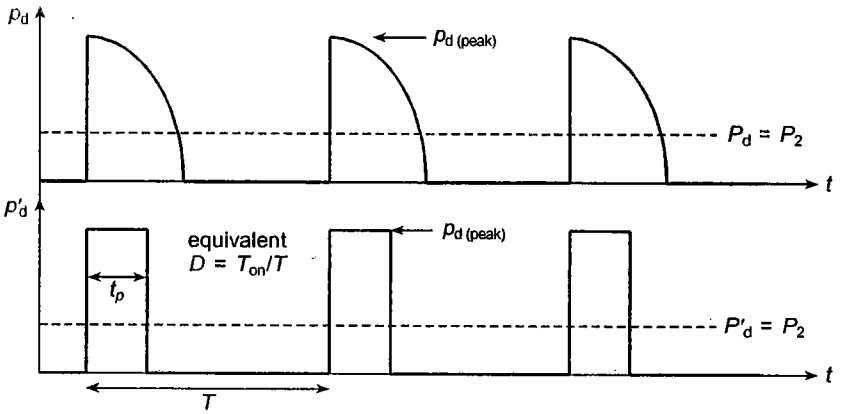
$$Z_\theta(t_p, D) = D + (1 - D)\, z_\theta(t_p) \tag{11.12}$$



(a) High $T_{j(max)}$ for high T_{on}



(b) Low $T_{j(max)}$ for the same D and P_d



(c) An equivalent rectangular power pulse (p'_d) and D, for a non-rectangular p_d.

Figure 11.9 Effect of D and frequency on T_j.

where D is duty cycle and t_p is the duration of the rectangular pulse (T_{on} an equivalent rectangular pulse, in case of a non-rectangular power pulse). Also,

$$Z_\theta(t_p, D) = \frac{\Delta T}{P_{max}} = \frac{T_j - T_c}{P_{max}} \tag{11.13}$$

For a step power input (P_d), the rise in junction temperature is given by

$$\Delta T = T(t) - T_a = P_d \sqrt{\frac{t}{\tau_\theta}} \tag{11.14}$$

and

$$\tau_\theta = \frac{\pi}{4} R_{\theta(c\text{-}s)} C_s \tag{11.15}$$

where τ_θ is the thermal time constant. Then

$$\Delta T^2 = P_d \frac{t}{\tau_o} \tag{11.16}$$

However, if the transient pulse power input is not a step function, then analysis is done with an equivalent square pulse with same total energy, as shown in Fig. 11.8. Since, flow of heat takes place through different materials (from junction to heat sink), the transient equivalent circuit includes the heat capacities, as shown in Fig. 11.8. The flow of heat is delayed due to this RC ladder network.

11.4.4 Heat Flow by Convection

The major part of heat flow from the heat sink to the atmosphere takes place by convection. For a vertical surface of height, h_v, the heat transfer to the surrounding air by convection is given by

$$P_{conv} = 1.34 A_{eff} \left(\frac{\Delta T}{h_v} \right)^{1/4} \Delta T \tag{11.17}$$

and

$$A_{eff} = \frac{K_s}{K_f} A \tag{11.18}$$

where A_{eff} is the effective surface area of the heat sink which depends upon the fins arrangement and natural or forced (air) cooling, A is the actual surface area of heat sink. K_s is surface reduction factor due to crowded fins and K_f is reduction factor of forced cooling (other than natural cooling). Therefore, thermal resistance for the convection is given by

$$R_{\theta,conv} = \frac{\Delta T}{P_{conv}} = \frac{1}{1.34 A_{eff}} \left(\frac{h_v}{\Delta T} \right)^{1/4} \tag{11.19}$$

If the gap between cooling fins of heat sink is less than 25 mm, the effective cooling by convection reduces. However up to 12.5 mm, the surface reduction factor (K_s) of heat sink does not change significantly. It is about 0.9. For small separation of fins (below 10 mm), the equation given below suffices

$$K_s = 0.4(0.3d - 1) \tag{11.20}$$

where d is the separation of fins in mm.

The size of heat sink reduces due to crowded fins and increases due to forced air cooling. For natural cooling (without forced air cooling by fan or by water circulation), K_f is 1. However, forced air cooling of the heat sink greatly reduces thermal resistance. The variation in the value of R_θ is almost exponential. Initially, it decreases rapidly and later variation becomes insignificant for increase in velocity of cooling air. It reduces to a half, if the air flow is at 2 m/s (or 7.2 km/hr) and becomes 1/3 for 4 m/s. Therefore, the required size of heat sink reduces drastically. Moreover, the transient performance of devices from transistor family improves due to better and quick

cooling. Sometimes both air and liquid (oil or water) are also used for cooling which further reduce the size of heat sink. Also, for turbulent flow of air (or coolant), the heat transfer rate is faster (3–4 times) than for the laminar flow.

Example 11.2 A flat heat-sink aluminium plate is placed in air stream blowing parallel at 30°C. The convective heat transfer coefficient is 30 W/m^2-°C. Calculate the area of the flat heat sink, if a MOSFET placed on it, dissipates 10.5 W (heat). The temperature of heat sink (plate) is maintained at 100°C.

Solution A system is normally designed to achieve high reliability for which the worst-case junction temperature is considered between 85 and 105°C (from 20 to 40°C below 125°C). Similarly, consider the worst-case heat sink temperature, i.e. the heat sink is at a junction temperature. Moreover, cooling is taking place by natural convection only. The heat generation of the device is equal to the heat transfer. Therefore,

$$P_d = hA\,(T_s - T_a)$$

or

$$10.5 = 30A\,(100 - 30)$$

or

$$A = 5 \times 10^{-3}\ \text{m}^2 = 50\ \text{cm}^2$$

Table 11.3 Heat Transfer Coefficient (h)

Process of heat transfer	h in W/m^2-°C
Free convection, air	5–28
Forced convection, air	10–500
Water	100–17,000
Boiling water	2,500–57,000
Condensation of steam	5,000–110,000

11.4.5 Heat Flow by Radiation

A significant amount of heat flows from the heat sink to the atmosphere by radiation. Thermal radiation is based on the concept of the black body. The total thermal radiation from the black body is given by the Stefen–Boltzman law. The expression of heat flow (q) in terms of W/m^2, is given by

$$q = 5.7 \times 10^{-8} e(T_1^4 - T_2^4) \tag{11.21}$$

where e is the emissivity constant, T_1 and T_2 are temperatures of hot and cold bodies in Kelvin. Therefore, the radiated power from a surface area A of the heat sink (hot body) to the atmosphere (air) is given by

$$P_{rad} = 5.7 \times 10^{-8} eA(T_s^4 - T_a^4) \tag{11.22}$$

The value of emissivity constant varies from 0 to 1 (refer to Table 11.4). A rough-black or matt-black surface radiates more heat than a smooth and bright or shiny surface. Its value is 0.9, 0.65, 0.25, 0.15 and 0.1 for matt-black oxidized aluminium, black iron-plate, cast iron, polished copper and polished aluminium, respectively. The value of R_θ due to radiation is given by

$$R_{\theta(rad)} = \frac{\Delta T}{P_{rad}} = \frac{\Delta T}{5.7 \times 10^{-8} eA\,(T_s^4 - T_a^4)} \tag{11.23}$$

Table 11.4 Emissivity Constant (e) for Radiation

Materials	*e* at 100°C
Aluminium (polished)	0.095
Aluminium (commercial sheet)	0.09
Aluminium oxidized (up to 200°)	0.11
Copper (polished)	0.023
Copper (commercial)	0.072
Stainless steel (polished)	0.074
Iron (oxidized)	0.736
Aluminium paint	0.52
Water	0.95

11.5 PROCEDURE OF HEAT SINK DESIGN

Following procedure may be adopted for the calculation of the size and type of heat sink. A suitable custom-built heat sink may be selected there from.

1. For a given heat generation of a device and an ambient (air) temperature, $R_{\theta(s\text{-}a)}$ has to be calculated. The effective heat flow from heat sink to air is due to convection and radiation. Therefore, $R_{\theta(s\text{-}a)}$ is equivalent to two parallel thermal resistances, convection, $R_{\theta(s\text{-}a)(conv)}$ and radiation, $R_{\theta(s\text{-}a)(rad)}$.
2. Find $R_{\theta(s\text{-}a)(conv)}$ using the equation:

$$R_{\theta(s\text{-}a)(conv)} = \frac{1}{1.34A_{eff}}\left(\frac{d_{vert}}{\Delta T}\right)^{1/4}$$

   For natural convection, K_f is 1. However, for forced air cooling, K_f is less than 1. It reduces to almost 0.2 for higher speed (12 m/s). Similarly, if fins are not crowded (between 12 to 25 mm), take $K_s = 0.9$. For narrow fins, K_s is less than 1. It can be found using (11.20).
3. For calculation of $R_{\theta(s\text{-}a)(rad)}$ for radiation, the emissivity factor (e) is important. Generally, matt-black oxidized aluminium heat sinks are used, whose e is equal to 0.9. Therefore,

$$P_{rad} = 0.9 \times 5.7 \times 10^{-8} eA\ (T_s^4 - T_a^4)$$

   and

$$R_{\theta(s\text{-}a)(rad)} = \frac{\Delta T}{P_{rad}} = \frac{1.96 \times 10^7}{(T_s^2 + T_a^2)(T_s + T_a)}$$

4. Find $R_{\theta(s\text{-}a)}$ as mentioned in 1. From the chart of the standard size heat sinks (available in the market), a suitable heat sink can be selected. Else, for a particular type of heat sink, as given in Fig. 11.6a, the length of heat sink can be found.

Example 11.3 Design a heat sink for a fast-recovery diode operates at 10 kHz with 50% duty cycle and 60-A current (peak) in a 400-V converter. The thermal resistance between junctions to case is 0.7 K/W and the ambient temperature is 45°C. The device on-state loss at that condition is 40 W. At the worst-case junction temperature (150°C), the reverse-recovery charge is 1.1 μC (@ reverse dI_F/dt = 40 A/μs at 60 A and 400 V).

Solution The on-state loss at 50% duty cycle or at 60 A (i.e. at 30 A diode average current), is 40 W. At frequency above 100 Hz, fast recovery diodes are used. Therefore the switching losses are also added to the on-state conduction loss. The turn-off time is longer and therefore turn-on loss is neglected. The turn-off loss depends linearly upon the junction temperature and the switching frequency. The reverse recovery switching loss is given by

$$P_R = Q_R V_R f_s$$

where V_R is the reverse-voltage applied just after turn off, Q_R is the maximum reverse recovery charge and f_s is the switching frequency. Then

$$P_R = 1.1 \times 10^{-6} \times 400 \times 10 \times 10^3 = 4.4 \text{ W}$$

Total losses in the device, P_d = 40 + 4.4 = 44.4 W. The thermal resistance of the heat sink can be found as

$$P_d = \frac{T_j - T_a}{R_{\theta(j\text{-}c)} + R_{\theta(c\text{-}s)} + R_{\theta(s\text{-}a)}}$$

Then

$$R_{\theta(s\text{-}a)} = \frac{T_j - T_a}{P_d} - R_{\theta(j\text{-}c)}$$

Consider the worst case, i.e. the heat-sink temperature is same as the junction te.nperature. Therefore, $R_{\theta(c\text{-}s)}$ becomes zero, and

$$R_{\theta(s\text{-}a)} = \frac{150° - 45°}{44.4} - 0.7 = 1.665 \text{ K/W or °C/W}$$

A suitable custom-built heat sink may be selected accordingly.

11.6 MAGNETIC MATERIALS

Magnetic components and materials are extensively used in power electronic circuits. Soft magnetic materials are used in transformers, saturable reactors, chokes and inductors; while hard magnetic materials are used in permanent magnet and ferrite beads for EMI suppression. These devices may be required to operate at mains frequency (50 or 60 Hz) or over a wide range of frequency from dc to several MHz. The use and applications of these materials and components vary over wide range on the basis of their parameters, viz., inductance, voltage, current, power, frequency, leakage, dissipation, efficiency, voltage regulation, weight, size, cost, etc. Although standard type of transformers and chokes are available in the market, even then, due to large variation in the parameters (as discussed above) it is impractical for a manufacturer to produce and stock for all requirements. Thus, according to the consumer's need, these components are designed and fabricated.

Although design method are standardized but due to involvement of non-linearity (as permeability does not remain constant for different values of flux density), the calculation gets heavily affected. Therefore, the solution highly relies on experience. Moreover, several software packages are available for designing the magnetic circuits and components, such as QUICK FIELD of Tera Analysis Ltd., OPERA software of Vector Fields, SABER of Analogy Software, etc.

The characteristic of magnetic materials varies over wide range. These materials are classified in the further sections on the basis of **B-H** curve or loop.

11.6.1 Ideal or Perfect Permeability

In this case, slight amount of magnetic field intensity (**H**) is enough to establish a very large flux density (**B**) and material is loss less. **B** is always proportional to **H** for all values of **H** and therefore permeability and permeability constant, μ (or μ_r) remain constant. Here both hysterisis and eddy current losses are absent. Practically no such material exists.

11.6.2 Soft Magnetic Materials

These materials are extensively used in power electronic circuits. Low iron-loss steel of high permeability is used for core lamination of inductors, transformers and rotating machines. It minimizes the reluctance of flux path, the requirement of magnetic field intensity (**H**) or ampere-turns and the iron losses for alternating current. Soft magnetic materials are further classified as: ferromagnetic materials and ferrimagnetic materials.

Materials of the former type are based on iron and nickel and applicable to low and mains frequency. While the ferrite materials are based on ceramic oxides of materials (Mn, Zn, Ni, etc). It is used from a few kHz to nearly 100-MHz frequency range.

Ferromagnetic materials Cold-rolled, grain-oriented steel (3–4% silicon) laminations are used for low and mains frequency transformers and inductors. Non-oriented steels are usually used for rotating machine laminations. Iron powder cores are made by compacting insulating high-quality spongy iron powder. The insulation of powdered particles increases resistivity while both permeability and eddy current-loss reduce. Alloys powders are also used with a combination of 50–75% nickel, 20–45% iron and small percentage of molybdenum. Higher percentage of iron increases saturation level (B_{sat}) but the iron losses also increases. For RFI suppression and filter applications, silicon steel is not effective. Thus iron alloys with high iron content are used to achieve high flux density and higher core losses which help RFI suppression.

With alternating flux in steel sheet, the self-inductance at central part becomes high. It causes skin effect and prevents flux penetration inside the sheet. As frequency increases, the flux density at central part reduces in comparison to the surface flux. That is why, the core material are produced in a different lamination thicknesses for different frequency applications. For example, 0.3-mm laminations for 0–200 Hz, 0.1-mm laminations for 0.2–2 kHz and 0.05-mm laminations for pulse or above 1 kHz applications.

Ferrimagnetic materials Ferrites are polycrystalline magnetic ceramic oxides. It is a compound of one or more oxides of Fe, Ni, Zn, Cu, Ba, Co, Mn mixed with iron oxide (Fe_2O_3). For lower and higher frequency applications, combinations of Mn–Zn and Ni–Zn are used respectively.

11.6.3 Magnetically Hard Materials

This type of material has very high residual magnetism. This characteristic is utilized for permanent magnet (PM) poles, e.g. PMdc motors, PMac motors, stepper motors, etc. For example, alnico steels and neodymium iron–boron have residual flux density ($\mathbf{B}_r$) more then 1 tesla (T). Also $\mathbf{B}_r$ for samarium–cobalt and ferrite are about 0.9 T and 0.3 T, respectively.

11.6.4 Constant Permeability Materials

In this case, **B** is always proportional to **H** for all values of **H** and therefore the permeability, μ (or μ_r) remain constant. Here both hysterisis and eddy current losses are neglected (e.g. air, vacuum and all non-magnetic and insulating materials).

11.6.5 Complex and/or Nonlinear Permeability Materials

For this type of materials, there is sinusoidal relationship between **B** and **H**. The hysterisis loop is considered to be elliptical. Sometimes the relationship between **B-H** is nonlinear and complex too.

11.6.6 Accurate Characteristics Materials

Several magnetic materials are manufactured under strict quality control conditions. It gives an accurate **B-H** characteristics and a family of **B-H** loops. Several software packages are available for simulation of magnetic circuits with built-in facilities of **B-H** curve and loops of these standard magnetic materials.

11.7 MAGNETIC CIRCUITS

In case of an electric circuit, current is considered to be confined to the conductor and circuit components only. It is because outside the electric circuit (e.g. air or insulation), the resistance or impedance are in the range of several hundred thousand ohms to several hundred megaohms). Therefore, the leakage current is almost negligible. However, in case of magnetic circuits, the circuit completes its path through air, vacuum, non-magnetic materials and magnetic materials. The reluctance (just like the resistance of an electric circuit) of magnetic material and non-magnetic materials (outside the magnetic material) does not defer to a large extent. The relative permeability (μ_r, which is inversely proportional to reluctance) of non-magnetic materials including air/vacuum is one. It varies in between 10 to 10^5, for magnetic materials. Therefore, the flux does not confine to magnetic materials only (like current in conductor and electric circuit elements), but substantially leaks to neighbouring materials and completes the magnetic circuit path through them. Therefore, analysis of magnetic circuit design of inductors and transformer becomes somewhat complex.

A magnetic circuit can be described by Ampere's law (Fig. 11.10). It states that the line integral of the magnetic field intensity (**H**) is equal to the (enclosed) current, i.e.

$$\int \mathbf{H} \cdot \mathbf{dl} = \int \mathbf{J} \cdot \mathbf{ds} = \sum i = Ni = \Im \tag{11.24}$$

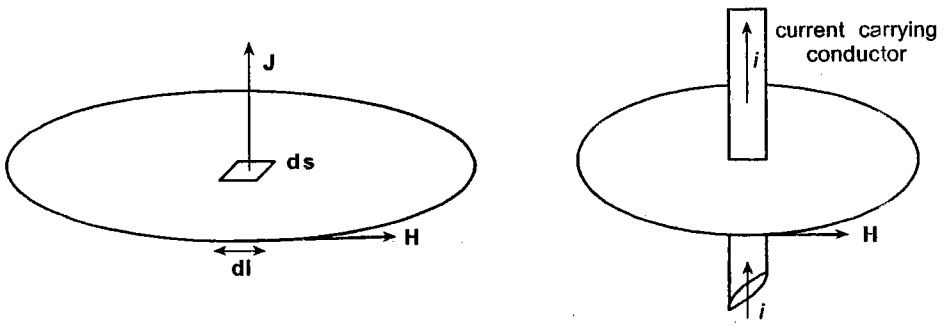


Figure 11.10 General form of Ampere's law.

where,

H = Magnetic field intensity (A/m)

dl = Differential length of magnetic field (m)

J = Conduction current density (A/m^2)

ds = Differential surface through which current passes (m^2)

i = Conduction current (A)

Σi = Total current (A)

N = Number of turns of windings, and

$\Im$ = the magneto-motive force (mmf). It is like an emf in electric circuits and its unit is ampere-turns.

The direction of the magnetic field produced by the current is given by the right-hand rule method. The magnetic field intensity (**H**) sets up a proportional flux density (**B**) at every point along the flux path. That is,

$$\mathbf{B} = \mu \mathbf{H} \quad \text{and} \quad \mathbf{B} = \mu_o \mu_r \mathbf{H} \tag{11.25}$$

The relative permeability, $\mu_r = 1$ for air, vacuum and all the non-magnetic materials. For magnetic materials, μ_r varies from 10 to several thousand. The flux through a certain area is given by

$$\phi = \oint \mathbf{B} \cdot \mathbf{ds} = BA_c \tag{11.26}$$

where A_c is area of cross-section of core material.

If l_c is the length of the mean path of flux (Fig. 11.11), then

$$\phi = \mu_c H A_c = \mu_c \frac{\text{Ni}}{l_c} A_c \tag{11.27}$$

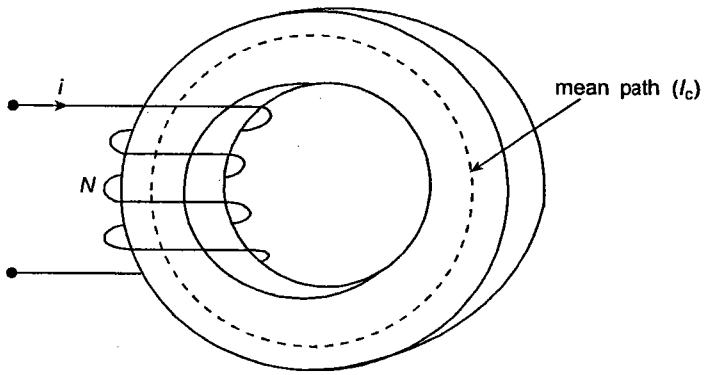


Figure 11.11 Toroidal inductor with N turns.

or

$$\phi = \frac{\text{Ni}}{l_c/(\mu_c A_c)} = \frac{\mathcal{F}}{\mathcal{R}} = \mathcal{F}\mathcal{P}$$

or

$$\mathcal{R} = \frac{l_c}{\mu_c A_c} \quad \text{and} \quad \mathcal{P} = \frac{\mu_c A_c}{l_c} \tag{11.28}$$

where $\mathcal{R}$ and $\mathcal{P}$ are the reluctance and the permeance of the path of the magnetic circuit respectively, through which the flux passes.

11.7.1 Electrical Analog of Magnetic Circuits

The flux (ϕ) in the core resembles like electric current in a close circuit path. Thus, if ϕ is analogous to the current then mmf ($\mathcal{F}$) and reluctance ($\mathcal{R}$) are analogous to emf and resistance of an electric circuit respectively as shown in Fig. 11.12. The permeance, $\mathcal{P}$ is inverse of the

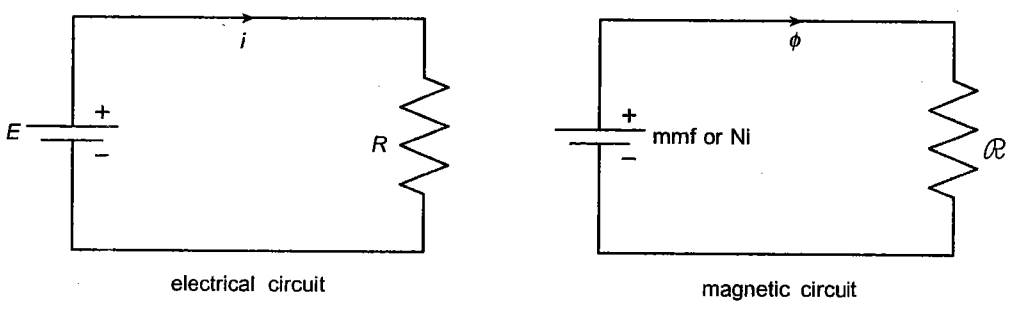


Figure 11.12 Electrical and magnetic analog circuits.

reluctance and it is analogous to the conductance of an electric current. However, there is a practical difference between magnetic circuit and electric circuit. In an electric circuit, the current confines to the connected circuit elements and the connecting wires only as the conductance through the materials surrounding the circuit (air, insulation of wire and cables, etc.) is extremely low. However, in magnetic circuits, $\mathcal{P}$ or μ_r of iron or magnetic materials are compatible to surrounding medium (air or non-magnetic materials). Therefore, a significant amount of flux leaks and completes its path outside the magnetic material or core, undesirably. Sometimes this leakage may be negligible due to high $\mathcal{P}$ or μ_r of magnetic materials (initial part of **B-H** curve, as shown in Fig. 11.13), as most of the flux confine to the magnetic material due to low reluctance. However, when the same magnetic core gets saturated (last part of the **B-H** curve), both $\mathcal{P}$ and μ_r reduce drastically and more flux leaks outside the magnetic material. Thus the leakage flux becomes significant portion of the total flux. In general, the leakage flux calculation is also incorporated for accurate magnetic circuit design.

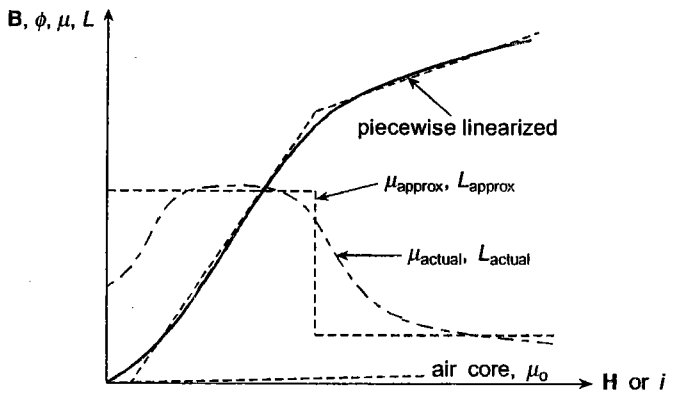
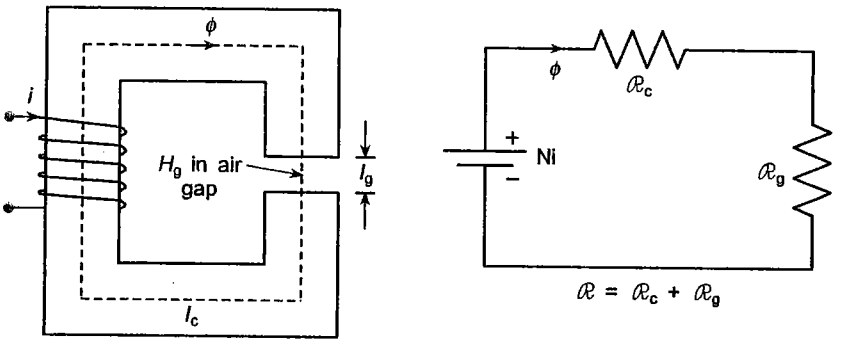


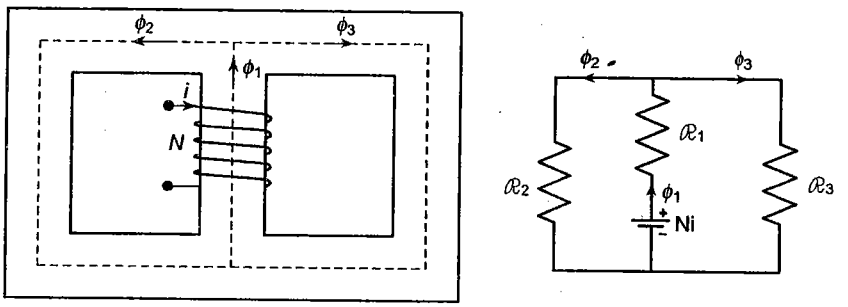
Figure 11.13 **B-H** curve of magnetic materials.

11.7.2 Magnetic Circuit Calculation

Electrical circuit analog can be utilized for the calculation of the reluctance, inductance, etc., for a given magnetic circuit. Series and parallel combinations of reluctance (like series and parallel combinations of resistance) can be employed to find the final or total value of the reluctance ($\mathcal{R}$). If there are two magnetically, dissimilar materials through which the same flux passes. The two reluctances will be in series (Fig. 11.14a). Similarly, if flux splits and each component completes its path independently through the same or different materials, the two reluctances will be in parallel (Fig. 11.14b).



(a) Series component



(b) Parallel component

Figure 11.14 Magnetic circuits.

11.7.3 Calculation of Inductances

Every current carrying conductor generates magnetic flux around it. The inductance of conductor is related with the flux linkage (λ) and therefore the Ampere's law holds good for this condition. However, most simple configuration is with a toroidal core of magnetic material, as shown in Fig. 11.11. If the permeability (μ) of the material is assumed to be constant, the value of the inductance is given by

$$L = \frac{\lambda}{i} \tag{11.29}$$

Also from the Ampere's law, with the assumption of negligible leakage flux outside the core, the flux passing through the core remains constant at any point (within the core) along the length of flux path, l_c. Therefore,

$$\mathbf{H}\, l_c = Ni \tag{11.30}$$

Moreover, due to symmetry of the core, the flux density (**B**) remains constant across the cross-sectional area of the core at each and every point. Therefore,

$$\mathbf{B} = \mu \mathbf{H} = \mu_o \mu_r \frac{Ni}{l_c} \tag{11.31}$$

The flux in the core is given by

$$\phi = BA_c = \frac{\mu_o \mu_r A_c N i}{l_c} \tag{11.32}$$

Therefore, from (11.29), the inductance is given by

$$L = \frac{\lambda}{i} = \frac{N\phi}{i} = \frac{\mu_o \mu_r A_c N^2}{l_c} \tag{11.33}$$

11.7.4 Inductors with an Air Gap

If there is an air-gap of length, l_g in the core of the magnetic material. The reluctances of the iron core and the air-gap are given by

$$\mathcal{R}_c = \frac{l_c - l_g}{\mu_o \mu_r A_c} \cong \frac{l_c}{\mu_o \mu_r A_c}, \quad \mathcal{R}_g = \frac{l_g}{\mu_o A_c} \tag{11.34}$$

The total reluctance, $\mathcal{R}$ is sum of $\mathcal{R}_c + \mathcal{R}_g$. Since l_c/μ_r is very small in comparison to l_g, the flux in the iron core and the air-gap is given by

$$\phi = \frac{mmf}{\mathcal{R}} = \frac{Ni}{\mathcal{R}_c + \mathcal{R}_g} = \frac{Ni}{\frac{1}{\mu_o A_c}\left(\frac{l_c}{\mu_r} + l_g\right)} \cong \frac{Ni\,\mu_o A_c}{l_g} \tag{11.35}$$

The inductance is given by

$$L = \frac{N\phi}{i} = \frac{\mu_o A_c N^2}{l_g} = \frac{N^2}{l_g/(\mu_o A_c)} = \frac{N^2}{\mathcal{R}_g} \tag{11.36}$$

Although μ or μ_r of the core material is assumed to be constant but practically it varies with the magnitude of the current, as shown in Fig. 11.13. In general, before the knee point it can be assumed constant without much deviation in the value of inductance which is proportional to slope on B-H curve i.e. **dB/dH** or $d\phi/di$. Because of the variation of μ or μ_r, the characteristics **B-H** curve is not a straight line (as in case of air core, where $\mu = \mu_o$). It is therefore evident from the equation of the inductance that its value varies over wide range due to variation of μ or μ_r. Moreover, the **B-H** curve of each specimen (magnetic material) has a unique relation. The manufacturers supply the average curves. That is why, it is very difficult to design an inductor or a transformer of exact value. Since inductance is proportional to μ_r, and μ_r is the slope of **B-H** curve (Fig. 11.13), L does not remain constant but varies according to **H** or the level of current (e.g. in case of alternating current). If the **B-H** curve is piece-wise linearized, it can be assumed that there are two effective values of inductance, i.e. before saturation and after saturation. In general, inductor/transformer is designed to operate in the former condition, however, sometimes, it is purposely used to operate in both conditions (e.g. in a ballast circuit of compact fluorescent lamp, CFL).

11.7.5 Effect of Leakage

As discussed earlier, the flux does not confine to the core rather leaks and completes its path through air or other materials (Fig. 11.15). Moreover, if the air gap is small we may assume that

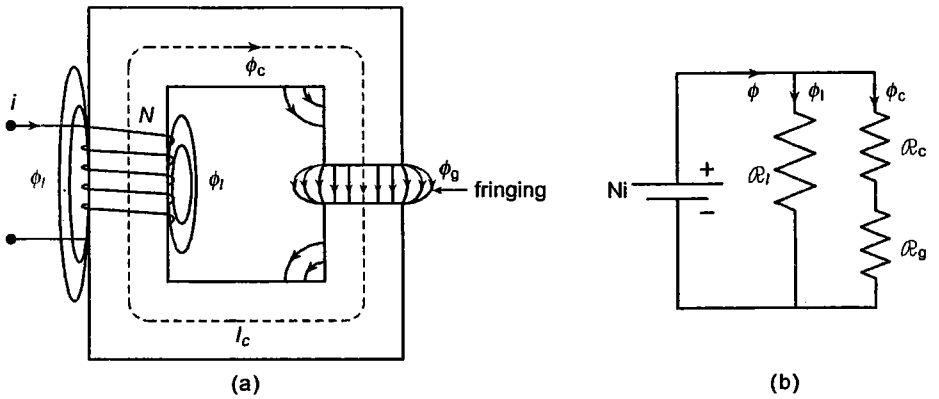


Figure 11.15 Leakage flux of an inductor with an air-gap.

the fringing effect is negligible and therefore the flux density remains same in the core as well as in the air gap. Otherwise, due to fringing effect, flux density ($\mathbf{B}_g$) will reduce (because the area through which the flux passes is now increased). Therefore, $\mathcal{R}_g$ also decreases ($\mathcal{R} \propto 1/A$). The leakage is represented by a parallel reluctance, $\mathcal{R}_l$ (as shown in Fig. 11.15b). The inductance of the inductor is given by

$$L = \frac{N\phi}{i} = \frac{N}{i}(\phi_l + \phi_c) = \frac{N}{i}\left(\frac{Ni}{\mathcal{R}_l} + \frac{Ni}{\mathcal{R}_c + \mathcal{R}_g}\right) = N^2\left(\frac{1}{\mathcal{R}_l} + \frac{1}{\mathcal{R}_c + \mathcal{R}_g}\right) \tag{11.37}$$

or

$$L = L_l + L_{cg}$$

where L_l is the leakage inductance and L_{cg} is the inductance due to ϕ_c.
Also

$$L_{cg} = \frac{N^2}{\mathcal{R}_c + \mathcal{R}_g} \cong \frac{N^2}{\mathcal{R}_g} \qquad (\text{as } \mathcal{R}_c << \mathcal{R}_g) \tag{11.38}$$

Therefore, $L \cong L_l + L_g$. Further more, if $L_l << L_g$, then the effective inductance of inductor is related with the inductance due to air gap.

11.7.6 Energy Storage

The effect of an air gap plays an important role in energy storage in the magnetic circuit or inductance. The magnetic stored energy is given by

$$W_m = \frac{1}{2}Li^2 = \frac{1}{2}(L_l + L_g)i^2$$

Since the leakage inductance, L_l is very small in comparision to L_g, we have

$$W_m \cong \frac{1}{2}L_g i^2 = \frac{1}{2}\frac{N^2}{R_g}i^2 = \frac{1}{2}\frac{\Im^2}{\mathcal{R}_g} = \frac{1}{2}\phi^2\mathcal{R}_g = \frac{1}{2}\frac{\phi^2 l_g}{\mu_o A_c} = \frac{1}{2\mu_o}l_g A_c B^2 = \frac{B^2}{2\mu_o}v_g \tag{11.39}$$

or

$$W_m \propto B^2 v_g \tag{11.40}$$

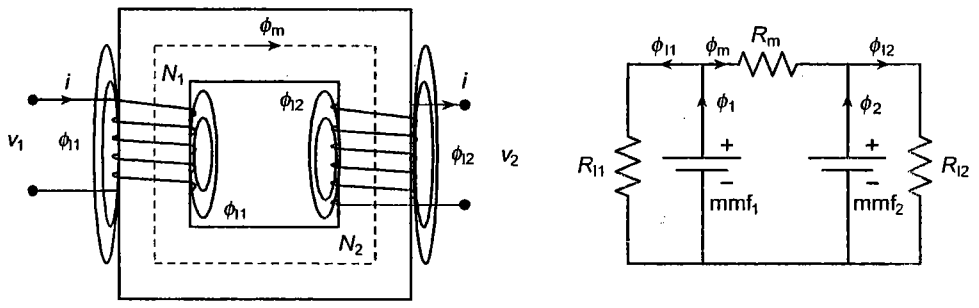
where, v_g is the volume of the air gap.

It is evident that the energy storage depends upon the volume of the air gap as well as the maximum flux-density, up to the saturation level of different magnetic materials (Table 11.5). Moreover, the air gap not only makes the inductor independent of the core's magnetic property and its variation, it also reduces residual magnetism in the core. The stored energy and the energy stored in air-gap per-unit volume (w_g), depend upon the inductance and the current. Therefore, **B** is allowed up to the saturation level (B_{sat}) in the core. Normally, air gap is taken $\frac{1}{10}$ th of the core cross-section area. Accordingly, the core-area (A_c) and the air gap are adjusted.

Table 11.5 Properties of Magnetic Materials

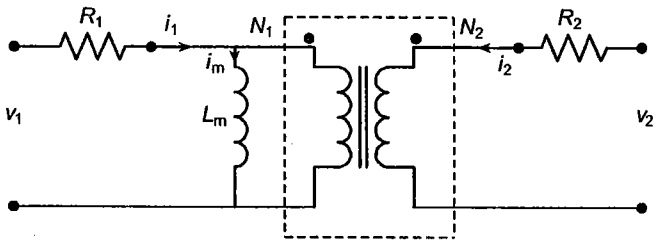
Materials	$\mathbf{B}_{sat}$ (T)	μ_r	ρ (μΩ-cm)	$w_{g(max)}$ (J/cm^3)
Ferrite-I (Ni–Zn)	0.2–0.3	150	10^{11}	0.035
Ferrite-II(Mn–Zn)	0.3–0.4	1000–4000	10^8	0.143
Nickel alloys (48%)	1.5	40000	48	0.895
Metallic glass/metglass	1.6	10000	125	1.018
Silicon–steel (2.5%)	2.0	5000	40	1.59
Core or armature–iron	2.1	4500	25	1.755
Low silicon–iron	2.2	2700	10	1.925

In case of transformers operating at a high frequency, the leakage flux becomes significant in comparison to the winding resistance. Similarly, L_m also becomes high (Fig. 11.16). At a high frequency (above 10 kHz), the skin effect in the copper conductors of the windings becomes significant. If the diameter of the conductor is 1 mm or more, litz wires are used, which is a combination of isolated and insulated stranded parallel conductor (just like bundle conductor of transmission line and sometimes the litz wires are transposed, too). As discussed earlier for high-frequency applications, proper core material is selected to reduce eddy current and hysteresis losses. To reduce eddy current, the resistivity of core materials should be high (spongy iron powder or carbonyl iron are used). Similarly, laminations size (thickness) should also be selected according to frequency of operation.

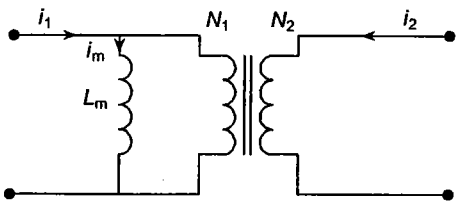


(a) Magnetic circuit

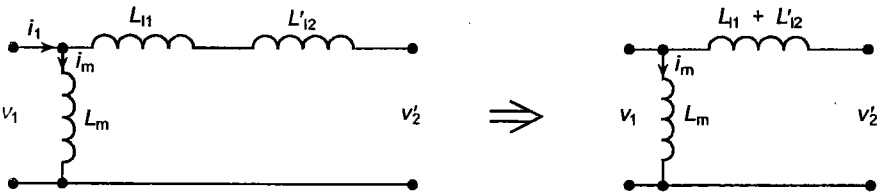
Figure 11.16 (*Cont.*)



(b) Equivalent electric circuit



(c) Simple model with perfect coupling



(d) Approximate equivalent circuit with referred secondary winding leakage inductance (L'_{12})

Figure 11.16 Electrical and magnetic circuits of transformers.

Example 11.3 Find the inductance of a core structure made of stallay, as shown in Fig. 11.14a. Before the knee point (1.2 tesla), μ is constant and $\mu_r = 4000$. The number of turns, mean path of the core flux, air gap and core area are 1000, 10 cm, 1 mm and 2 cm^2, respectively. Find: (a) the induction current and (b) the maximum allowable current that will not saturate the core.

Solution Let the flux confined to the core and leakage is negligible. Moreover, magnetic field intensity (**H**) follows the mean path, l_c. Reluctances of the core and air-gap are given by

$$\mathcal{R}_c = \frac{l_c - l_g}{\mu_o \mu_r A_c} = \frac{l_c}{\mu_o \mu_r A_c}, \qquad \text{since } l_c >> l_g$$

and

$$\mathcal{R}_g = \frac{l_g}{\mu_o A_c}$$

Now, using electrical analog, as shown in Fig 11.14a,

$$L = \frac{N\phi}{i} = \frac{N^2}{\mathcal{R}} = \frac{N^2}{\mathcal{R}_c + \mathcal{R}_g}$$

Therefore,

$$\frac{1}{L} = \frac{\mathcal{R}_c + \mathcal{R}_g}{N^2} = \frac{1}{N^2}\frac{l_c}{A_c}\frac{1}{\mu_o\mu_r} + \frac{1}{N^2}\frac{l_g}{A_c}\frac{1}{\mu_o}$$

or

$$\frac{1}{L} = \frac{1}{L_c} + \frac{1}{L_g}$$

It is just like two inductors connected in parallel and the effective permeability, μ_e is given by

$$\frac{1}{\mu_e} = \frac{1}{\mu_r} + \frac{l_g}{l_c}$$

Then from the previous equation of the inductance

$$L = \frac{N^2}{\frac{l_c}{\mu_o A_c}\left(\frac{1}{\mu_r} + \frac{l_g}{l_c}\right)} = \frac{N^2 A_c \mu_o}{\frac{l_c}{\mu_r} + l_g}$$

Normally, for ferromagnetic materials, μ_r varies from 2000 to 6000 for the linear region of **B-H** curve (before saturation). Therefore, $(l_c/\mu_r) >> l_g$ and the effective (approximate) inductance is given by

$$L = \frac{N^2 A_c \mu_o}{l_g}$$

Therefore, for such type of magnetic circuits, air-gap reluctance dominates as the core reluctance is negligible, which is omitted. It simplifies the analysis and it does not much affect the accuracy. Now, $N = 1000$ turns, $\mu_o = 4\pi \times 10^{-7}$ H/m, $\mu_r = 4000$, $l_c = 10$ cm, $l_g = 1$ mm, $A = 2 \times 10^{-4}$ m^2. Therefore,

$$L = \frac{(1000)^2 \times 4\pi \times 10^{-7} \times 2 \times 10^{-4}}{0.1/4000 + 0.001} = 245.2 \text{ mH}$$

Also,

$$\Im = Ni = \phi\mathcal{R} = \frac{\phi}{A_c}A_c(\mathcal{R}_c + \mathcal{R}_g)$$

or

$$Ni \cong \mathbf{B}A_c\mathcal{R}_g = \mathbf{B}A_c\frac{l_g}{A_c\mu_o} = \frac{\mathbf{B}l_g}{\mu_o}$$

then

$$i = \frac{Bl_g}{N\mu_o}$$

To avoid saturation condition, **B** should be less than 1.2 tesla. Therefore,

$$i \le \frac{1.2l_g}{N\mu_o} = \frac{1.2 \times 10^{-3}}{1000 \times 4\pi \times 10^{-7}} = 0.95 \text{ A}$$

The current through the inductor should be less than 0.95 A.

SUMMARY

It is necessary to protect the power semiconductor devices from abnormal conditions for its satisfactory and reliable operation. The device damage or failure takes place due to temperature rise and not by heat, current or power dissipation. Actually, over-voltage, over-current or high-power dissipation in a device leads to temperature rise. The heat generated in the device across the junctions has to be dissipated for its safe and reliable operation. For the temperature above 50°C, each 10–15°C rise, increases junction thermal fatigue and reduces the reliability to a half. Normally, matt-black coloured aluminium heat sinks are used for this purpose. The flow of heat takes place by conduction, convection as well as by radiation. Forced cooling (forced convection) enormously accelerates the heat flow. Both air and liquid coolant (e.g. water) is used for this purpose. Thermal resistance models are used for estimation of heat flow and designing the heat sinks. Custom-built heat sinks are also available in the market for such applications.

The requirements of inductors and transformers in power electronic circuits vary over wide range on the basis of their performance. According to the costumer's need, these components are designed. Normally, soft magnetic materials (ferromagnetic and ferrimagnetic) are used for this purpose. Magnetic circuits of these components are designed according to the requirement. Normally, an air gap is purposely provided in all inductors, and transformers of flyback converters, to increase their energy-storage capability. The size of core materials and conductors is designed to reduce eddy-current loss and skin effect. Powdered-iron core materials and thin laminations are used to reduce eddy-current losses at a high frequency.

REVIEW QUESTIONS AND PROBLEMS

1. Why are heat sinks used?
2. How is the reliability of a device affected by temperature?
3. Why are heat sinks normally matt-black?
4. Why is silicon-grease used?
5. Why is mica sheet used between casing and heat-sink?
6. Why is resistance model used for heat flow?
7. What do you mean by transient thermal impedance?
8. Why is a rewirable fuse not suitable for the protection of power semiconductor devices?
9. Why is a crow-bar protection circuit used?
10. How does a temperature rise in a device affect its performance?
11. Why is fuse protection not adequate for devices from the transistor family?
12. What is significance of I^2t rating?
13. On what factors, convection and radiation of heat from heat-sink depend?
14. What is the significance of design of magnetic circuits/components in power electronics?

15. What types of core materials are used for high-frequency transformers?
16. Why are high-frequency transformers used?
17. How is the core of a flyback converter transformer different from the core of a normal isolation transformer?
18. What are limitations of increasing the air gap to enhance the energy-storage capacity in the above transformers?
19. What is need of resetting the core of isolation transformers?
20. Why are Litz wires used?
21. A maylor insulation sheet of 0.05-mm thickness is placed between a TO-5 package (casing) device and an aluminium heat sink. The mating surface area is 5 cm^2. The thermal resistivity of maylor is 635°C-cm/Watt. Find the thermal resistance and temperature rise in the maylor sheet for 20-Watt power dissipation in the device.
22. Find the inductance of a core structure as given in example 11.3, while the length of the core is reduced to a half, i.e. 5 cm. Comment on the result.

12

Simulation of Power Electronic Converters*

12.1 INTRODUCTION

Computers have long been used to create numerical and logical models or simulations of real-world systems. Indeed, a large part of the motivation for developing the first computers in the 1930s and 1940s was able to perform calculations to simulate and analyze physical systems, such as electrical circuits and the flight of artillery shells. Since then, computer simulation has become an indispensable tool of scientists, engineers, economists, and other people who work with, and desire to understand, the behaviour of complex systems.

In this chapter, the concept of simulation is discussed in detail with some examples. The importance and need for doing it in power electronics is discussed with various practical circuits and waveforms. A comparison of results is shown between the simulation and the real hardware circuit. Names of a few simulation tools are also mentioned.

12.2 IMPORTANCE OF SIMULATION

Simulation has become a very powerful tool in industry application as well as in academics, nowadays. It is now essential for an electrical engineer to understand the concept of simulation and learn its use in various applications. Simulation is one of the best ways to study the system or circuit behaviour without damaging it. The tools for doing the simulation in various fields are available in the market for engineering professionals. Many industries are spending a considerable amount of time and money in doing simulation before manufacturing their product. In most of the research and development (R&D) work, the simulation plays very important role. Without

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simulation, it is quite impossible to proceed further. It should be noted that in power electronics, (much more than in signal level electronics), computer simulation and a proof of concept hardware prototype in the laboratory are complimentary to each other. However, computer simulation should not be looked upon as a substitute for a hardware (breadboard) prototype.

In many cases, testing a real-world system can be prohibitively expensive or outrightly impossible. Seeing how the generator of a power plant is going to be damaged in a real system, is an example of an expensive exercise to conduct in reality. But by damaging the generator into a simulated fault condition, generator safety engineers can quickly evaluate potential designs and reduce the level of risk for it to sacrifice.

An example of an impossible-to-realize experiment would be estimating the environmental damage brought by an asteroid colliding with earth. At present, we lack the ability to conduct this experiment in actuality. But on a computer, we can safely slam simulated asteroids of all sizes and shapes into various parts of a simulated earth, all day long, without having to worry about triggering real-world mass extinction. Many systems are so complex that their correctness and behaviour cannot be easily or confidently predicted, either analytically or through experience and intuition. An integrated circuit (IC) is one example of such a system. For the device to function properly, tens or hundreds of thousands of individual circuits must operate exactly as planned. Isolating errors in the finished product can be difficult. For this reason, software vendors have developed numerous specialized circuit-simulation tools to let the designer simulate a circuit's performance on a computer under a variety of operating conditions and stimuli, and monitor the behaviour of the circuit at any point. Without such tools, the development of even moderately complex IC is vastly more difficult and expensive, and in many cases, nearly impossible. Beyond allowing engineers to see if their designs work, computer simulation allows the rapid comparison of alternative designs. By comparing the performance of various permutations of a given design, an engineer can optimize the performance, cost, or other desirable attributes of the design, subject to the constraints within which it must function.

12.2.1 Benefits of Computer-aided Simulation

Benefits of computer-aided analysis in power electronics circuits are enormous. They are listed as follows:

1. Evaluating the effects of variations in elements, such as resistors, power semiconductor devices, transformers, and so on
2. The assessment of performance, improvements or degradations
3. Evaluating the effects of noise and signal distortion without the need of expensive measuring instruments
4. Sensitivity analysis to determine the permissible bounds due to tolerances on each and every element value or parameter of active elements
5. Fourier analysis without expensive wave analyzers
6. Evaluating the effects of nonlinear elements on the circuit performance
7. Optimizing the design of electronic circuits in terms of circuit parameters.

12.2.2 Demerits of Computer-aided Simulation

We need to realize that there are several factors that make simulation of power electronic systems very challenging:

1. Solid-state power semiconductor switches including diodes and thyristors present extreme nonlinearity during their transition from one state to the other. The simulation programme ought to be able to represent this switching of states in an appropriate manner.
2. The simulation may take a long time. The time constants, or in other words the response time of various parts within the system, may differ by several orders of magnitude.
3. Accurate models are not always available. This is especially true for power semiconductor devices but is also the case for magnetic components, such as inductors and transformers.
4. The controller, which may be analog and/or digital, needs to be modelled along with the power converters.

12.3 WHAT IS SIMULATION?

Electronic circuit design requires accurate methods for evaluating circuit performance. Because of the enormous complexity of modern integrated circuits, computer-aided circuit analysis is essential and can provide information about circuit performance that is almost impossible to obtain with laboratory prototype measurement.

Analysis of a system with some tool without actually making the real system is known as *simulation*. For example, an engineer wants to design a simple full-bridge rectifier circuit then he needs to know the behaviour of his circuit in terms of rating of the components used and the output of the system. The engineer can do this, without going into the lab, just by sitting on his computer and using the software tool to run a simulation.

The simulation is done in various fields of engineering. Various tools are used in different areas of engineering. Power electronics is one of the engineering areas, where simulation plays a very important role. It contains various electronic circuits, whose behaviour should be known to the engineer.

With the advancement in software by introduction of graphic user interface (GUI) technology, the job of simulation tool developer's became easy.

The modelling of the components is done on the basis of their standard mathematical equations. Standard symbols are chosen for the components by using the GUI technology. After combining the above two things together the simulation field is revolutionized.

In the latter part of this chapter, some very important tools are mentioned which is commonly accepted by the engineers for the simulation study.

Main Tool Features

Normally, a simulation tool has large number of built-in facilities. It includes sources (power supplies, oscillators, signal generators, etc.), standard circuit configurations, specifications of commercially available semiconductor devices and facilities (instruments) for real-time estimation and measurement. These facilities, e.g. given in TINA^{pro}, can be classified as follows:

(a) Editing and tools presentation
- Schematic and Netlist
- TEXT, equation editor and interpreter

- Used defined excitation
- Annotation tools for presentation

(b) Analog, digital and mixed-mode simulation
- DC, AC and transient analysis
- Digital simulation
- Mixed circuit analysis
- Symbolic analysis

(c) Advanced analysis tools
- Fourier analysis (Fourier spectrum, Fourier series and distortion)
- Noise analysis (noise spectrum, signal to noise ratio etc.)
- Tolerance analysis (Monte Carlo and the worst-case analysis)
- RF network analyzer

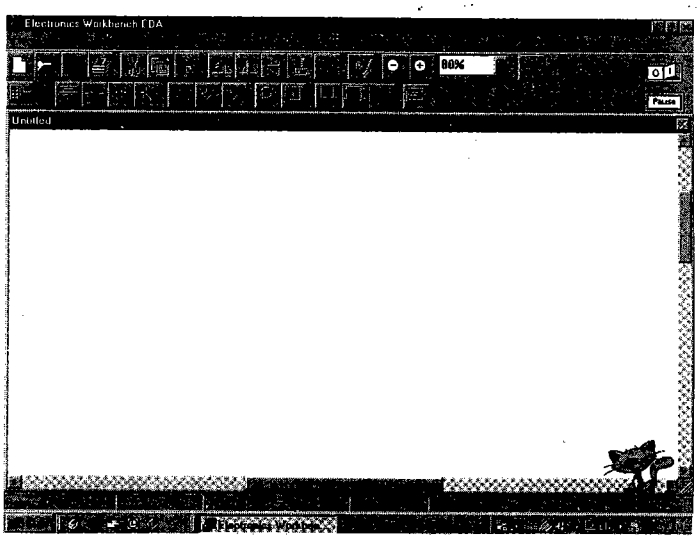
(d) Virtual instruments for real-time test and measurement
- Digital multimeter
- Storage oscilloscope
- Signal generator
- Signal analyzer
- Logic analyzer
- Network analyzer
- Signal and spectrum analyzer
- XY recorder
- Digital signal analyzer

(e) Library manager for SPICE and S-parameters
- 20,000 + built-in component models
- Spice library manager.

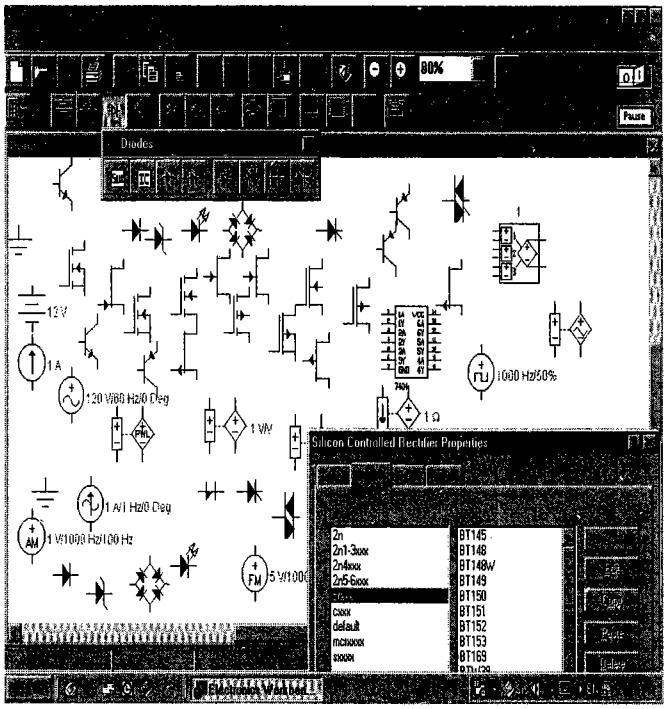
Figure 12.1 shows different facilities available with a typical tool, e.g. Electronics Workbench. Different icons of windows are available for different facilities. Similarly, specifications of standard/known commercially available devices are also available in the tool, e.g. there is a choice for diode (1N4001, 1N4002, BY127) or thyristor (2N3898, BT136) in a circuit. Both controller circuit and converter circuit can be analyzed simply by drawing the circuit on the workspace of screen using the drag-and-drop method and selecting different sources, devices, converters, instruments, etc. Similarly, function generators, CRO, storage oscilloscope (to capture transients), bode plotters, etc., can also be used at appropriate places.

12.4 SIMULATION TOOLS

Simulation of power electronic converters and circuits can be done, either by (i) circuit-oriented simulators (e.g. PSPICE, PSIM, TINA^{pro}, Electronics Workbench, etc.), or by (ii) mathematical-model based equation solvers—using high-level languages (e.g. C, C++, Visual BASIC, FORTRAN, BASIC), or high-level language-based packages (MATLAB, MATHEMATICA, etc.). In this section, a few software simulation tools are listed which are widely accepted by the engineering society, particularly by the electrical engineers. These simulation tools are in use in industries as well as in academic institutions.

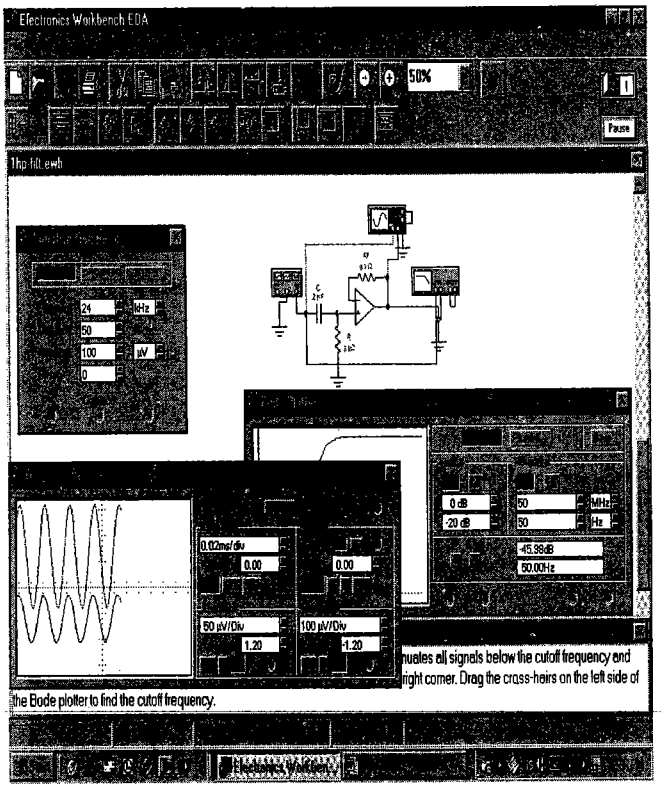


(a) Different facilities with EDA based Electronics Workbench simulation tool (courtesy: Electronics Workbench, website: WWW.electronicsworbench.com)



(b) Different icons and windows show different facilities available with the simulation tool which include different devices and data base of standard devices commercially available, e.g. thyristors/SCR/traic of 2N4xxx series and BTxxx (courtesy: Electronics Workbench, website: WWW.electronicsworbench.com)

Figure 12.1 (*Cont.*)



(c) Different windows show different facilities available with the simulation tool which include signal generators and measuring instruments, e.g. display of output by CRO/DSO, etc. (courtesy: Electronics Workbench, website: WWW.electronicsworkbench.com)

Figure 12.1 Different facilities available with Electronics Workbench EDA.

PSIPCE This tool is used for simulating the digital and analog circuits. The stability of the system and the optimization of the circuit components can also be done using this tool. This is the most powerful and popular tool for circuit level analysis. It has the model of most of the components in its library. The library of this software simulation tool is very broad. Waveforms at different points in power electronics circuit are very important to be known. Waveforms can be seen at various points in the circuit using this tool. Even the analysis of these waveforms in terms of Fourier transforms etc. can also be studied. The component-manufacturing vendors are giving readymade PSPICE model, which can be included in the library and can be used for the analysis. For example, Infineon, a manufacturer of semiconductor devices, has introduced a MOSFET and named COOL MOS. It has different additional features (as compared to conventional FET). They have given the PSPICE model of the new MOSFET. Similarly, almost every manufacturer gives the SPICE model for their components. This software package is in use for VLSI, power electronics and other circuit designs. In the next section, some examples are given using this tool.

Electronics Workbench This is another powerful tool from *Interactive Image Technologies Ltd.* It has a vast component library of electronic components and power semiconductor devices. It has

similar computational facilities. Figure 12.1 shows various features of the tool. The recently released package for this purpose is MULTISIM2001 from Electronics Workbench. It has schematic capture, simulation and programmable logic facilities.

PSCAD *Power systems computer aided design* (or PSCAD) is a package for simulating interactions between power electronic systems (converters, machine drives, static VAR controllers, HVdc, power supplies, etc.) and power systems. It is extensively used for study of HVdc systems. An evaluation version is available at http://www.pscad.com/.

PSIM *Power SIM* (or PSIM) is a package for motor drives and digital control simulation. Sample circuits are available for motor control, PF control, vector control (PWM) and SMPS. There is evaluation version available, which can be obtained from http://www.power simtech.com/.

PLECS *Piece-wise linear electrical circuit simulation* (or PLECS) is add-on for SIMULINK for dynamic systems. It converts a circuit into a *SIMULINK* subsystem. The package is available free at http://www.eeh.ee.ethz.ch/plecs/.

VTB *Virtual test bed* (or VTB) is a free package for multi-disciplinary dynamic systems (e.g. renewable energy systems, battery systems, fuel cells, super capacitors, etc.). It is available on http://vtb.engr.sc.edu/.

SABER This is a very powerful tool for simulation of analog circuits and systems, digital systems, event driven analog systems and mixed mode systems through all level of description from the highest structural level down to transistor level. With SABER's MAST language, even a combination of circuit blocks with different description levels in one model description is possible. For example, an electrical controller can be coupled with a mechanical system. Thus the overall performance of the whole system can be analyzed by SABER tools. A library is also provided with a number of predefined templates, which can be used as circuit hierarchy and a number of predefined components.

ONLINE SIMULATION Recently, Prof. Carlos A. Canesin of the Paulista State University, UNESP (Brazil) has developed a web-based power electronics educational tool for online simulation. It is an open WWW-HTML-based multimedia course in power electronics. The main purpose is to provide an interactive visual simulation and analysis of idealized uncontrolled and controlled rectifiers (single-phase and three-phase topologies). Moreover, JAVA applet programs were implemented to solve some design-oriented equations for rectifier applications. The emphasis is on interactive waveform analysis, stresses on devices, average and rms values of main circuit variables. It can be accessed free of charge at http;//www.dee.feis.unesp.br/LepApplets.

MATLAB and SIMULINK These are very powerful mathematical-model based equation-solver mathematical software tools. These are mainly used to study the system behaviour. In this package, the mathematical model of any system or component can be simulated in form of its equation. It is also a user-friendly tool, mainly used to study the behaviour of big systems by modelling it through their mathematical expressions. For example, a diesel based distributed/ dispersed generating (DG) system is a complex system, its performance can be analyzed by modelling computation using MATLAB/SIMULINK.

Recently WebMATHEMATICA package is also released by WOLFRAM Research, for online computation and visualization (www.wolfram.com/webmathematica).

There are many other tools, which are also available in the market and that can be tried to get the best design.

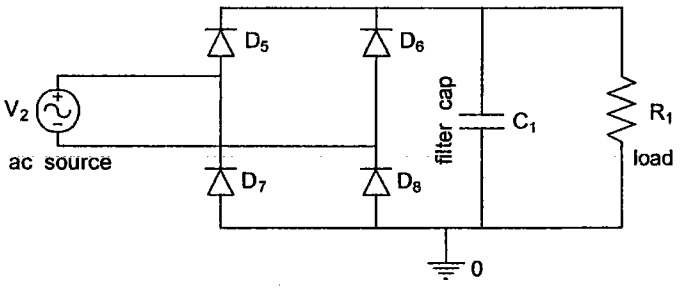
12.5

SOME EXAMPLES

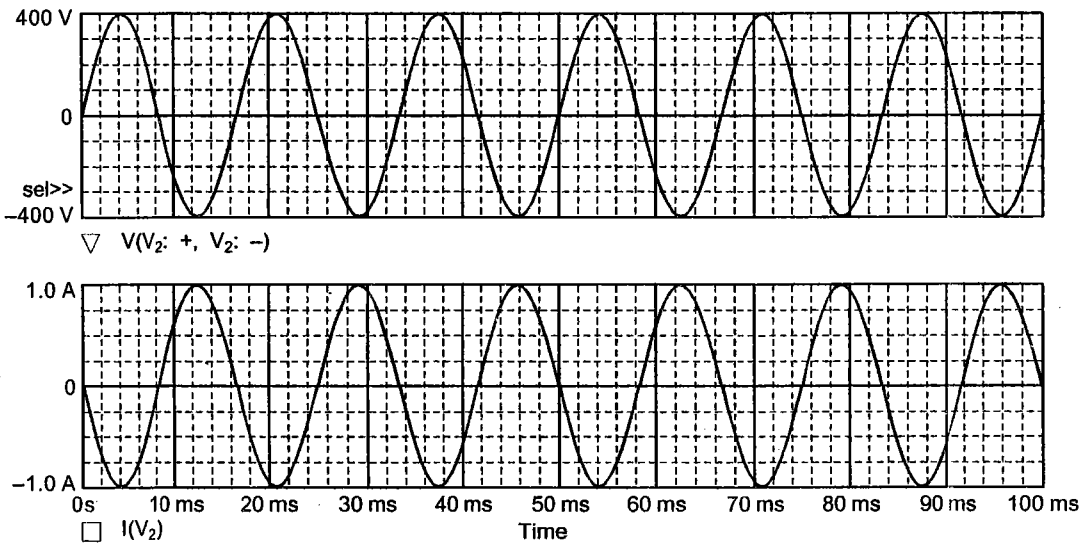
We discuss some simulation examples of simple electrical circuit to understand the functioning of simulation tools. The examples mentioned in Figs. 12.2–12.5 are based on the PSPICE simulation software package. The comparison is also done between the simulation and the actual CRO waveforms for some results.

12.5.1 Analysis of a Full-bridge Rectifier

The examples mentioned above is simulated in the PSPICE tool. It is a simple full-bridge rectifier circuit (Fig. 12.2a). After running the simulation it generates output files, and the desired output can be seen on the desktop of PC Fig. 12.2b and c. Figure 12.2b presents the waveforms of the input voltage and current and it is exactly same as of the actual circuit test condition in Fig. 12.2d.

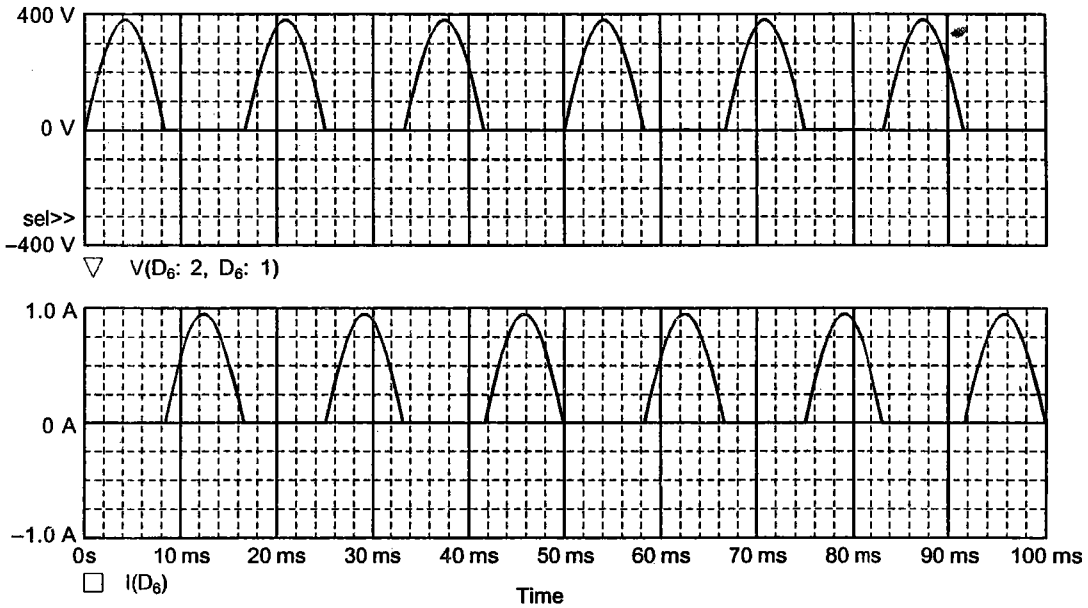


(a) Schematic of a full-bridge rectifier circuit in Pspice

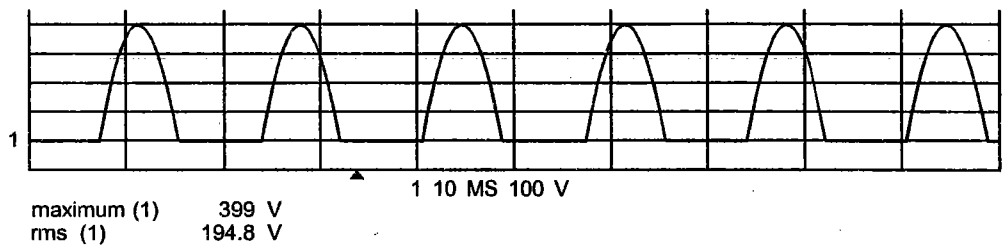


(b) Simulation result: waveform of input voltage and current

Figure 12.2 (*Cont.*)



(c) Simulation result: voltage and current across one of the rectifier diode



(d) CRO Result: (in actual circuit test) voltage across the rectifier diode

Figure 12.2 Analysis of a full-bridge rectifier.

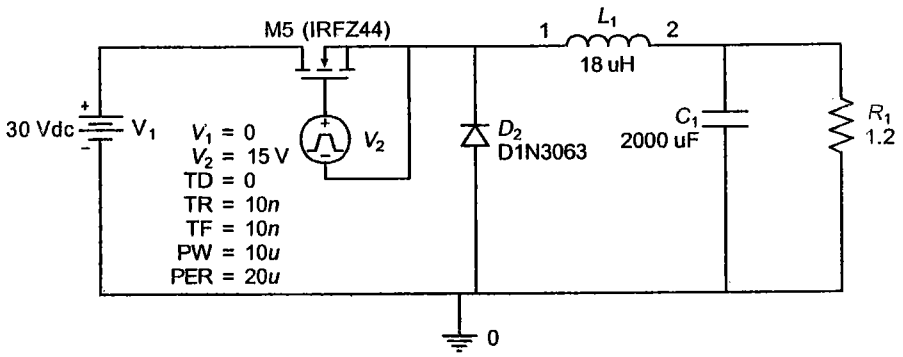
The components used are V_2, as ac voltage source; D_5, D_6, D_7, D_8, as simple diodes; C_1, as the filter capacitor and R_1, as load. (0 is the ground). All these components are available in Pspice library.

After running this simulation wave shape of the voltage and current can be seen at any point of the circuit.

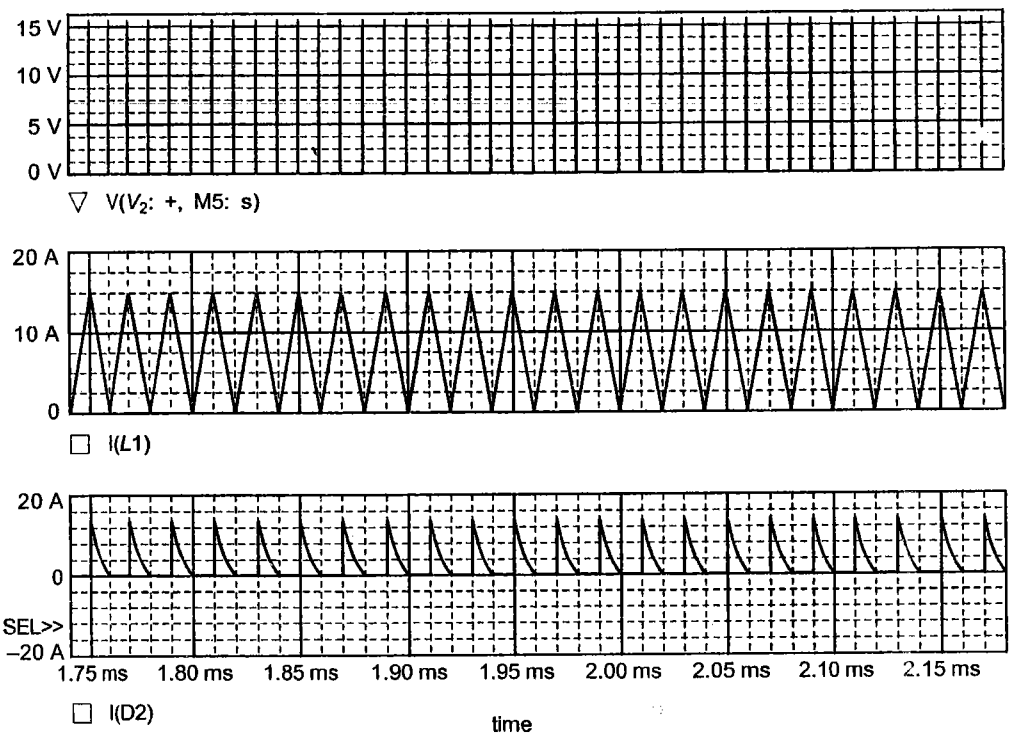
12.5.2 Analysis of a Buck Converter

This is an example of a simple buck converter, which is the most popular topology used in SMPS. A buck converter is used to get output voltage lower than the input voltage. It is basically stepping down of voltage without any transformer. In Fig. 12.3, the MOSFET is driven by the gate signal of frequency 50 kHz. The diode D_2, inductor L_1, the capacitor C_1 and the load R_1 are at the output end (Fig. 12.3a). These components are available in the library of Pspice. This particular circuit is designed for an output of 6 V with an input of 30 V (Fig. 12.3c). Figure 12.3b shows the electrical waveforms at the gate of MOSFET, current through L_1 and diode D_2.

The nature of current through L_1 and D_2 can be easily seen. Current through L_1 is rising when the MOSFET is on, and decreasing when it is off. A power electronics engineer can play with the values of L_1, C_1 and the frequency of operation for MOSFET and get the desired output just by sitting on computer. These results can be verified in the lab by assembling the actual circuit.

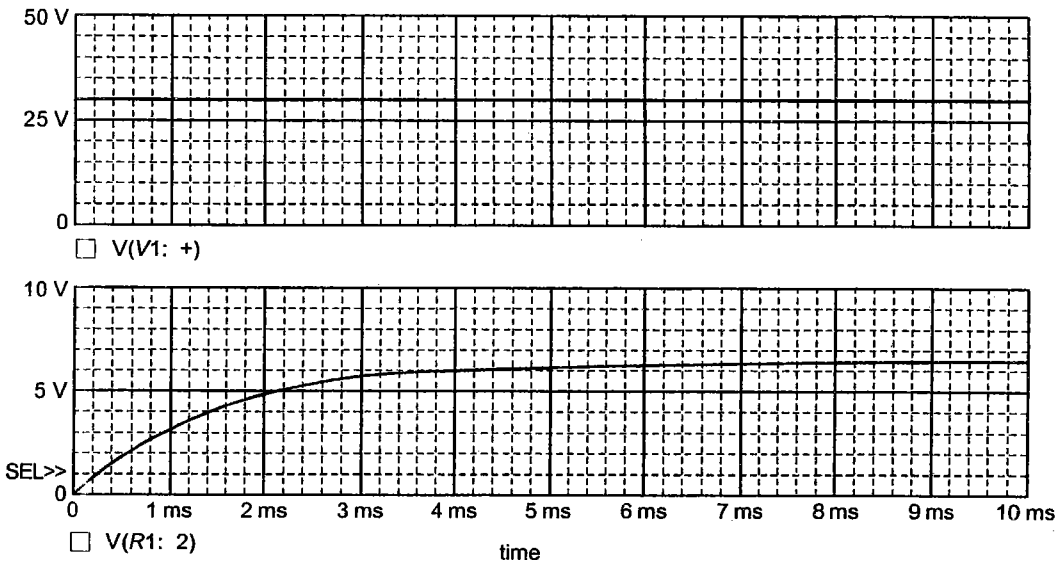


(a) Schematic of simple buck converter



(b) Simulation result: gate-source voltage of buck MOSFET M5, current through inductor L_1, current through diode D_2

Figure 12.3 (*Cont.*)

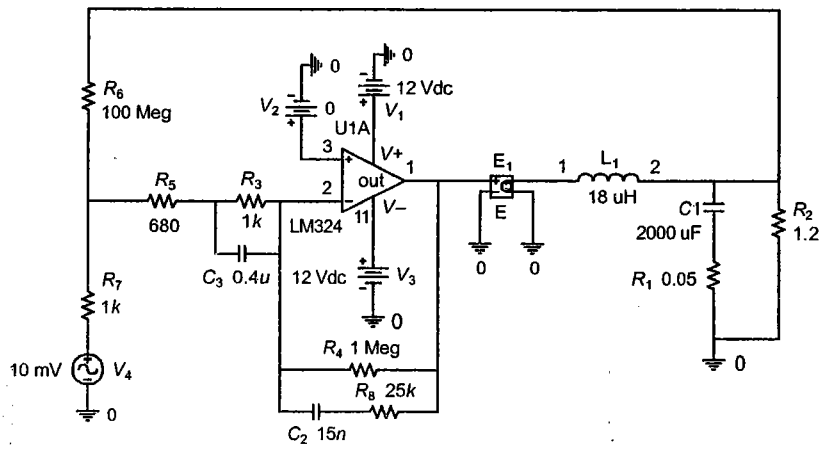


(c) Simulation result: input and output voltage

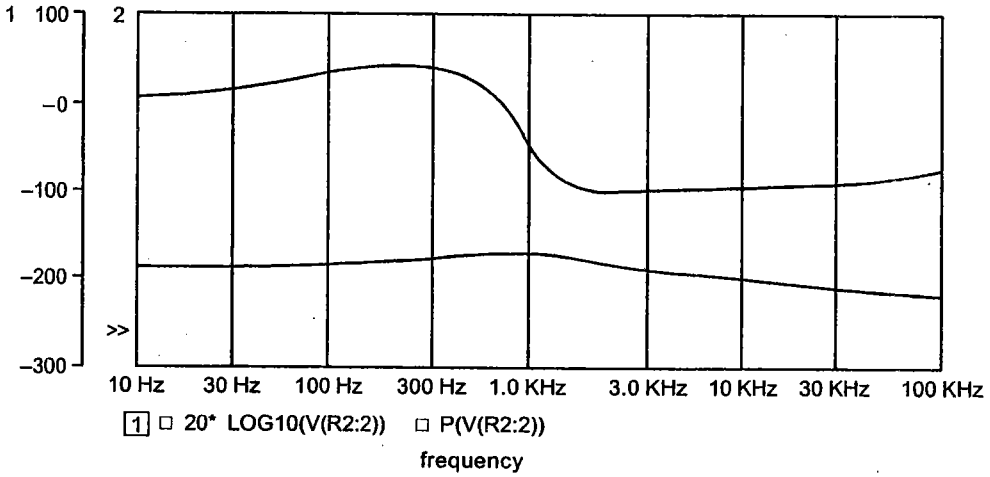
Figure 12.3 Analysis of a buck converter.

12.5.3 Dynamic Stability Analysis of a Buck Converter

PSPICE simulation tool can be used for studying the behaviour of a given circuit for its stability by using bode plot. A system needs a feedback loop in order to maintain the constant output. The regularization of output can be done by using a closed-loop system or with an open-loop system. It is very important for the designer to know whether the loop is stable or unstable during the operation. Generally, in any feedback system, amplifiers are used to regulate the output. There are various ways to check the stability of a system. Bode plot is one of them. Figure 12.4 shows a way to do a Bode plot study for a buck converter using PSPICE simulation tool.



(a) Schematic of an error amplifier for checking the dynamic stability analysis of a buck converter

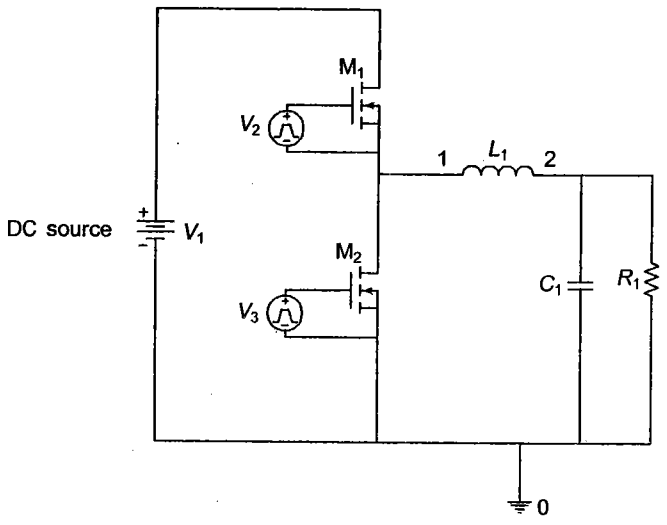


(b) Bode plot for study of stability using PSPICE simulation

Figure 12.4 Dynamic stability analysis of a buck converter.

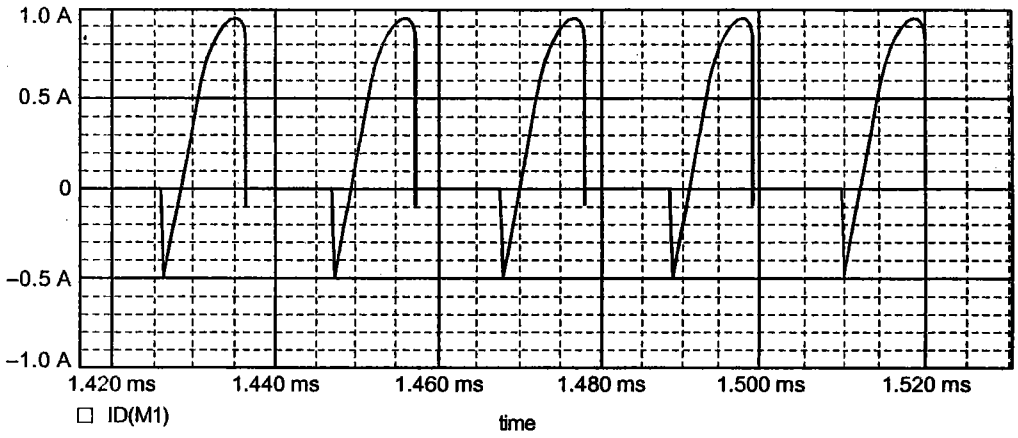
12.5.4 Analysis of a Half-bridge SMPS Topology

The schematic is shown in Fig. 12.5a, which contains one dc source, two MOSFETs and one inductor, capacitor and a resistive load. The plot of the drain current of the upper MOSFET M1 is shown Fig. 12.5b and it is compared with the actual circuit result on CRO (Fig. 12.5c). The gate signal of both the MOSFETs are also plotted to check the conduction (Fig. 12.5d).

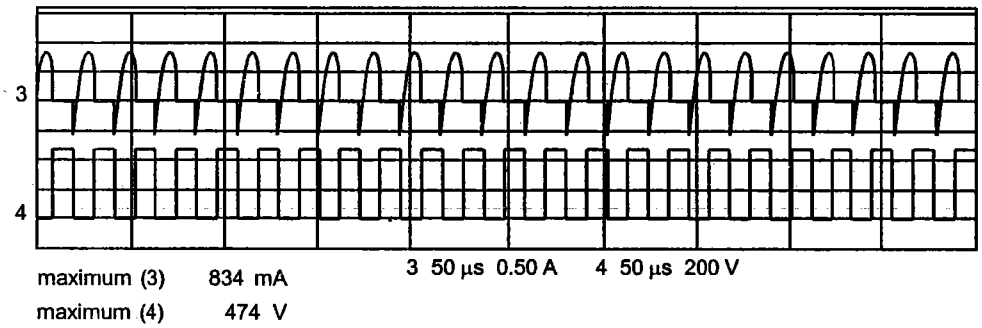


(a) Schematic of a half-bridge SMPS topology

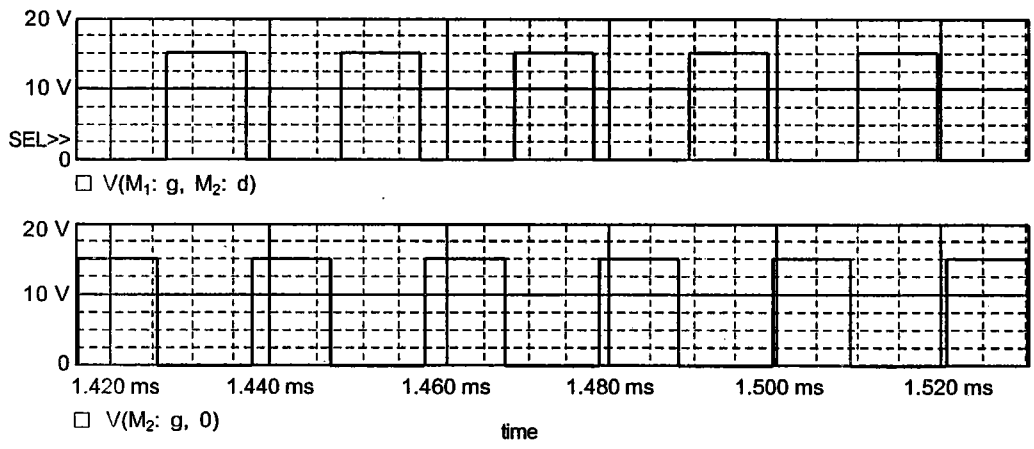
Figure 12.5 (*Cont.*)



(b) Simulation result: drain current of upper MOSFET



(c) CRO Result of drain current of MOSFET



(d) Simulation result: gate signal of upper and lower MOSFET

Figure 12.5 Analysis of a half-bridge SMPS topology.

SUMMARY

Simulation is very powerful tool for a comprehensive study of a power electronic system. Both circuit-oriented simulators and mathematical-model based equation-solvers are used.

Several examples are given to understand the concept of simulation. There are many more things about simulation that can be learnt by practice. This chapter mainly emphasizes the use of the circuit-oriented simulation tools for power electronic circuits.

PSPICE is one of the best platforms till date for the power electronics simulation. There are many other software simulation packages which are available in the market. These can be easily learnt by the engineers.

REVIEW QUESTIONS AND PROBLEMS

1. Why is simulation of power electronic circuits needed?
2. Compare different types of simulation tools.
3. What do you mean by the library of the simulation tool?
4. Why is hardware realization necessary, even after a successful simulation result?
5. Describe the facilities available with any simulation tool.
6. Using Pspice, TINApro or Electronics Workbench, show the current response of a full-wave diode rectifier circuit with an *RC* load. Using DSO, show the transient current (from the first cycle up to the third cycle).
7. Using Pspice or Electronics Workbench, show the input current and the output voltage of a uncontrolled, mid-point, full-wave rectifier or converter (diodes with a centre-tapped transformer). The output secondary voltage of the transformer is 200 V, at 50 Hz. The on-state forward resistance of diode is 15 Ω. Also, the load resistance is 1.5 kΩ. Find (i) the peak input current and (ii) the average load current.

Appendix

A1

DERIVATION OF CURRENT RESPONSE EQUATIONS WITH SUDDENLY APPLIED DIRECT (OR STEP) VOLTAGE

RL Circuits

Using Laplace transform, the current response equation of an *RL* circuit with a step input (dc) voltage (V) and a circulating current initial (I_0) at the switching instant (Fig. A1), can be easily derived. At $t = 0$, the switch is moved from A to B (ideally, within no time) to connect the load to the supply. The instantaneous current $i(t)$ in the circuit can be found using its voltage equation, which is given by

$$v_L(t) + v_R(t) = V \tag{A1}$$

where v_L and v_R are voltage drop across the inductor and resistor, respectively. Therefore,

$$L\frac{di(t)}{dt} + Ri(t) = V \tag{A2}$$

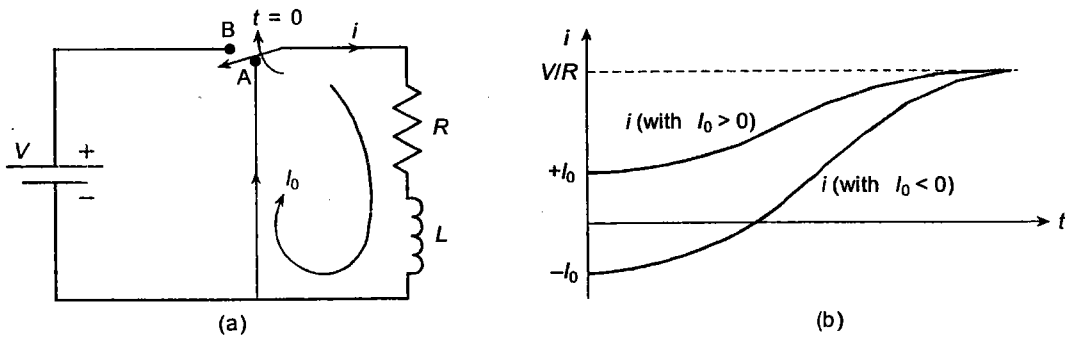


Figure A1 RL circuit with step (dc) input.

Taking Laplace transform,

$$\frac{V}{s} = RI(s) + L\,[sI(s) - I_0] \tag{A3}$$

or

$$I(s) = \frac{(V/L) + sI_0}{s[s + (R/L)]} = \frac{[V/(sR)] - [(V/R) - I_0]}{s + (R/L)} \tag{A4}$$

The complete expression for the instantaneous current is given by

$$i(t) = \frac{V}{R} - \left(\frac{V}{R} - I_0\right) e^{-Rt/L}$$

and

$$v_R(t) = i(t)R = V - (V - I_0R)\, e^{-Rt/L} \quad \text{and} \quad v_L(t) = V - v_R(t)$$

Figure A1(b) shows the current response for positive and negative values of I_0. The variation of v_R is same as i.

RLE Circuits

The current response equation for an *RLE* load connected with a step input (dc) voltage (V) and an initial circulating current (I_0), can also be found with the help of the previous equations. This condition appears when a dc chopper is used to control the speed of a dc motor by controlling the armature voltage (v_a), as shown in Fig. A2. During the on-period (T_{on}), the voltage equation is given by

$$v_a(t) = V = R_a i_a(t) + L_a \frac{di_a(t)}{dt} + E_b \tag{A5}$$

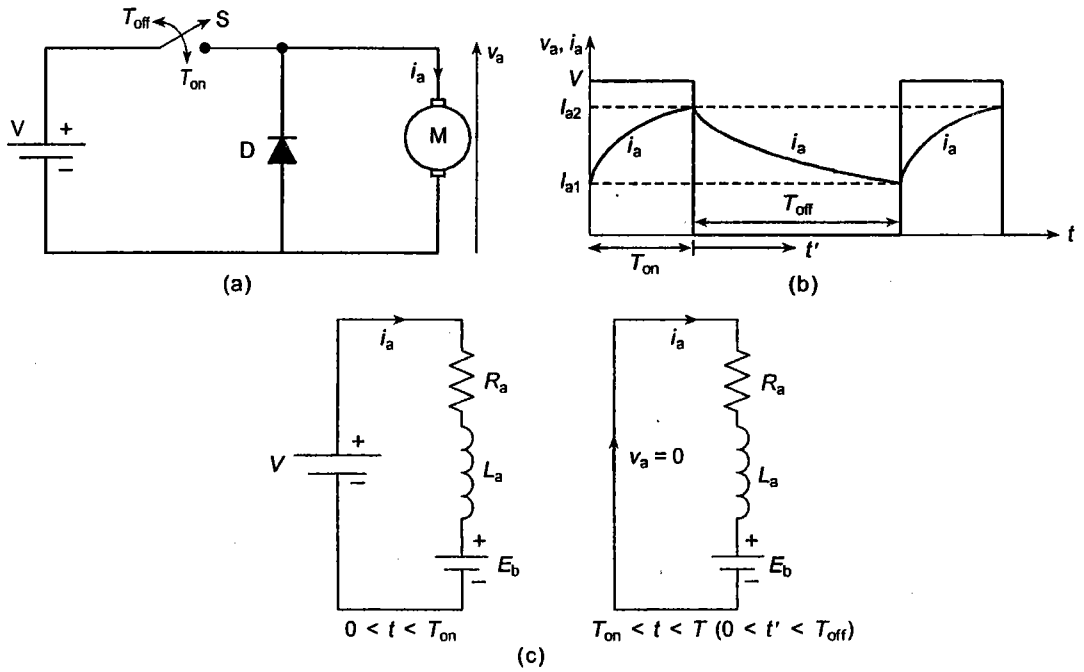


Figure A2 *RLE* loads with step (dc) input.

Thus,

$$i_a(t) = \frac{V - E_b}{R_a} - \left(\frac{V - E_b}{R_a} - I_{a1}\right)\exp\left(-\frac{R_a t}{L_a}\right) \tag{A6}$$

where I_{a1} is the initial value of i_a during the on-period (T_{on}).
Let I_{a2} is the maximum value of $i_a(t)$, therefore, at the end of on-period ($t = T_{on}$),

$$i_a(T_{on}) = I_{a2} = \frac{V - E_b}{R_a} - \left(\frac{V - E_b}{R_a} - I_{a1}\right)\exp\left(-\frac{R_a}{L_a} T_{on}\right) \tag{A7}$$

Since freewheeling period starts from $t = T_{on}$, therefore, the time reference can be shifted by T_{on}. If load current is continuous, the freewheeling diode conducts for the whole off-period (T_{off}). The voltage equation is given by

$$0 = R_a i_a(t') + L_a \frac{di_a(t')}{dt'} + E_b, \qquad \text{where } t' = t - T_{on} \tag{A8}$$

Therefore,

$$i_a(t') = -\frac{E_b}{R_a} - \left(-\frac{E_b}{R_a} - I_{a2}\right)\exp\left(-\frac{R_a t'}{L_a}\right) \tag{A9}$$

At the end of the off-period, at $t' = T_{off} = T - T_{on}$,

$$i(T - T_{on}) = I_{a1} = -\frac{E_b}{R_a} - \left(-\frac{E_b}{R_a} - I_{a2}\right)\exp\left[-\frac{R_a}{L_a}(T - T_{on})\right] \tag{A10}$$

Solving both equations (A7) and (A10) for I_{a1} and I_{a2},

$$I_{a1} = \frac{V}{R_a}\frac{\exp[(R_a/L_a)T_{on}] - 1}{\exp[(R_a/L_a)T] - 1} - \frac{E_b}{R_a} \tag{A11}$$

and

$$I_{a2} = \frac{V}{R_a}\frac{1 - \exp[-(R_a/L_a)T_{on}]}{1 - \exp[-(R_a/L_a)T]} - \frac{E_b}{R_a} \tag{A12}$$

For an RL load of a dc-to-dc converter ($E_b = 0$), the above equations may be simplified as

$$I_{a1} = \frac{V}{R_a}\frac{\exp[(R_a/L_a)T_{on}] - 1}{\exp[(R_a/L_a)T] - 1} \tag{A13}$$

and

$$I_{a2} = \frac{V}{R_a}\frac{1 - \exp[-(R_a/L_a)T_{on}]}{1 - \exp[-(R_a/L_a)T]} \tag{A14}$$

RC Circuits

The current response equation for an *RC* circuit with step input (dc) voltage (V) and an initial trapped charge (Q_0) or initial voltage (V_0), on the capacitor (Fig. A3), can be obtained from the voltage equation as given below

$$\frac{1}{C}\int i(t)\,dt + V_0 + Ri(t) = V \tag{A15}$$

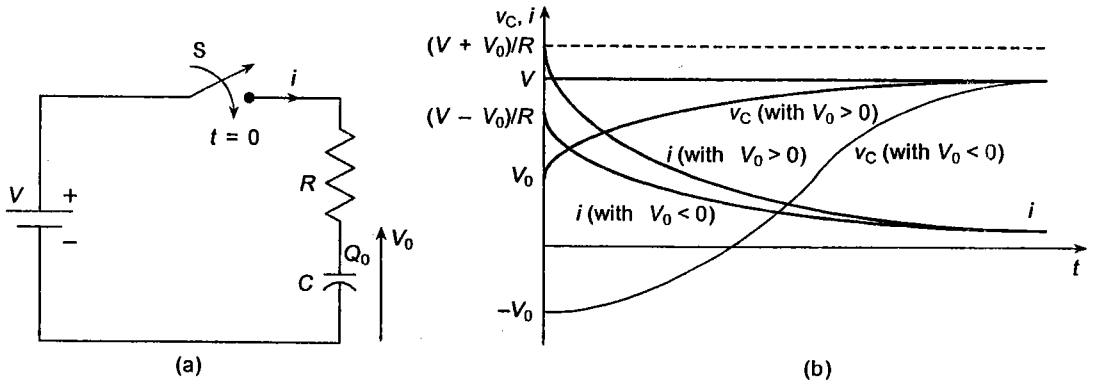


Figure A3 An *RC* series circuit with step (dc) input.

Taking Laplace transform,

$$\frac{V}{s} = \frac{I(s)}{sC} + \frac{V_0}{s} + RI(s) \tag{A16}$$

or

$$I(S) = \frac{(V - V_0)/s}{R + (C/s)} = \frac{V - V_0}{R\left[S + (1/RC)\right]} \tag{A17}$$

or

$$i(t) = \frac{V - V_0}{R}\, e^{-t/(RC)} \tag{A18}$$

Voltage across R,

$$v_R(t) = Ri(t) = (V - V_0)\, e^{-t/(RC)} \tag{A19}$$

At $t = 0$, the value of current is maximum,

$$I_0 = I_{max} = \frac{V - V_0}{R} \tag{A20}$$

However, if polarity of V_0 is opposite (upper plate of capacitor is negative), then

$$I_0 = I_{max} = \frac{V + V_0}{R} \tag{A21}$$

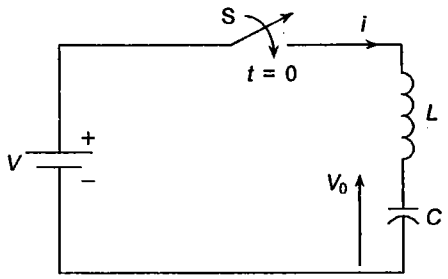
The voltage across capacitor is given by

$$v_C(t) = \frac{1}{C}\int_0^t i(t)\,dt = (V - V_0)[1 - e^{-t/(RC)}] \tag{A22}$$

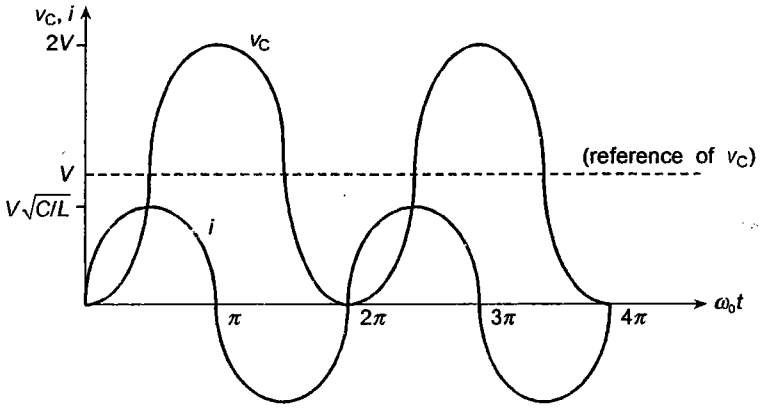
Undamped Series LC Circuits

When R is very small (or $R = 0$), an *RLC* under-damped circuit behaves as an *LC* resonating circuit. Let us consider an initial current, I_0 is circulating in the circuit and V_0 is initial voltage on the capacitor (Fig. A4). At $t = 0$, let the switch is moved instantaneously from A to B. The voltage equation is given by

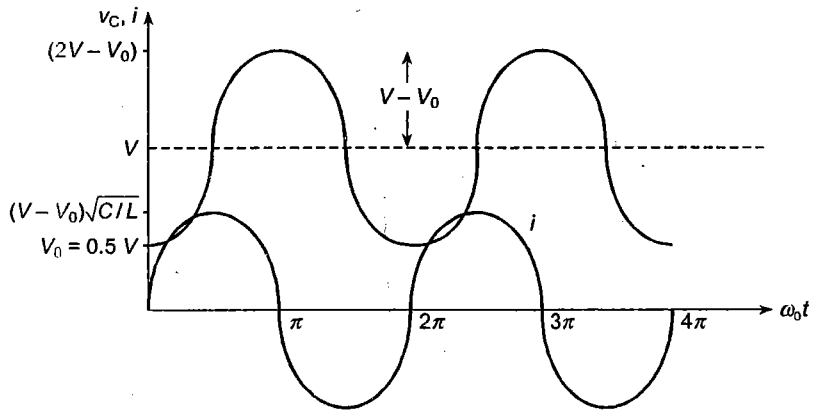
$$v_L(t) + v_C(t) = V \tag{A23}$$



(a) circuit



(b) $I_0 = 0$, $V_0 = 0$ (zero initial condition)



(c) $I_0 = 0$, $V_0 = 0.5\,V$

Figure A4 LC resonating circuits with step (dc) input.

With the initial condition, $i(t = 0) = I_0$ and $v_C(t = 0) = V_0$, the voltage equation is given by

$$L\frac{di(t)}{dt} + \frac{1}{C}\int i(t)\,dt + V_0 = V \tag{A24}$$

Taking Laplace transform,

$$\frac{V}{s} = L\left[sI(s) - I_0\right] + \frac{I(s)}{sC} + \frac{V_0}{s} \tag{A25}$$

or

$$\frac{V - V_0}{L} + sI_0 = I(s)\left(s^2 + \frac{1}{LC}\right) \tag{A26}$$

$$I(s) = \frac{V - V_0}{L\left(s^2 + (1/LC)\right)} + \frac{sI_0}{\left(s^2 + (1/LC)\right)} \tag{A27}$$

Then

$$i(t) = (V - V_0)\sqrt{\frac{C}{L}}\sin\frac{t}{\sqrt{LC}} + I_0\cos\frac{t}{\sqrt{LC}}$$

where the resonating angular frequency of the load current, $\omega_0 = 1/\sqrt{LC}$. Also,

$$v_C(t) = \frac{1}{C}\int_0^t i(t)\,dt + V_0 \tag{A28}$$

$$= V - (V - V_0)\cos\frac{t}{\sqrt{LC}} + I_0\sqrt{\frac{L}{C}}\sin\frac{t}{\sqrt{LC}} \tag{A29}$$

For zero initial condition ($I_0 = 0$, $V_0 = 0$),

$$i(t) = V\sqrt{\frac{C}{L}}\sin\frac{t}{\sqrt{LC}} = V\omega_0 C\sin\omega_0 t \tag{A30}$$

and

$$v_C(t) = V\left(1 - \cos\frac{t}{\sqrt{LC}}\right) = V(1 - \cos\omega_0 t) \tag{A31}$$

It is evident from the Fig. A4, that:

1. Both i and v_C oscillate (sinusoidal wave) and do not decay, as there is no damping element ($R = 0$).
2. The undamped, natural oscillation angular frequency, $\omega_o = 1/\sqrt{LC}$. At $\omega_o t = \pi$ or $T/2 = \pi\sqrt{LC}$, capacitor voltage (v_C) reaches to its peak value.
3. V_0 causes reduction or increase in the magnitude of current and voltage across each component, L or C.
4. I_0 has the same effect as V_0.
5. Both V_0 and I_0 cause change in amplitude of the current response and v_C, too.

6. For power electronic applications, where repeated switching takes place, normally only the first-cycle or first half-cycle is important. The damping-factor does not significantly modify the current response in the first cycle. Therefore, even a series *RLC* underdamped circuit (which is very common in power electronics), can be analyzed as a series *LC* circuit. It greatly simplifies the analysis.

UNDAMPED PARALLEL LC CIRCUITS

Let a dc current source is energizing a parallel *LC* resonant circuit, as shown in Fig. A5. The current equation is given by

$$i_L(t) + i_C(t) = I_0 \quad \text{or} \quad i_L(t) + C\frac{dv_C(t)}{dt} = I_0$$

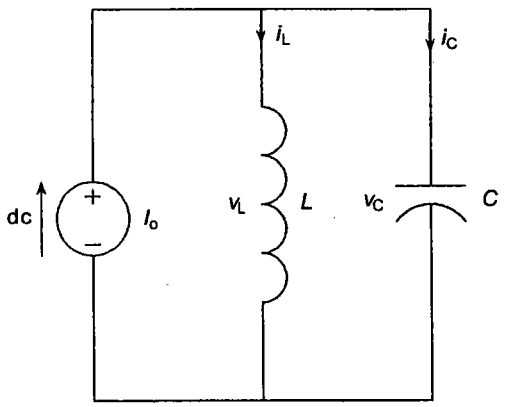


Figure A5 An *LC* parallel circuit with step (dc) input.

Also,

$$v_C(t) = v_L(t) = L\frac{di_L(t)}{dt}$$

Let the initial condition be $i_L(t = 0) = I_{L0}$ and $v_C(t = 0) = V_{C0}$, then the solution of the resonating current and voltage are given by

$$i_L(t) = I_0 + (I_{L0} - I_0)\cos\omega_o t + \sqrt{\frac{C}{L}}\, V_{C0}\sin\omega_o t$$

and

$$v_C(t) = \sqrt{\frac{L}{C}}\,(I_0 - I_{L0})\sin\omega_o t + V_{C0}\cos\omega_o t$$

With zero initial condition,

$$i_L(t) = I_0(1 - \cos\omega_o t) \quad \text{and} \quad v_C(t) = I_0\sqrt{\frac{L}{C}}\sin\omega_o t$$

It is evident that both the above quantities are purely sinusoidal. If a load resistance (R) is also connected in parallel, for the sake of simplification of analysis, it may be assumed that the voltage across the load is v_C. Therefore, the load current is equal to v_C/R which is also sinusoidal.

Series RLC Circuits

Let at switching instant, $i(0) = I_0$ and $v_C(0) = V_0$, the voltage equation of the series RLC circuit is given by

$$L\frac{di(t)}{dt} + Ri(t) + \frac{1}{C}\int i(t)\,dt + V_0 = V \tag{A32}$$

or

$$\frac{d^2i(t)}{dt^2} + \frac{R}{L}\frac{di(t)}{dt} + \frac{i(t)}{LC} = 0 \tag{A33}$$

The complete solution for the current is

$$i(t) = k_1 e^{(-a+b)t} + k_2 e^{(-a-b)t} \tag{A34}$$

where

$$a = \frac{R}{2L} \quad \text{and} \quad b = \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}$$

Let the initial charge on the capacitor, $\int i(t)dt = Q_0$ and the current at the switching instant of the circuit, $i(t = 0) = I_0$. Thus from (A34) and (A32), respectively

$$I_0 = k_1 e^0 + k_2 e^0 \tag{A35}$$

or

$$k_2 = I_0 - k_1 \tag{A36}$$

and

$$L\left(\frac{di}{dt}\right)_{t=0} + (RI_0 + V_0) = V \tag{A37}$$

or

$$L\,[(-a + b)\,k_1 + (-a - b)k_1] + (RI_0 + V_0) = V \tag{A38}$$

Thus, putting the value of k_2, from (A36) in (A37), we get

$$L\,[(-a + b)\,k_1 + (-a - b)\,I_0 - (-a - b)\,k_1] + (RI_0 + V_0) = V \tag{A39}$$

or

$$k_1 = \frac{V - V_0 + \left[a + b - (R/L)\right] I_0}{2bL} \tag{A40}$$

$$= \frac{V - V_0 + (-a + b)\,I_0}{2bL} \tag{A41}$$

The transient term in (A35) becomes

$$i(t) = \{k_1[e^{(-a+b)t} - e^{(-a-b)t}] + I_0 e^{(-a-b)t}] \tag{A42}$$

or

$$i(t) = e^{-at}\,[k_1(e^{bt} - e^{-bt}) + I_0 e^{-bt}] \tag{A43}$$

Thus, the circuit may be an overdamped, under-damped or critically damped (Fig. A6). The current response is given by

$$i(t) = [2k_1 \sinh bt + I_0 e^{-bt}]\, e^{-at} \qquad \text{(for over-damped circuits)} \tag{A44}$$

and

$$i(t) = [2k_1 \sin \beta t + I_0 e^{-\beta t}]\, e^{-at} \qquad \text{(for under-damped circuits)} \tag{A45}$$

where

$$2 \sinh bt = e^{bt} - e^{-bt} \quad \text{and} \quad 2 \sin \beta t = e^{j\beta t} - e^{-j\beta t}$$

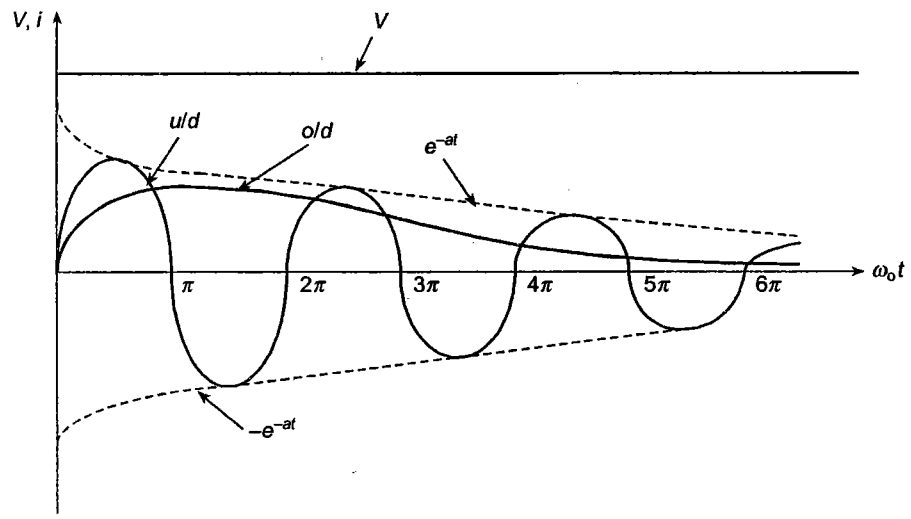


Figure A6 The current response of under-damped and over-damped series *RLC* circuits with step (dc) input.

The resonating frequency,

$$\omega_r = \beta = jb = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

Also

$$\xi = \text{Damping ratio} = (R/2)\sqrt{C/L} \tag{A46}$$

$$\omega_0 = \text{angular undamped natural frequency} = 1/\sqrt{LC} \tag{A47}$$

ω_r = angular damped resonating or oscillating frequency,

$$\beta = \omega_0\sqrt{(1 - \xi^2)}, \quad \alpha = a = \frac{R}{2L} = \frac{R}{2}\sqrt{\frac{C}{L}}\,\frac{1}{\sqrt{LC}} = \xi\omega_0 \tag{A48}$$

Then for the zero initial condition, the current response of a series *RLC* underdamped circuit is given by

$$i(t) = 2k_1 e^{-\alpha t} \sin \beta t \tag{A49}$$

or

$$i(t) = \frac{V}{\omega_0 L} \exp(-\xi\omega_0 t) \sin \omega_r t \tag{A50}$$

A2

DERIVATION OF CURRENT RESPONSE WITH ALTERNATING VOLTAGE INPUT

RL Circuits

Let the switch, S is moved from A to B at $\omega t = \alpha$, such that at initial condition, I_0 flows in the *RL* circuit (Fig. A7). The voltage equation is given by

$$R_i(t) + L\frac{di(t)}{dt} = v(t) = V_m \sin \omega t, \qquad \text{where } \omega t \geq \alpha \tag{A51}$$

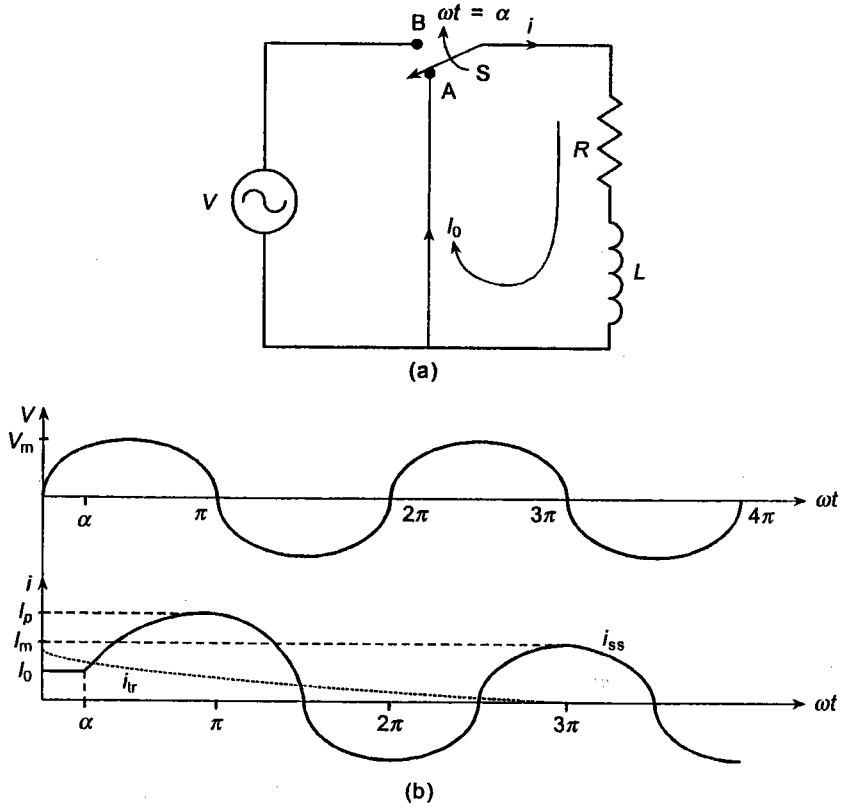


Figure A7 An RL circuit with sinusoidal input.

There are two component of the solution, i.e. steady-state part (i_{ss}), and the transient part (i_{tr}). The solutions are:

$$i(\omega t) = i_{ss}(\omega t) + i_{tr}(\omega t) \tag{A52}$$

and

$$i(\omega t) = I_m \sin(\omega t - \phi) - [I_m \sin(\alpha - \phi) - I_0]e^{(\alpha - \omega t)\cot\phi} \tag{A53}$$

where I_m is the steady-state maximum value of current,

$$I_m = \frac{V_m}{\sqrt{R^2 + (\omega L)^2}} \quad \text{and} \quad \phi = \tan^{-1}\frac{(\omega L)^2}{R}$$

Then

$$i(t) = I_m\left\{\sin(\omega t - \phi) - [\sin(\alpha - \phi) - \eta]e^{(\alpha-\omega t)\cot\phi}\right\}, \quad \text{where } \eta = \frac{I_0}{I_m} \tag{A54}$$

The transient term causes a dc offset in the current (Fig. A7). The surge or peak (I_P) value of the current becomes double of I_m for a purely inductive circuit. In the presence of I_0, I_P increases or decreases according to the positive or negative polarity of I_0, respectively.

RC Circuits

Let the switch, S, is closed at $\omega t = \alpha$, such that a trapped voltage on the capacitor is V_0 (Fig. A8). The voltage equation is given by

$$v(\omega t) = V_m \sin \omega t, \qquad \text{where } \omega t \geq \alpha$$

Then

$$Ri(t) + \frac{1}{C}\int_0^t i(t)\,dt + V_0 = v(\omega t) = V_m \sin \omega t, \qquad \text{where } \omega t \geq \alpha \tag{A55}$$

The complete expression for the current is,

$$i(\omega t) = I_m \sin(\omega t + \phi) - \tan\phi[\omega c V_0 + I_m \cos(\alpha + \phi)] \exp[(\alpha - \omega t)\tan\phi] \tag{A56}$$

where,

$$I_m = \frac{V_m}{\sqrt{R^2 + [1/(\omega c)]^2}}, \qquad \phi = \tan^{-1}\frac{1}{\omega CR}$$

Also

$$i(\omega t) = I_m[\sin(\omega t + \phi) - \tan\phi\{\gamma + \cos(\alpha + \phi)\} \exp\{(\alpha - \omega t)\tan\phi\}] \tag{A57}$$

where

$$\gamma = \frac{V_0 \omega C}{I_m} = \frac{V_0}{X_C I_m} = \frac{V_0}{V_{Cm}}$$

which is equivalent to the ratio of initial voltage (V_0) to the maximum voltage on capacitor (V_{Cm}) at steady-state condition. In this case, although the transient term dies quickly but the transient current peak (I_p) may be very large, almost equal to $(V_m \pm V_0)/R$. Therefore, for high value of ϕ (low PF), I_P may be several times of I_m. Figure A8(c) shows the effect of V_0 (positive or negative) on the current response.

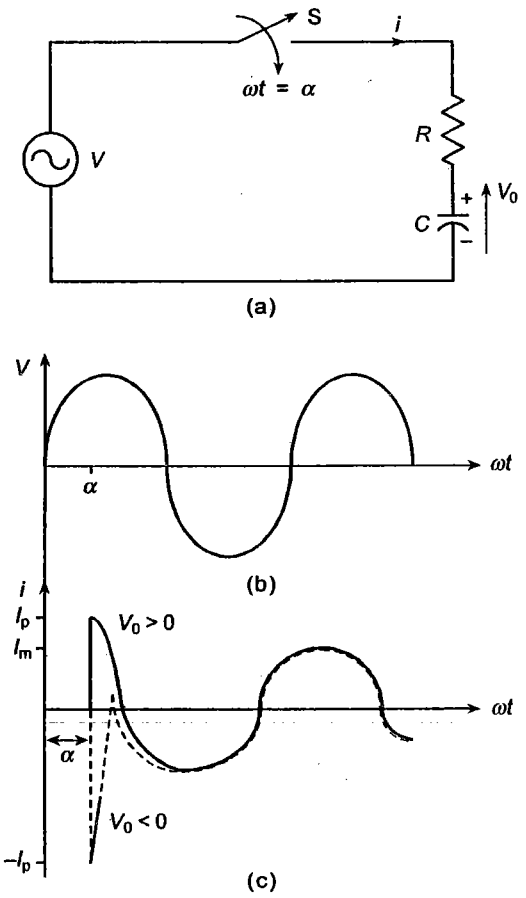


Figure A8 An *RC* circuit with sinusoidal input.

RLC Circuits with I_0, V_0

The current response of a series *RLC* circuit with ac voltage input, initial circulating current (I_0) and trapped voltage (V_0) on capacitor at the switching instant, can be found by the voltage equation, which is given by

$$L\frac{di(t)}{dt} + Ri(t) + \frac{1}{C}\int i(t)\,dt = V_m \sin \omega t \tag{A58}$$

or

$$\frac{d^2i}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{i}{LC} = \frac{\omega V_m}{L}\cos \omega t \tag{A59}$$

The complete expression for an inductive series *RLC* circuit ($X_L > X_C$), is the sum of steady-state term and the transient term,

$$i(\omega t) = I_m \sin(\omega t - \phi) + c_1 e^{(-a+b)t} + c_2 e^{(-a-b)t} \tag{A60}$$

where

$$X_L = \omega L, \quad X_C = \frac{1}{\omega C}, \quad \phi = \tan^{-1}\frac{X_L - X_C}{R}, \quad Z = \sqrt{R^2 + (X_L - X_C)^2}, \quad I_m = \frac{V_m}{Z}$$

Let V_0 and I_0 are present at the switching instant of the circuit ($\omega t = \alpha$). Thus, from (A51) and (A58), respectively

$$c_2 = -[I_m \sin(\alpha - \phi) - I_0] - c_1 \tag{A61}$$

and

$$L\left[\frac{di}{dt}\right]_{t=0} + RI_0 + V_0 = V_m \sin\alpha \tag{A62}$$

or

$$L[\omega I_m \cos(\alpha - \phi) + (-a + b)c_1 + (-a - b)c_2] + RI_0 + V_0 = V_m \sin\alpha \tag{A63}$$

Thus, from (A63) and (A60),

$$c_1 = \frac{E_0}{2bL} - \frac{1}{2}[I_m \sin(\alpha - \phi) - I_0] \tag{A64}$$

and

$$c_2 = -\frac{E_0}{2bL} - \frac{1}{2}[I_m \sin(\alpha - \phi) - I_0] \tag{A65}$$

where

$$E_0 = V_m \sin\alpha - \omega L I_m \cos(\alpha - \phi) - V_0 - \frac{R}{2}[I_m \sin(\alpha - \phi) + I_0] \tag{A66}$$

The transient term in (A60) becomes

$$\left\{\frac{E_0}{bL}\frac{e^{bt} - e^{-bt}}{2} - [I_m \sin(\alpha - \phi) - I_0]\frac{e^{bt} + e^{-bt}}{2}\right\} e^{-at} \tag{A67}$$

Thus, putting the values of c_1 and c_2 in (A61), we get for over-damped series *RLC* circuits

$$i(\omega t) = I_m \sin(\omega t - \phi) + \left\{\frac{E_0}{bL}\sinh bt - [I_m \sin(\alpha - \phi) - I_0]\cosh bt\right\} e^{-at} \tag{A68}$$

For critically damped series *RLC* circuits

$$i(\omega t) = I_m \sin(\omega t - \phi) + \left\{\frac{E_0 t}{L} - [I_m \sin(\alpha - \phi) - I_0]\right\} e^{-at} \tag{A69}$$

Similarly, for under-damped RLC circuits

$$i(\omega t) = I_m \sin(\omega t - \phi) + \left\{\frac{E_0}{\beta L}\sin\beta t - [I_m \sin(\alpha - \phi) - I_0]\cos\beta t\right\} e^{-at} \tag{A70}$$

where

$$\beta = jb = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

Here, under-damped and over-damped circuits have transient terms, like the current response of under-damped and over-damped *RLC* circuits energized by a dc source (discussed earlier). From the current response equation, it is evident that the decaying transient term is not constant. Therefore, the steady-state waveform superimposes over the transient-term waveform. If this *RLC* circuit is an under-damped circuit (which is common), the transient term is oscillating and the oscillation is related to β. That is, the transient oscillating current of frequency, β superimposes over the steady state magnitude. For an over-damped circuit, there is a non-uniform decaying offset current (represented by the transient term). The steady-state response term will be superimposed over that.

A3

SPECIFICATIONS OF DIFFERENT USEFUL DEVICES*

High Voltage Power MOSFET/IGBT Gate Drivers (IR2100/2000 Series)

Figure A9 shows the block diagram of various parts of a gate driver circuit. Following are important features of such drivers:

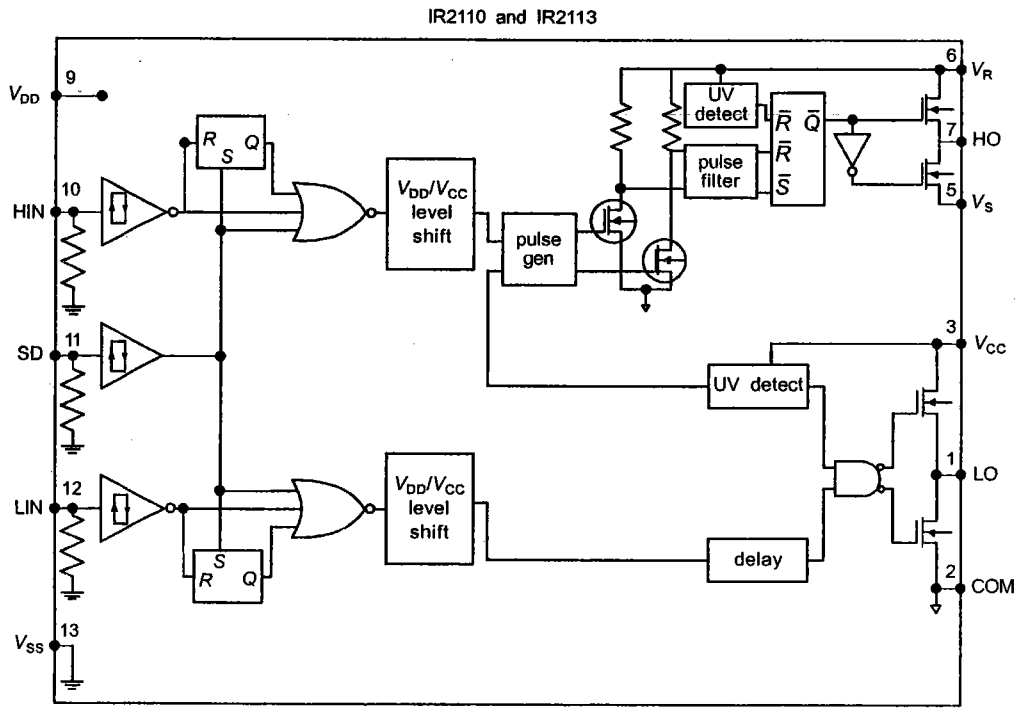


Figure A9 Custom-built gate driver IC (courtesy: International Rectifiers).

*Courtesy: International Rectifier, website: www.irf.com.

- Drives single, pair, and six (for upper device of a half or full-bridge) MOSFET or IGBT
- Floating high side driver
- Ground referenced low side driver
- Operates to either 500 V or 600 V
- High *dv/dt* and negative transient immunity
- CMOS compatible schmitt trigger inputs
- Low quiescent power dissipation
- Undervoltage lockout with hysteresis (for all channels)
- Matched delay times for high and low channels (blanking)
- Latch immune CMOS.

These gate driver IC are designed for general and specific applications.

General type: IR2110, IR2111, IR2112

Special type: IR2113

- For buck-boost converters: IR2125
- For 3-phase, six-step, PWM: IR2130, IR2132
- For square-wave and high-voltage, IR2111
- For resonant and phase-shifted PWM: IR2112, 2113
- For oscillating application converters: IR2155

Special type: IR2000 series (1 MHz operation)
For high power digital/analog audio amplifiers (push-pull) or bridge converters: IR2010.
Various devices of International Rectifiers and their configurations are given in Table A1.

Table A1 Different Types of Driver ICs

Part number	*Configuration*	*Maximum floating supply offset voltage*	*I_o source, sink*	*Schametic*	*(1) Case outline*	*Case style*
IR2110	High side and low side	500 V	2 A/2 A	S1	P1	14 pin DIP
IR2110-1					P2	14 pin DIP w/o pin 4
IR2110-2					P3	16 pin DIP w/o pins 4 & 5
IR2110S					P4	16 pin SOIC wide body
IR2111	Half bridge	600 V	200/420 mA	S3	P5	8 pin DIP
IR2112	High side and low side	600 V	200/420 mA	S2	P1	14 pin DIP
IR2112-1					P2	14 pin DIP w/o pin 4
IR2112-2					P3	16 pin DIP w/o pins 4 & 5
IR2112S					P4	16 pin SOIC wide body

Nomenclature Code

To show ratings and other details, a systematic numbering system is adopted by manufactures of devices. Normally, it varies form manufacturer to manufacturer (Fig. A10).

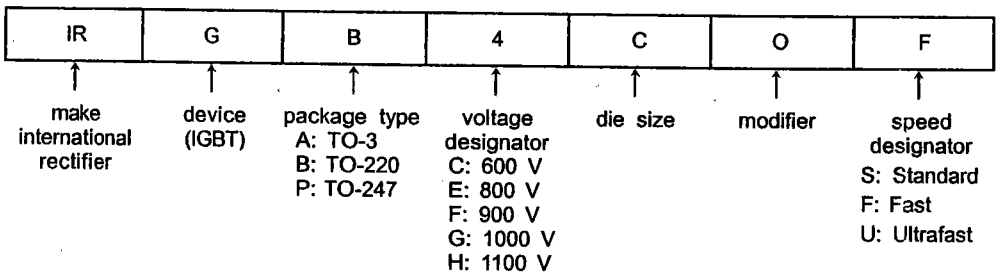


Figure A10 Nomenclature code for IGBT of International Rectifiers.

A4

SPECIFICATION OF IRGBC30S SERIES IGBT*

Specification of a typical IGBT is given below.
Refer to Tables A2–A5.

Table A2 Absolute Maximum Ratings

	Parameter	*Maximum*	*Units*
V_{CES}	Collector-to-emitter voltage	600	V
I_C @ T_C = 25°C	Continuous collector current	34	A
I_C @ T_C = 100°C	Continuous collector current	18	A
I_{CM}	Pulsed collector current (1)	68	A
I_{LM}	Clamped inductive load current (2)	68	A
V_{GE}	Gate-to-emitter voltage	±20	V
E_{ARV}	Reverse voltage avalanche energy (3)	10	mJ
P_D @ T_C = 25°C	Maximum power dissipation	100	W
P_D @ T_C = 100°C	Maximum power dissipation	42	W
T_j, T_{STG}	Operating junction and storage temperature range	–55 to +150	°C
	Soldering temperature, for 10 s Mounting torque, 6–32 or M_3 screw	300 [0.063 in. (1.6 mm) from case] 10 lbf.in (1 N-m)	°C

Table A3 Thermal Resistance

	Parameter	*Type*	*Maximum*	*Units*
$R_{\theta JC}$	Junction-to-case		1.2	°C/W
$R_{\theta CS}$	Case-to-sink, flat, greased surface	0.56		
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount		80	
Wt	Weight	2.0 (0.07)		g (oz)

*Courtesy: International Rectifier, website: www.irf.com.

Table A4 Switching Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	*Type*	*Maximum*	*Units*	*Conditions*
Q_g	Total gate charge (turn-on)	28	40	nC	I_C = 18 A V_{CC} = 400 V
Q_{ge}	Gate-emitter charge (turn-on)	5.0	8.0	nC	V_{GE} = 15 V
Q_{gc}	Gate-collector charge (turn-on)	12	20	nC	
$t_{d(on)}$	Turn-on delay time	26		ns	T_j = 25°C
t_r	Rise time	32		ns	I_C = 18 A,
$t_{d(off)}$	Turn-off delay time	820	1100	ns	V_{CC} = 480 V
t_f	Fall time	720	1200	ns	V_{GE} = 15 V,
E_{on}	Turn-on switching loss	0.51		mJ	R_G = 23 Ω
E_{off}	Turn-off switching loss	6.6		mJ	energy losses
E_{ts}	Total switching loss	7.1	10	mJ	include 'tail'
$t_{d(on)}$	Turn-on delay time	26		ns	T_j = 150°C I_C = 18 A, V_{CC} = 480 V V_{GE} = 15 V, R_G = 23 Ω energy losses include 'tail'
t_r	Rise time	35		ns	
$t_{d(off)}$	Turn-off delay time	1200		ns	
t_f	Fall time	1500		ns	
E_{ts}	Total switching loss	12		mJ	
L_E	Internal emitter inductance	7.5		nH	Measured 5 mm from package
$C_{i\theta s}$	Input capacitance	700		pF	V_{GE} = 0 V V_{CC} = 30 V F = 1.0 MHz
$C_{o\theta s}$	Output Capacitance	70		pF	
$C_{r\theta s}$	Reverse transfer capacitance	9.2		pF	

Table A5 Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	*Minimum*	*Type*	*Maximum*	*Units*	*Conditions*
$V_{(BR)CES}$	Collector-to-emitter breakdown voltage	600			V	V_{GE} = 0 V, I_C = 250 μA
$V_{(BR)ECS}$	Emitter-to-collector breakdown voltage (4)	20			V	V_{GE} = 0 V, I_C = 1.0 A
$\Delta V_{(BR)CES}/\Delta T_j$	Temperature coefficient of breakdown voltage		0.75		V/°C	V_{GE} = 0 V, I_C = 1.0 mA

(*Cont.*)

Table A5 (Cont.)

	Parameter	Minimum	Type	Maximum	Units	Conditions
$V_{CE(on)}$	Collector-to-emitter saturation voltage		1.7	2.2	V	I_C = 18 A, V_{GE} = 15 V
			2.4		V	I_C = 34 A
			1.9		V	I_C =18 A, T_j = 150°C
$V_{GE(th)}$	Gate threshold voltage	3.0		5.5	V	V_{CE} = V_{GE}, I_C = 250 μA
$\Delta V_{GE(th)}/\Delta T_j$	Temperature coefficient of threshold voltage		−11		mV/°C	V_{CE} = V_{GE}, I_C = 250 μA
g_{fe}	Forward transconductance (5)	6.0	11		S	V_{CE} = 100 V, I_C = 18 A
I_{CES}	Zero gate voltage collector current			250	μA	V_{GE} = 0 V, V_{CE} = 600 V
I_{GES}	Gate-to-emitter leakage current			±100	nA	V_{GE} = ±20 V

Requirements for Snubber Capacitors

Requirements for snubber capacitors for thyristors and diodes are given in Table A6.

Table A6 Requirements for Snubber Capacitors

Device rated current (A)	*Snubber capacitor (μF)*
1	0.022
3	0.1
10	0.33
30	0.5
100	1
>100	1 to 2

A5

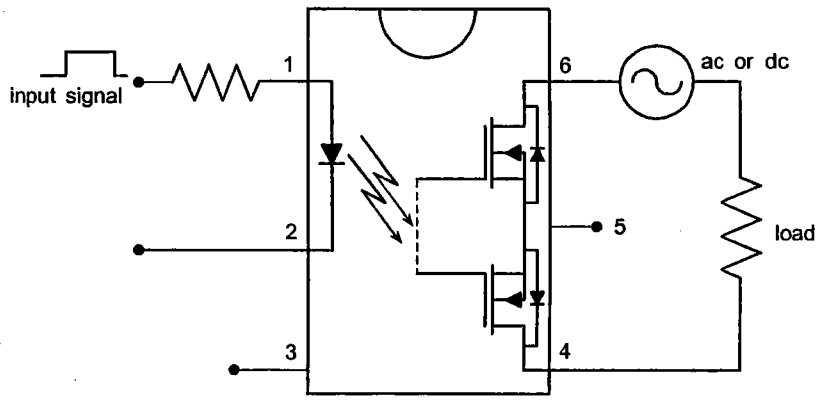
MICROELECTRONICS RELAYS AND INTELLIGENT POWER SWITCHES

For industrial control, instrumentation and telecommunication applications, following microelectronic relays and intelligent power switches are used.

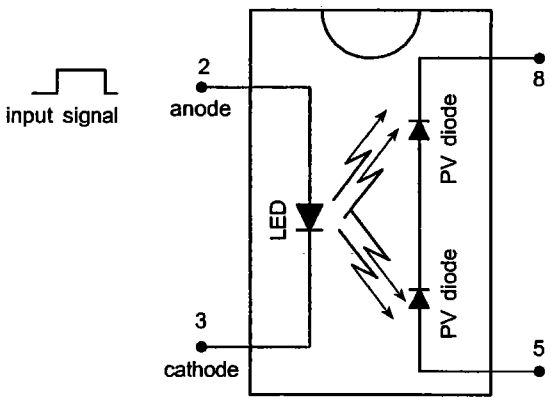
Microelectronic Relays

Microelectronic relays are power MOSFET or IGBT output photovoltaic relays, where the output switch is controlled by radiation from a *GaAlAs* light-emitting diode (LED), optically isolated from the output (Fig. A11). Such relays have the following features:

- Replace electromechanical and reed relays (EMR)
- Up to 1000 times longer life than EMR
- Up to 50% smaller than EMR
- High sensitivity
- Solid-state reliability
- Up to 4000-V galvanic isolation.



(a) A microelectronic relay



(b) A photovoltaic isolator

Figure A11 A MOSFET based microelectronic relay and a photovoltaic isolator. (*Courtsey:* International Rectifier).

Photovoltaic Isolators (Photovoltaic Opto-isolated Solid-state Relay)

Photovoltaic isolators generate an electrically isolated DC voltage upon receipt of a DC input signal and are capable of directly driving MOSFET or IGBT gates. The output is controlled by radiation from a *GaAlAs* light-emitting diode (LED), optically isolated from the output.

Intelligent Power Switches

Ultra-low $R_{DS(on)}$, fully protected MOSFET switches, offered in low- and high-side configurations, include the following protection features:

- Over-current protection
- Over-temperature protection
- ESD protection
- Active clamp.

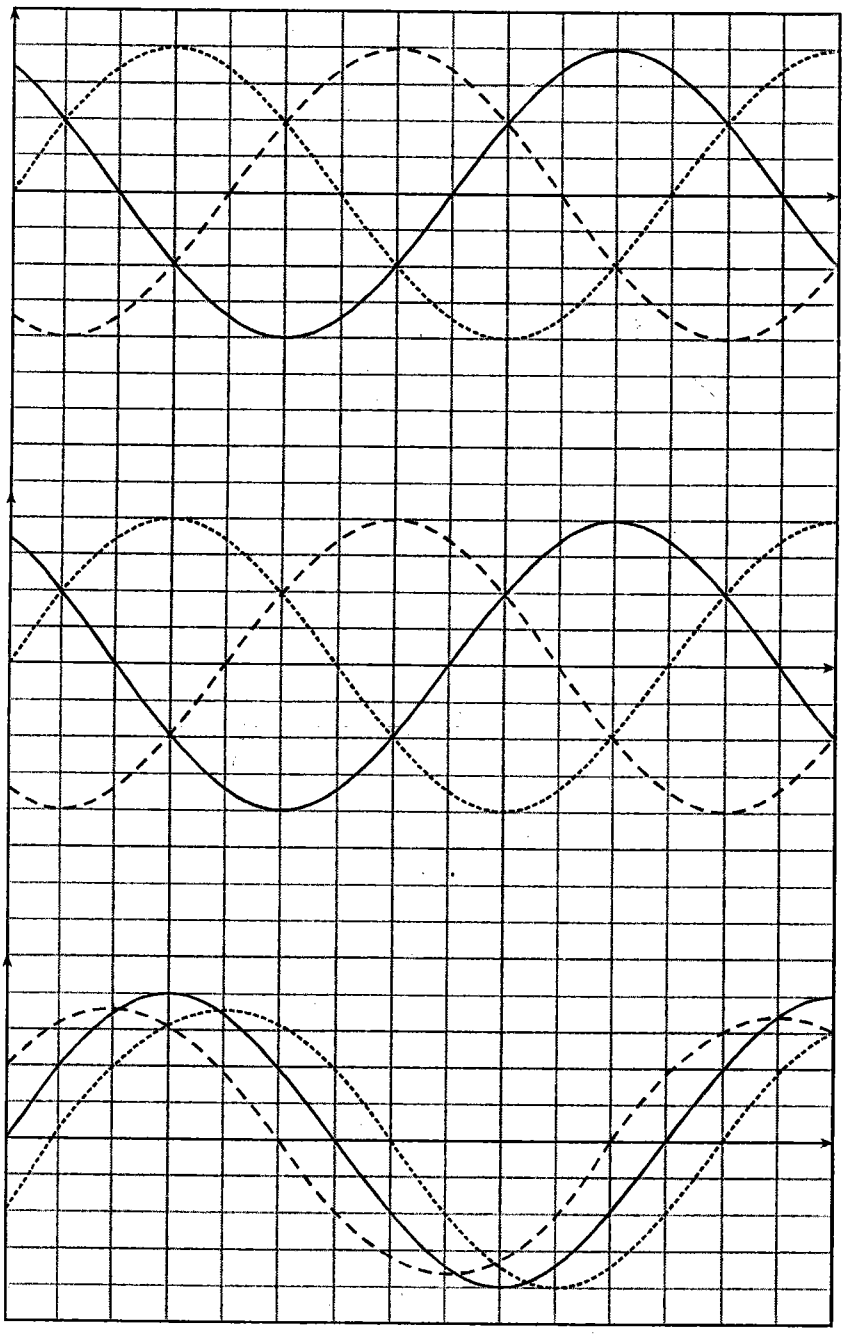


Figure A12 Waveform exercise sheet-1 (developed by Jamil Asghar, Department of Electrical Engineering, Aligarh Muslim University, Aligarh).

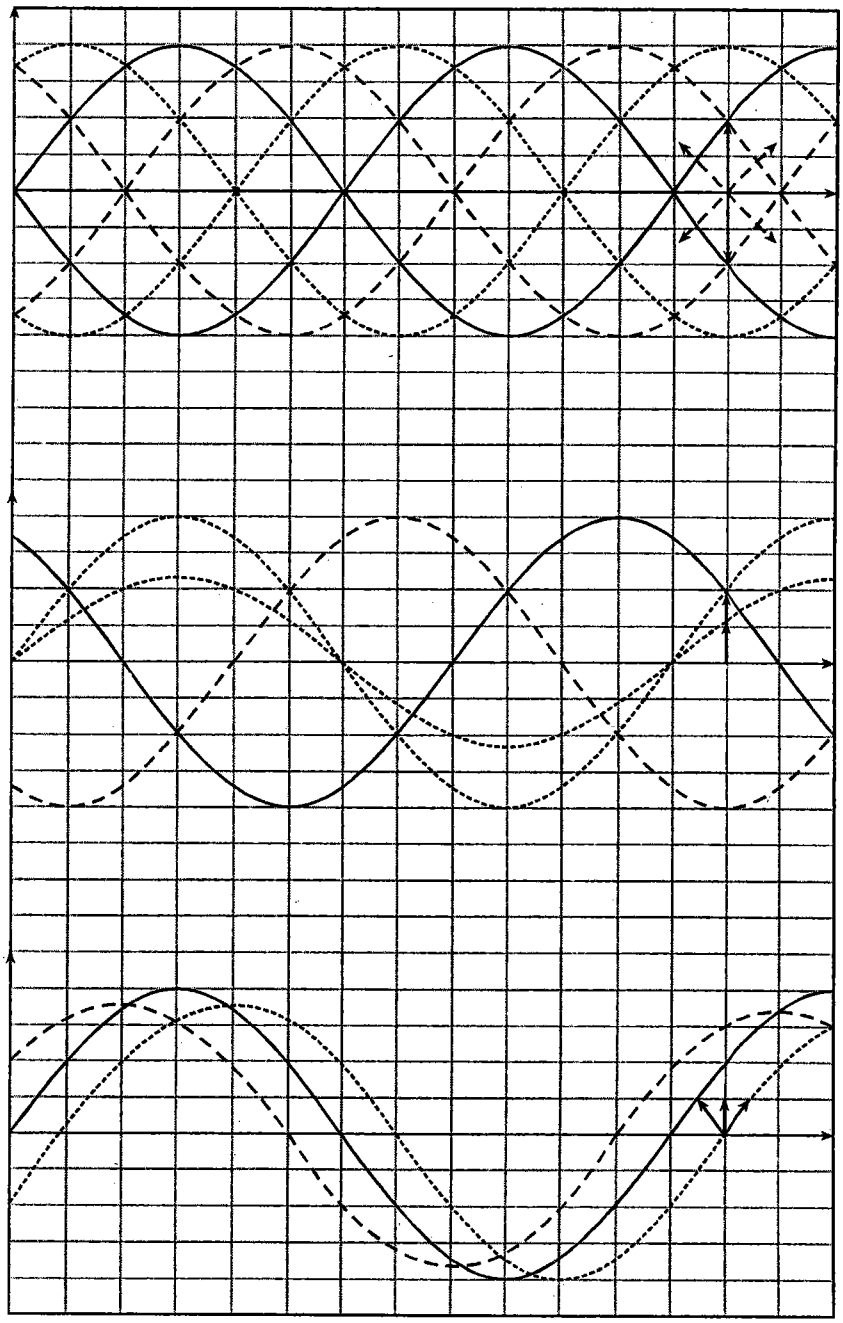
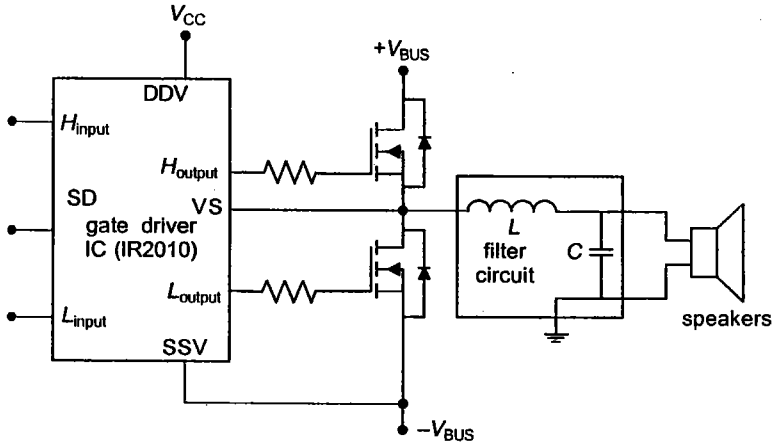
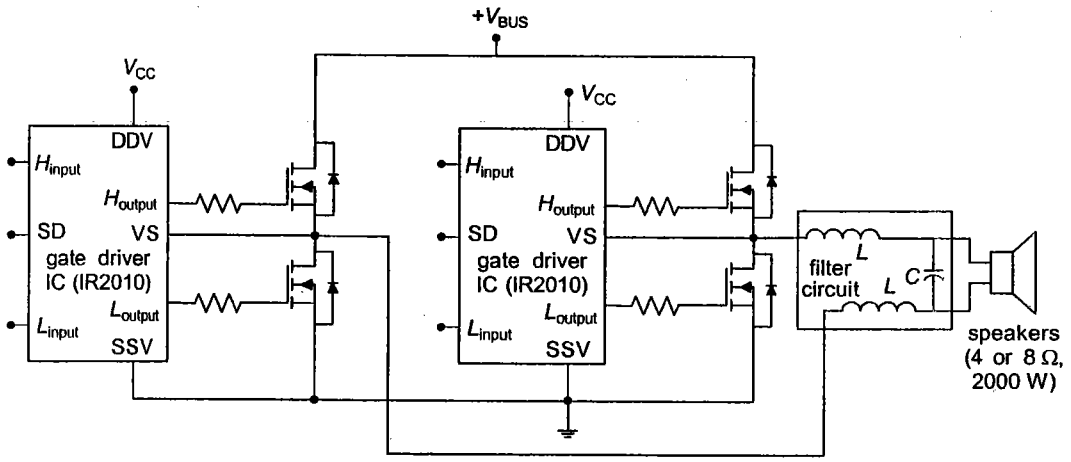


Figure A13 Waveform exercise sheet-2 (developed by Jamil Asghar, Department of Electrical Engineering, Aligarh Muslim University, Aligarh).



(MOSFET-IRFR18N15D or IRFP264N, DC bus = ±20 to ±105 V, output power = 35 to 1000 W, 4 Ω)
(MOSFET-IRF7473 or IRFP254N, DC bus = 26 to +105 V, output power = 35 to 500 W, 8 Ω)

(a) Half-bridge circuit topology



(MOSFET-IRF7389 or IRFP260N, DC bus = 24 to 149 V, output power = 50 to 2000 W, 4 Ω)
(MOSFET-IRFR4105 or IRFP264N, DC bus = 26 to 210 V, output power = 30 to 2000 W, 8 Ω)
(Driver IC-IR2113S is used with IRFP series MOSFET, e.g. IRFP260N/IRFP254N/IRFP254N/IRFP264N)

(b) Full-bridge circuit topology

Figure A14 MOSFET and gate driver IC for PWM, class D, audio-amplifier circuit topology (PWM switching frequency up to 400 kHz and maximum modulation index, M = 85%). (Courtesy: International Rectifier, El Segundo, CA90245, USA.)

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Answers

Chapter 1

10. 1.42 MW; 14200 kWh

Chapter 2

16. With turning-on time and turning-off time, 2 μs and 25 μs, respectively; f_{max} = 37.037 kHz at 125°C with turning-on time and turning-off time, 2 μs and 11 μs, respectively; f_{max} = 76.9 kHz at 25°C.

Chapter 3

Follow example 3.6: R = 670 kΩ and C = 0.01 μF

Chapter 5

3. PF = 0.89, V_o = 206 V

4. $I = \sqrt{2}I_1$

5. β = 215°, V_o = 112.77 V for V = 230 V or V_o = 0.49 V

7. I_1 = 12.23 A, I = 12.49 A, THD = 20.7%

10. I_o = 12.5 A

11. 282.84 V

Chapter 6

7. THD = 0.483, PF = 0.9, 0.83, 0.636, 0.344, 0, –0.483 and 0.636.

9. Figure (a): No control of T_1, works as a half-wave uncontrolled converter.
Figure (b): No control of D_1, works as a half-wave controlled converter.
Figure (c): A half-wave uncontrolled converter with controlled free-wheeling (V_o = 0 from $\omega t = 3\pi/2$ to 2π)

Figure (d): The load voltage is positive and negative respectively for the conductive periods of the bridge α to β and $(\pi + \alpha)$ to $(\pi + \beta)$, respectively. Because the load is at the ac side.

Figure (e): It works as full-converter in the positive half-cycle and semi-converter in the negative half-cycle.

15. (i) 181 V, 34.6° (ii) −79 V, 111°

16. (i) $\alpha_1 = 34.6°$, $\alpha_2 = 145.4°$, (ii) $\alpha_1 = 111°$, $\alpha_2 = 69°$

17. PF = 0.477, THD = 31.08%

CHAPTER 7

2. 88%

12. 1.544 A, 0.05 A, 0.8 A, 24 V

13. 9 A, 11 A, 100 V, 5 N–m

14. $t_c = 40$ μs

15. 1.222

16. 874 V

17. (a) 21.74 μF (b) 92 V (c) 100 μs (d) 200 μs

18. (i) 19.41 A (ii) 0 A (when i_a becomes zero, free-wheeling diode does not allow a negative current).

CHAPTER 8

15. (a) 27.01 V, (b) 180 W, (c) 60 V, (d) Third harmonic, 0.333, (e) 4.24 A, 3 A

16. (a) 54.02 V, (b) 720 W, (c) 60 V, (d) Third harmonic, 0.333, (e) 8.48 A, 6 A

17. (a) −10.80 A, (b) $\pm 24(1 - 1.462e^{-100t})$, (c) 12.6% (d) 3.8 ms and 6.2 ms

20. (a) 8.07 A, (b) 8.77 A, (c) 42.54%, (d) 769.13 W, (e) 3.496 A

21. (a) 125°, (c) 8.33 A

22. (a) 3.84 kW, 16 A (b) 72°, 2.304 kW or 144°, 4.608 kW

23. 31.08%, 13.26%

24. 31.08%, 1.97%

25. (a) 84.85 V, (b) 55.92 V (c) 114.12%

26. (a) 22.61 A, (b) 16 A, (c) 15.33 kW, (d) 31.95 A

27. (a) 19.59 A, (b) 13.86 A (c) 11.52 kW (d) 24 A

28. (a) 17.96 A, (b) 31.11 A, (c) 22 A, (d) 9.676 kW, (e) 43.98 A

29. (a) 15.56 A, (b) 26.95 A, (c) 19.05 A, (d) 7.263 kW, (e) 33.02 A

CHAPTER 9

17. $V_{i(max)} = 80$ V, $T_{on} = 1.16$ μs, $T_{off} = 2.7$ μs, $f_{s(max)} = 257.7$ kHz

18. $t_1 = 0.053$ μs, $t_2 = 0.25$ μs, $t_3 = 0.0587$ μs, $T_{on} = 0.356$ μs, $f_s = 1.2$ MHz

19. $L = 0.153$ mH, $C = 0.1$ μF, $Y(j2.4\omega_o) = 0.13/R$, $V_{3(max)} = 33.3$ V, $I_{3(max)} = 0.433$ A

CHAPTER 10

15. 360 W for each battery (or 360 VA for inverter).

16. (i) 7.2 hours for twenty 12-V, 150-AH parallel plate type and 2.8 hours for ten 120-AH, 12-V tabular batteries (for unity pF and lossless inverter).
(ii) 4.9 hours for plate type and 1.96 hours for tubular type (for 0.8 pF and 0.85 efficiency of inverter).

CHAPTER 11

21. $R_{\theta(c\text{-}s)} = 0.635$°C/Watt and 12.7°C

22. 248 mH, no significant change as the air-gap remains same.

CHAPTER 12

7. (i) 93 mA (ii) 59 mA

Index

AC chopper, 173–175
  multiple PWM control, 176
AC phase control, 8, 16, 133
AC regulators, 13, 153–170, 177
  PWM, 395
  three-phase, 158–170
AC voltage
  control, 10
  controller, 127
  regulator, 10, 143–147
Air-cooled, 76
  forced, 76, 416, 424
Air gap, 434, 435
Ampere-hour, 400
Ampere's law, 430
Amplitude modulation ratio, 313
Analyzer
  logic, 444
  network, 444
  signal, 444
Annotated tools, 444
Apparent, 136
Astable multivibrator, 108
Automatic control, 3
Automatics voltage regulator (AVR), 397, 398
Auto-transformers, 392
Avalanche
  breakdown voltage, 17
  diode, 24

BASIC, 444
Batteries
  lead-acid, 400
  maintenance-free, 399
  storage, 399–402
  tubular, 402
B-H curve, 402, 428
Bilateral switching, 26
BJT, 71
  power, 112, 468
Blackout, 391–392
Blanking period, 199, 363, 366
Blocking junction, 416
Blocking period, 189
Bode
  plot, 45
  plotters, 444
Boltzmann's constant, 22
Breakdown voltage, 24, 26
  emitter-to-base, 121
Bridge circuit, 200
Bridge converters/inverters, 105
Buck converters
  analysis of, 449–451
  dynamic stability analysis of, 451–452

120°-conduction, 322–326
180°-conduction, 318–322, 326
C, 444
C++, 444
Calculation, 141–143
Capacitors
  bypass, 272
  filter, 449
  parasitic, 114
Carbonyl iron, 436
Carrier
  mobility, 58
  signal, 313
Ceiling fan, 8
Channel, 59
Charge circuit, 399

Chopper control, 103
Chopper frequency, maximum, 268
Choppers, 13, 16
  class-A, 254
  class-B, 256
  class-C, 256
  class-D, 256
  class-E, 256
  classification of dc, 254–256
  dc, 249
  dual, 256
  four-quadrant, 250
  resonant pulse-commutated, 260–265
  step-down, 249
  step-up, 249
  two-quadrant, 250
Circuit
  full-bridge rectifier, 449
  RLC series, 357
  -simulation tool, 442
Circuits
  crowbar protection, 413–414
  custom-built integrated driver, 118
  driver and buffer, 99, 100, 108
  emitter-follower, 117
  gate drive, 113
  LC resonant, 354
  magnetic, 429–438
  n-channel, 117
  parallel resonant, 360–362
  phase-shifting, 103
  practical triggering, 105
  pulse-forming, 103, 108
  RC phase-shifter, 105
  resonant converter, 355–362
  RLE, 256
  series-resonant, 355–360
  short-circuit protection, 125
  shunt voltage regulator, 271
  snubber, 35, 352, 395
  underdamped series RLC, 119
Clamping voltage, 23
Clock driver, 118
CMOS, 115
Commercial utility, 390
Commutation, 27, 189, 190
  angle (β), 131, 132, 232
  circuit, 260
  complementary impulse, 268
  complementary load, 268
  current, 256
  forced, 50, 256
  impulse, 256, 257
  load, 50, 256, 257, 259
  natural, 50, 251
  period, 257, 264
  resonant-pulse, 256
  voltage, 233, 256
Compact fluorescent lamp (CFL), 7
Compact fluorescent lamps, 368
Compactness, 3
Comparator, 13
Computer
  -aided analysis, 442
  -aided simulation, 442–443
  program, 141–143
  simulation, 441, 442
Conduction, 416–417
  period, 168
Conduction mode
  continuous, 274, 278–280, 281–283
  discontinuous, 274–277, 280
Conference, 13
Configurations
  full-wave, 188, 380
  half-wave, 188, 380
  ZVS, 383
Connected loads, Y and Δ, 158
Contactor, 392
Continuous rating, 41
Contractor-switch, 190
Cooling, 3
  forced, 424
  natural, 424
Coreless, 117
Cosine control, 179
Convection, 424–425
  natural, 426
Converter,
  ac-to-dc, 271
  half-wave, 375
  half-wave ZCS, 382
  parallel-resonant, 354
  resonant switch, 386
  series-resonant, 354
  synchronous, 406
  ZCS resonant buck, 380
Converters
  analysis of, 209–213
  boost type, 277
  buck or forward, 272–277
  buck-boost type, 281–283

circuit topology of, 283
class-E, 368–371
cuck, 284–287
dc-to-dc, 249, 272–296
dual, 236, 237
flyback, 287–291, 403, 404, 410
full, 188, 211–213
full-bridge, 295–296
full-wave, full, 201–205
full-wave, half-controlled, 197–201
full-wave, uncontrolled, 193
fully-controlled, 188
half-controlled, 16, 188, 195–213
half-wave, fully-controlled, 196–197
half-wave, half-controlled, 197
half-wave, uncontrolled, 189–192
LE resonant, 368–371
line-commutated, 215
load resonating, 362–371
multiple, 236–241
naturally-commutated, 188
parallel dual, 236
parallel loaded resonant, 362
push–pull, 294–295
reactive power of, 244–245
resonant, 365–368, 410
resonant ac link, 386
resonant dc link, 382–386
resonant-switch, 371–382
self-commutating, 362–371
semi-, 188
series multiple-stage, 236, 239–241
series resonating, 363–364
six-pulse, full-wave, 225–229
six-pulse, full-wave, uncontrolled, 219
six-pulse, mid-point, uncontrolled, 219
step-down, 272
three-phase, 213–230
three-phase, uncontrolled, 216–222
three-pulse controlled, 222
three-pulse dual, 238–239
three-pulse half-wave, 222–224
twelve-pulse, 241–244
twelve-pulse parallel, 242–243
twelve-pulse series, 242–243
uncontrolled, 188, 216–217
ZCS resonant-switch, 380–382
ZVS resonant-switch, 375–380
Critical equipments, 389
Crowbars, 44
Current
circulatory, 236, 237, 238
eddy, 436
fault, 411, 413
gain, 55, 112
leakage, 16
limit control (CLC), 253
limiting inductor, 238
limiting protection, 404
non-circulatory, 236, 237, 238
peak controllable, 71
resonating, 264
reverse-leakage, 17, 22
reverse-recovery, 40
ripple, 242
Custom-built driver ICs, 99
Cyclo-converters, 10, 13, 16
step-up, 177
three-phase, 180

Damping ratio, 36
DC converters, 16
DC magnetization, 218
Dealy angle (α), 132
Delay subroutine, 108
Depletion layer, 21, 24, 65
Depth of discharge (DOD), 400
Device capacitances, 113
Diacs, 26
Digital multimeter, 444
Diode, 21, 73
drift region, 22, 59, 64
fast-recovery, 76, 352, 366, 416, 427
freewheeling, 198, 191, 224-225, 229, 239, 259, 268, 273, 292, 403
rectifiers, 20
Schottky, 17, 23
zener, 24, 44, 271
Direct frequency-changer, 177
Direct integration, 150
Discontinuous mode, 273
Distortion
factor, 308
total harmonic, 308, 392
Distributed generating (DG), 447
Disturbances, types of, 390
Doping (impurity), 28
level, 65
Double diffused structure (DMOS), 57, 64

Double impedance, 168
Driver circuits, 123–125
  design considerations of, 118
  IGBT, 120
Duty ratio, 403, 419, 422
Dynamic equalization, 47
Dynamic model, 34–35
Dynamic switching, 31–35
  load line, 66

Eddy current, 436
Efficiency, 3
Electric
  charge, 22
  field, 29
  power utility, 1
  vehicles, 400
Electrical analog, 431–432
Electromagnetic compatibility (EMC), 415
Electro-mechanical reed-relay (EMR), 392
Electro-mechanical switches, 11
Electron-hole pair, 52
Electronics Workbench, 444, 446–447
Electronic tap-changes, 170–172
Electro tap-changers, 394–395
Emissivity, constant, 425
Emmisivity factor, 426
Empirical formula, 419, 420
Energy
  magnetic stored, 435
  recovery snubber, 39
  storage, 435–438
Enhancement, 59
  type, 60
Epitaxial layer, 22
Equation editor, 444
Extended drain, 59
Extinction angle, 148, 191
Extrinsic layers, 21

FACT control, 409
Fairchild, 271
Feedback winding, 292
Ferromagnetic materials, 428, 438
Ferro-resonance, 393
Fibre optic, 102
Field-effect transistors, (FET), 17
Filter inductor, 241
Filters
  LC, 396
  RFI, 396
First breakdown, 55
First quadrant, 196, 222, 229, 237, 241
Flip-flop, 103
Flow
  heat, 425
  laminar, 425
  turbulent, 425
Flux density, 428, 430
  residual, 429
Flux linkage, 433
Flywheels, high-speed, 400
Forced current sharing, 50
FORTRAN, 444
Forward biased, 21, 28
Forward blocking, 28–29
  voltages, 46
Forward conducting, 29
Forward conduction, 21
Forward mode, 292
Forward recovery time, 17
Forward-repetitive maximum voltage, 52
Fourier analysis, 444
Fourier series, 171, 312
  expansion, 136, 139
Fourth quadrant, 202, 222, 229, 236, 237
Frequency
  deviation, 390
  modulation, 252
Fringing effect, 435
Fuel cell, 400
Full wave, 147–153
  configuration, 375
Function generators, 444
Fundamental components, 315

Gallium arsenide, 17
Gallium nitride, 17
Gas-filled rectifier diodes, 10
Gas-filled triode, 10
Gate-commutation devices, 20, 53–71
Gate
  characteristics, 39
  control, 31
  recovery period, 40
  resistor, 120
  structure, 57

Gating signal, 301
Gate turn-off thyristors (GTO), 72, 73
  gate-driver circuit, 122
  symmetrical, 54
Gate voltage, non-trigger, 81
Germanium power diode, 10
GLS bulb, 7
GLS lamp, 7
Graphical-user interface (GUI), 443
  technology, 443

Half-cell, 70
Harmonic analysis, 136–143, 150
Harmonic contents, 136
Harmonic distortion, total, 138
Harmonic factor, 138, 307
Harmonics
  higher-order, 395
  lowest-order, 308
Heat
  flow, 416–417, 424–426
  sinking, 76
Heating, 3
Heat sinks, 76, 415, 416, 417
  custom-built, 417, 426, 427
Heat transfer
  coefficient, 416
  mechanism, 416
HEXFET, 58
High-level languages, 444
  packages, 444
High-rupturing capacity (HRC) fuse, 43, 411
Hockey-puck, 417
Holding current, 30, 72
HVDC system, 8
Hysteresis loss, 402, 436

Ideal switch, 18
IEEE standard, 392
Ignitron, 10
Impedance
  of ac source, 231
  angle, 148
Impulse energy, 413
Inductance, common-emitter, 66
Inductances
  calculation of, 433–434
  leakage, 395
Inductor
  linear, 393
  smoothing, 251
Inductors, 434
  pure, 153–158
Installations, 8
Integral cycle control, 16, 128, 181
  technique, 134
Integrated circuits (ICs)
  chip IR2110, 125
  custom-built, 106, 271, 403
  gate-driver, 408
  linear, 99
  PWM, 404
Intrinsic module, 99
Intrinsic stand-off ratio, 25, 94
Intrinsic temperature, 415
Inverse definite minimum time, 413
Inversion, 188
  mode, 238
Inverter
  grade, 364
  grade SCR, 253
  line-commutated, 299
  McMurray-Bedford, 333–336
  modified McMurray, 330–333
  operation, 233
  PWM, 398
  three-phase, 318
  three-phase current-source, 328–330
Inverters, 10, 13, 16
  auxiliary commutated, 301
  classification of, 299–300
  complementary commutated, 301
  current-source, 300, 326–330
  forced-commutated, 301
  force-commutated thyristor-based, 330–336
  full-bridge, 306–307
  line-commutated, 300
  parallel, 301
  performance parameters of, 307–308
  phase-width modulated, 300, 310–317
  PWM, 310
  series, 300
  square-wave, 300, 308–310
  uniform PWM, 313
  voltage control of, 337–348
  voltage-source, 300, 301–305
Ionization, 60
Isolation, 272–296

Journals, 11, 13
Junction temperature, 22, 81, 416, 423

Kirchhoff's current law, 320

LASCR, 85
Latching current, 30, 35
LC filter circuit, 273
Level detector, 395
Light-emitting diodes (LEDs), 26
Lighting, 3
Line, 188
List of subscipts, 41–42
Litz wire, 77, 436
Load
  delta-connected, 165, 320
  line, 82
  R, 143–147
  RL, 147–153
  RLE, 205, 207
  star-connected, 320
Load current, 150, 153
  continuous, 198
  discontinuous, 198
Logic analyzer, 444
Loop-voltage equation, 260
Low-Schottky, 115

Magnetically hard materials, 429
Magnetic circuits, 429–438
Magnetic components, 410, 427
Magnetic field intensity, 428, 430
Magnetic materials, 427–429
  hard, 427
  soft, 427, 428
Magnetic saturation, 393
Mains diode, 22
MAST language, 447
Mastering triggering control (MTC), 103
MATHEMATICA, 444
MATLAB, 444
Matt-black, 420, 425
Maximum junction temperature, 76
Maximum possible gate power dissipation, 81
Mechanical relay, 392
Mechanical switch, 224
Melting period, 413
Mercury-arc rectifiers, 10
Mercury-carbon electrodes, 10
Mercury-vapour tube light, 7
Metal-oxide semiconductor field-effect transistor (MOSFET), 56–63, 72, 73
  depletion-type, 61
Mica sheet, 419
Microelectronic switches, 398
Miller effect, 114
Miniaturized circuit breakers (MCB), 411
Modulation index, 313
Modules
  intelligent/smart, 78
  smart power, 78

Natural cooling, 76
Natural frequency, 273
Natural switching point, 215
n-channel, 58
Negative temperature coefficients, 40
Noise protection, 414–415
Non-overlap mode, 366
Non-sinusoidal, 136
Numerical technique, 150

Off-period, 128
Off-state impedance, 16
On-period, 128
On-state resistance, 16, 56, 57, 59
On-state voltage, 17
  drop, 264
Open-loop system, 451
OPERA, 428
Operating frequency, 364
Optical fibre, 100
Opto-couplers, 85
  IC, 100, 102
Output voltage. 150
  control of, 338–339
Over-current, 410
  fault, 410
  protection, 43–44, 411–413
Overlap, 231–236
  angle, 233
  node, 366
  period, 231
Overload, 413

Over-voltage, 390, 392, 410, 413
protection, 44, 413

Parallel connections, 48–50
Parallel drafting factor, 49
Parasitic junction-capacitance, 378
Parasitic oscillations, 378
Peak inverse voltage (PIV), 83, 217
Permeability
constant, 428
perfect, 428
relative, 429
Permeance, 431
PF correction, 78
Phase-controlled converters, 10
Phase-controlled switching, 130–133, 181, 188
discontinuous, 16, 181–185
Phase-controlled technique, 10
Phase-shifting RC network, 93
Photodiodes, 26
Photo logic gate, 100
Photo SCR, 100, 102
Photo transistor, 100, 102
Photo triac, 100
Pilot SCR, 39
P-I-N, 17
Pinches-off, 59
Pinch-off voltage, 61
p-channel, 58
PLECS, 447
p-n junction, 21
Polysilicon, 57
Power
clean, 392
conditioning unit, 398
consumption, 7
dissipation, 76, 416
electronic controllers, 13–16
electronic devices, 18–19
input, 138
modules, 77–78
MOSFET, 408
outage, 391–392
quality, 392–396, 397
supplies, 3
utility, 410
zener diodes, 24–25
Power bipolar-junction transistors (BJT), 55–56
base drive, 121, 122
Power diodes
fast-recovery, 24
general-purpose, 22–23
Power electronics, 1
applications of, 3
evolution of, 10–13
Power factor (PF), 129, 133, 136, 181, 240
angle, 148
correctors, 405–408
displacement, 137, 175
distortion, 138
fundamental, 137
input, 138, 338
linear, 399
Power pulse
non-rectangular, 422
rectangular, 422
Power supplies
linear dc, 269–272
switched mode, 402–405
Power supply
linear, 399, 402
switched mode, 249, 390
uninterrupted, 389
Pre-arcing, 413
Press-pack, 417
Primary breakdown, 55
Printed circuit board (PCB), 118
Programmable peripheral interface, 108
Propagation delay, 115
PSCAD, 447
PSIM, 444, 447
PSPICE, 444, 446
simulation, 448
tools, 448
p+ substarte, 64
Pulse transformer, 85, 103
Pulse-width modulated inverter, 16
Pulse-width modulation (PWM), 252, 299
control, 403
multiple or uniform, 311
single, 311
sinusoidal, 311, 313
technique, 408
Punch through, 55, 65

QBASIC, 145
Quality factor, 357
QUICK FIELD, 428

Radiation, 425–426
Radio-frequency interface (RFI), 181, 414
Ramp signal, 108
Reactive power, 136
Recombination, 40
Recovery time, 17, 217
Rectifiers, 13, 17
  controlled, 10
  converter, 182
  operation, 214–215
  PWM, 406
  selenium, 10, 44
  silicon-controlled, 20, 27–28
  switched-mode, 125
  synchronous, 406
  uncontrolled, 16
Reduction, 424
Regenerative braking, 250
Regenerative mode, 256
Reliability, 3, 8
Reluctance, 431
Repetitive rating, 41
  non-, 41
Research and development (R&D), 11, 441
Resistance
  electrical, 416
  thermal, 416
Resonance condition, 393
Resonating circuit
  external LC, 265
Reverse biased, 21, 28
Reverse blocking, 22, 30, 54
  voltage, 22, 46
Reverse break-over, 23
Reverse recovery, 47, 352
  current, 40
  time, 22, 23, 40
Reverse-repetitive maximum voltage, 52
Ripple factor, 138
RLC series circuit, 357
RL load, 147–153
R load
  delta-connected, 168
  Y-connected, 160
RST7.5 interupt, 108

SABER, 428, 447
Safe operating area (SOA), 41, 55, 62–63, 66, 419
  forward bias, 55, 62, 66
  reverse bias, 55, 62, 66
  snubber switching, 66
  switching, 62
Saturation
  level, 436
  time, 55
SCR, 31–35, 73, 74
  asymmetric, 366
  commutation of, 50
  data sheet, 75
  light-activated, 52
  pilot, 39
Second-breakdown, 419
Semiconductor fuse, 43
Semi-converters, angle of, 210
Sequence control, 239
Servo-motor, 393
Short-time deviation, 390
Signal
  analyzer, 444
  generator, 444
Silicon, 10
  dioxide, 113
  grease, 77, 417
  oil, 417
Simulation, 443
  on-line, 447
  PSPICE, 448
  tools, 444–447
Simulators, circuit-oriented, 444
SIMULINK, 447
Single-phase gate signal, 160
Skin effect, 436
Smart power, 99
SMPS, 392
  topology, 452–453
Snubber interaction, 352
Soft start, 404
Solar photovoltaic, 249
Solid tantalum, 272
Space charge layer (SCL), 21, 29, 55, 59
Space charge limiting load, 66
Speed control, 3
Spice library manager, 444
Spongy iron powder, 436
Square-wave oscillator, 403
Stabilizer, servo-voltage, 393
Static induction devices, 66–69
Static induction diodes, 66
Static induction transistor logic, 66, 67–68
Static voltage equalization, 45
Stepfen-Boltzman law, 425

Storage
batteries, 399–402
oscilloscope, 444
times, 115
Substrate layer, 64
Surge, 41
Switches, bidirectional, 365–368
Switching angle, 32, 84, 196
Switching frequency, 361, 369
Switching losses, 382
Switching-on time, 82
Switching speed, 17, 56
Switching time, 121
constant, 119
delay, 16
turn-off, 121
Switching trajectory, 39
Switching turn-off time, 352
Switch mode, 352
Symmetric placement, 43
Synchronization, 96, 108

Thermal compounds, 77, 417–421
Thermal conducting grease, 417
Thermal conductivity, 416, 420
Thermal impedance, 421
transient, 421–424
Thermal joint compounds, 417
Thermal protection, 415
Thermal resistance, 416
Thermal turn-on, 30
Thermo-ionic valve, 10
Thyratron, 10
Thyristor
auxiliary, 332
-controlled reactor (TCR), 153, 156
main, 332
reverse-conducting, 366
Thyristors, 10, 20, 24, 27–53, 81–84
asymmetrical, 52
auxiliary, 259, 264, 301
diode model of, 32
field-controlled, 69
gate turn-off, 53
MOS-controlled, 70–71
negative group, 160, 179
positive group, 160, 179
protection, 43–44
rating, 41–50
reverse conducting, 52
series operation of, 44–50
static induction, 68–69
Time-ratio control (TRC), 103, 251
TINA pro, 443, 444
Tiny cells, 70
TMOS, 58
Transcendental equation, 148
Transformers
centre-tapped, 194
constant-voltage, 393
distribution, 392
isolation, 395
tap-changing, 187, 392
zig zag winding, 217–219
Transient analysis, 444
Transient response, 272
Transistor period, 76
Transistors, 10, 117
bipolar, 271
ferrite-core, 287
insulated-gate bipolar, 63–66
lateral punch-through, 66
metal-oxide semiconductor field-effect, 56–63
modal, 54
parasitic pnp, 65
pulse, 108
series pass, 271
silicon-steel core, 287
static induction MOS, 66
switching, 103
Trapped energy, 292
Triac, 51–52, 73
photo, 100
Triggerable monostable, 108
Trigger circuits, 86–87
ac thratron type, 93–94
ac type, 87–89
advanced, 94
diac, 91–93
full-wave type, 90–91
half-wave type, 89–90
microprocessor-based, 108
RC, 87–91
resistance, 86–87
UJT-based, 94–99
Trigger, extended pulse, 160
Triggering, 30
light, 31
Trigger sequence, 160

Triode, 52
TR load configuration, 165
TTL
  families, 115
  IC, 102, 115
  open-collector, 115
Tunnel diodes, 24–25
Tunneling effect, 25
Turn-off, 20
  characteristics, 40
  snubber, 35
  time, 123
Two-pulse, half or semiconductor, 197–198
Two-resistor model, 32–35

Undamped oscillation, 354
Under-damped circuit, 36
Under-damped oscillation, 354
Unidirectional device, 202
Unijunction transistor (UJT), 25–26
Uninterrupted power supply (UPS), 389, 396–399
  off-line, 397
  off-line, interactive, 398–399
  off-line, preferred, 397–398
  on-line, 397
  on-line, preferred, 399
  shutdown of, 399
Unipolar device signals, 112
Unipolar switching scheme, 316
Unsymmetrical blocking, 67

Vacuum, 10
  triode, 67
Vapour lamp, 10
Varistors, 44
  metal-oxide, 395
Virtual instruments, 444
Visual BASIC, 444
VMOS, 57
Voltage
  chopped distorted, 391
  clamp, 44
  complementary commutation process, 264
  deviations, 390, 392–395
  fundamental, 358
  gain, 357
  mid-point, 232
  regulators, 392, 395
  spikes, 390, 395
  stabilizers, 392
  trajectories, 352
  transients, 410
Voltage equalization, transient or dynamic, 47–48
Voltage pulses, non-repetitive, 395
V-shape structure, 57
VTB, 447

Wave-shaping, 178
WebMATHEMATICA, 447
Welding, 3
WOLFRAM Research, 447
Work horse, 399

XY recorder, 444

Zero-crossing detector (ZCD), 108
Zero-crossing instant (ZCI), 103, 105, 128, 358, 394
Zero-crossover instant, 222
Zero-current switching (ZCS), 66, 354, 371, 415
  resonant switch converters, 380–382
Zero-voltage switching (ZVS), 66, 128, 181, 354, 371, 425
  configuration, 383
  multi-resonant, 374
  resonant-switch converters, 375–380